Chapter 02 FET Amplifier

$V_{GS} \rightarrow DC$
$V_{gs} \rightarrow AC$

JFET Small Signal model :-

* The Gate to Source voltage (V_{gs}) ~~controlles~~ controls the Drain to Source channel current [I_{DSS}] of a JFET.
* ~~[illegible]~~ DC. Gate to Source Voltage (V_{gs}) control level of DC Drain current Given by to a relationship. Known as Shockleys Equation

$$\left\langle I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \right\rangle \rightarrow (1)$$

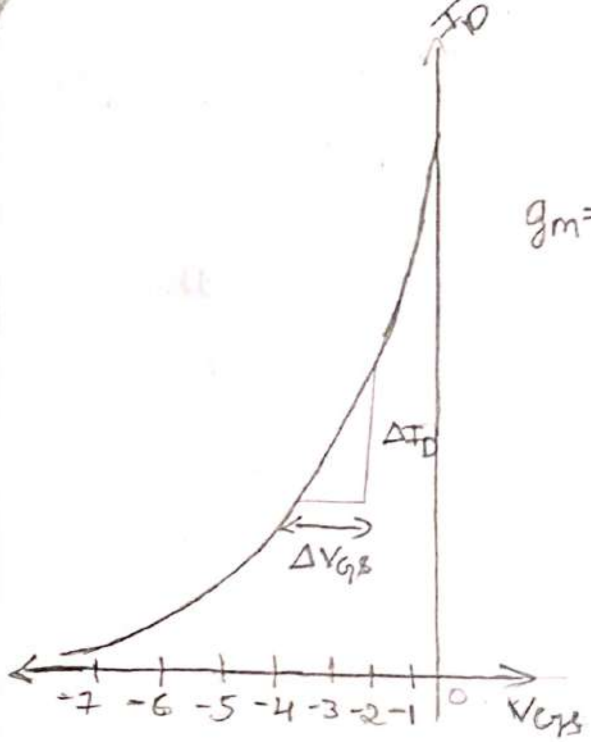
V_P :- pinch of voltage.
V_{GS} :- gate to Source voltage.
I_{DSS} :- Drain to Source channel current
I_D :- Drain Current

* The Change in Drain current (ΔI_D) $\Delta I_D \rightarrow I_{D2} - I_{D1}$ that will result form a change in ~~[illegible]~~ gate to Source Voltage (ΔV_{GS})
* can be ~~betor~~ determined using transconductance factor (g_m) In following manner.

$$\Delta I_D = g_m \Delta V_{GS}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \ (S)$$

* Graphical representation of I_D v/s V_{GS}



$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$

The transconductance also given,

$$g_m = \frac{2 I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{--- (2)}$$

$V_{GS} = 0$ then transconductance at become

$$g_{m0} = \frac{2 I_{DSS}}{|V_P|} \quad \text{---- (3)}$$

$$\left\langle g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)\right\rangle \quad \text{--- (4)}$$

Problems :-

Determine the magnitude of g_m for JFET with $I_{DSS} = 8mA$ at $V_P = -4V$. at following ~~po~~ Bias point

(a) $V_{gs} = -0.5\,V$

(b) $V_{GS} = -1.5\,V$

(c) $V_{GS} = -2.5\,V$

→

(a) $g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$

$$g_{m0} = \frac{2 I_{DSS}}{V_P}$$

$$g_{m0} = \frac{2 \times 8 \times 10^{-3}}{4}$$

$$g_{m0} = 4 \times 10^{-3}\,S.$$

$$g_m = 4 \times 10^{-3}\left[1 - \frac{(-0.5)}{(-4)}\right]$$

$$\langle g_m = 3.5 \times 10^{-3}\,S \rangle$$

(b) $V_{gs} = -1.5\,V$

$$g_{mo} = 4 \times 10^{-3}\,S$$

$$g_m = 4 \times 10^{-3} \left(1 - \frac{(-1.5)}{(-4)}\right)$$

$$\langle g_m = 2.5 \times 10^{-3}\,S \rangle$$

(c) $V_{gs} = -2.5$ $\quad g_{mo} = 4 \times 10^{-3}\,S$

$$g_m = 4 \times 10^{-3} \left(1 - \frac{(-2.5)}{(-4)}\right)$$

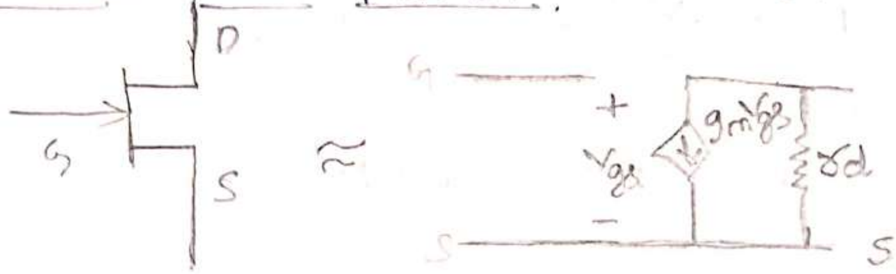
$$\langle g_m = 1.5 \times 10^{-3}\,S \rangle$$

Input Impedance for JFET : $\langle Z_i = \infty \rangle$

output Impedance for JFET :- $\langle Z_o = r_d \rangle$

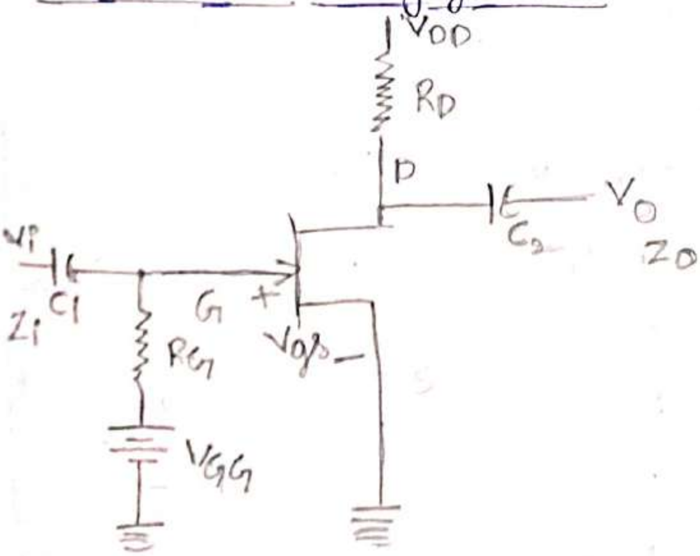
where $r_d = \dfrac{\Delta V_{DS}}{\Delta I_D} = \dfrac{1}{g_{os}} = \dfrac{1}{Y_{os}}$.

Equivalent model of JFET.

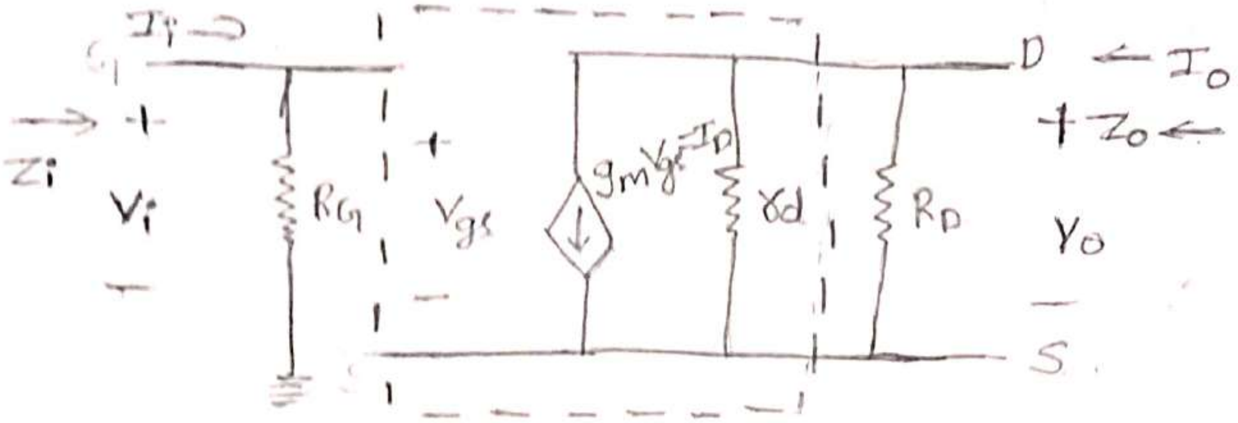


$I_D = g_m V_{gs}$

Fixed bias configuration :-



The AC Equivalent Circuit



Input Impedance is given by

$$\langle Z_i = R_G\ \Omega \rangle$$

output Impedance is given by

$$\langle Z_o = r_d \parallel R_D \rangle$$

A voltage gain is given by :-

$$A_v = \frac{V_o}{V_i}$$

$V_o = -I_o R_L$

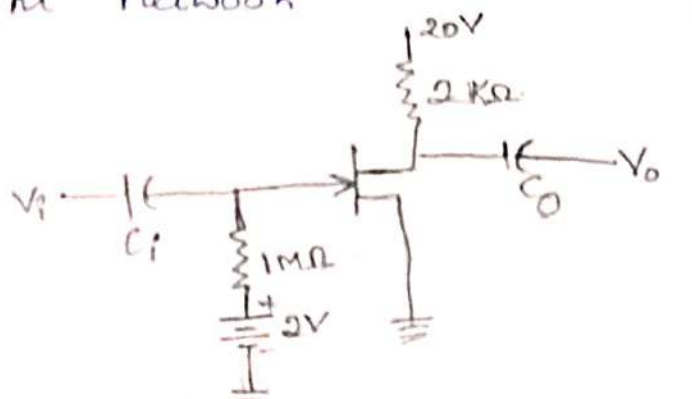
$V_o = -g_m V_{gs}(r_d \parallel R_D)$

$V_i = V_{gs}$

$$A_v = \frac{-V_{gs}\, g_m\, (r_d \parallel R_D)}{V_{gs}}$$

$$\langle A_v = -g_m (r_d \parallel R_D) \rangle$$

1. The fixed bias configuration having an operating point $V_{GSQ} = -2V$ $I_{DQ} = 5.625mA$. $I_{DSS} = 10mA$ and $V_P = -8V$. The network as shown in figure



The value $Y_{os} = 40\mu S$.

(i) $g_m = ?$

(ii) $r_d = ?$

(iii) $Z_i = ?$

(iv) $Z_o = ?$

(v) $A_v = ?$

(vi) Determine A_v by ignoring r_d

→ (iii) $Z_i = R_G$

$Z_i = 1 \times 10^{+6} \Omega$.

$\langle Z_i = 1 m\Omega \rangle$

(ii) $r_d = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{Y_{os}} = \frac{1}{40 \times 10^{-6} S} = 25 \times 10^{3} = 25 K\Omega$.

$\langle r_d = 25 K\Omega \rangle$

(i) $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$.

$g_{mo} = 2.5 mS$.

$g_m = 2.5 \times 10^{-3} \left(1 - \frac{(-2)}{(-8)}\right)$.

$\langle g_m = 1.875 mS \rangle$

(iv) $Z_o = r_d \parallel R_D$

$Z_o = (25 \times 10^{+3} \parallel 2 \times 10^{3})$

$\langle Z_o = 1.851 K\Omega \rangle$

(v) $A_V = -g_m (r_d \parallel R_D)$.

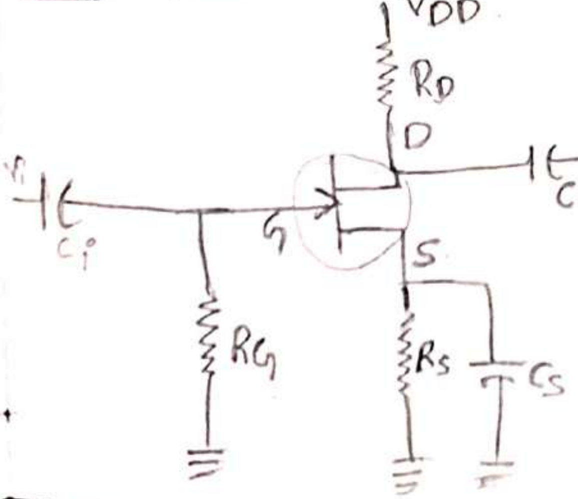
$A_V = -1.875 \times 10^{-3} (1.85 \times 10^{3})$.

$\langle A_V = -3.468 \rangle$

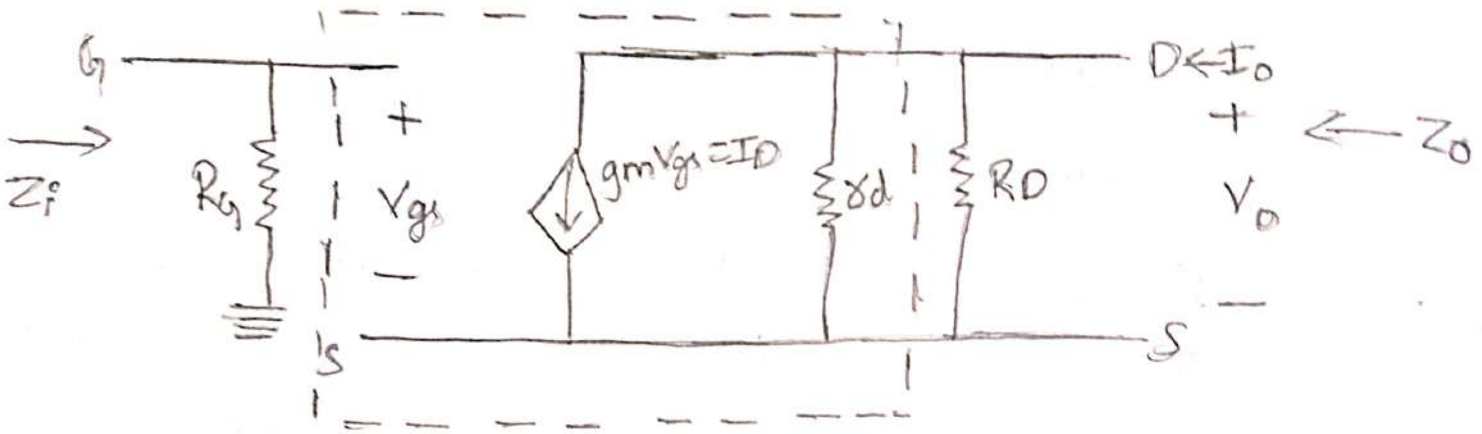
(vi) $r_d = \infty$ $A_V = -1.875 (2 \times 10^{3})$

$\langle A_V = -3.75 \rangle$

Self Bias configuration :-



AC Equivalent circuit for Self Bias given by



Input Impedance Is given by.

$\langle Z_i = R_G \, \Omega \rangle$

output Impedance Is given by.

$\langle Z_o = r_d \parallel R_D \rangle$.

(A_V) voltage gain. $A_V = \frac{V_o}{V_i}$

$V_i = V_{gs}$.

$V_o = -I_o R_L$.

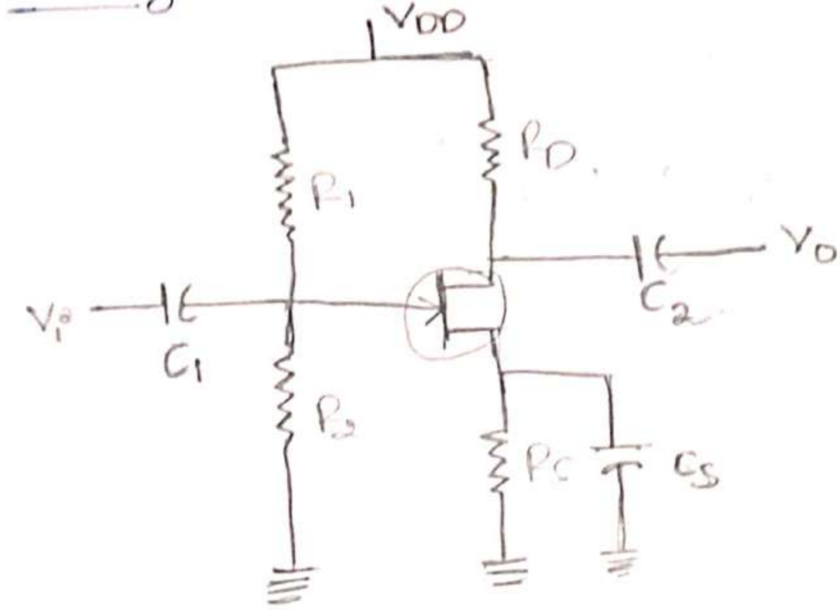
$V_o = -I_D (r_d \parallel R_D)$.

$V_o = -V_{gs} g_m (r_d \parallel R_D)$

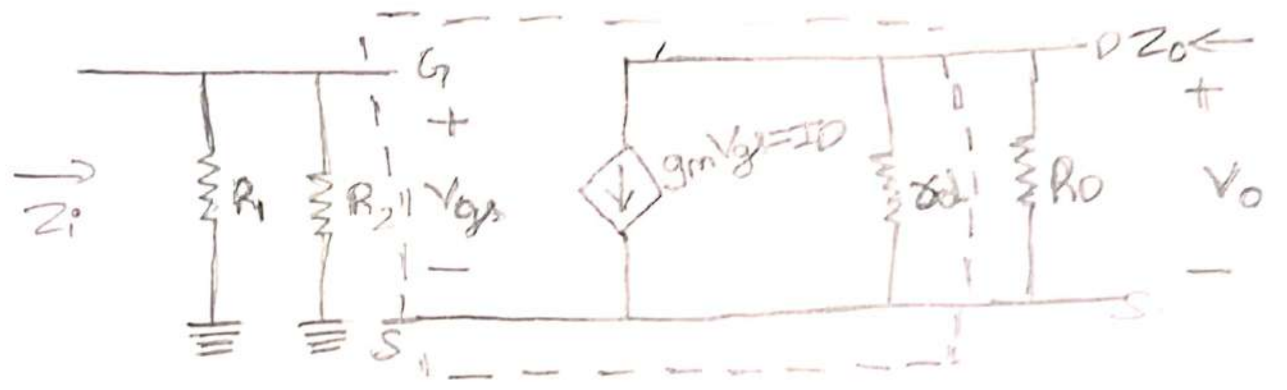
$A_V = -\frac{\cancel{V_{gs}} g_m (r_d \parallel R_D)}{\cancel{V_{gs}}}$

$\langle A_V = -g_m (r_d \parallel R_D) \rangle$

voltage divider Bias configuration :-



AC Equivalent circuit for voltage divider Bias configuration



Input Impedance is given by

$\langle Z_i = R_1 \| R_2 \, \Omega \rangle$

output Impedance is given by

$\langle Z_o = r_d \| R_D \, \Omega \rangle$

voltage gain (Av) is given by

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -I_o R_L$$

$$V_o = -I_D (r_d \| R_D)$$

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

$$V_i = V_{gs}$$

$$A_V = -\frac{g_m V_{gs} (r_d \parallel R_D)}{V_{gs}}.$$

$$\langle A_V = -g_m (r_d \parallel R_D) \rangle$$

Module - 1

Chapter-1 BJT Biasing

①

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INTRODUCTION:

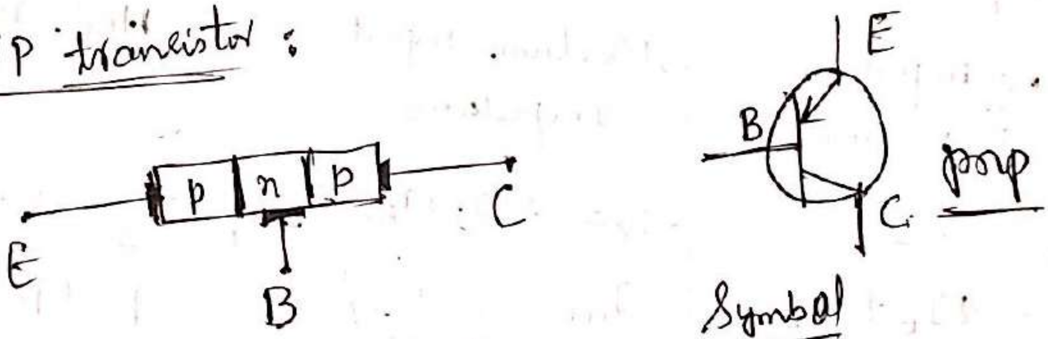
BJT stands for Bipolar (Electron & electron holes) Junction Transistor, is a Semiconductor device that is constructed with 3 doped semiconductor regions. i.e Base, Emitter and collector separated by 2 p-n junctions.

BJT are manufactured in two types.

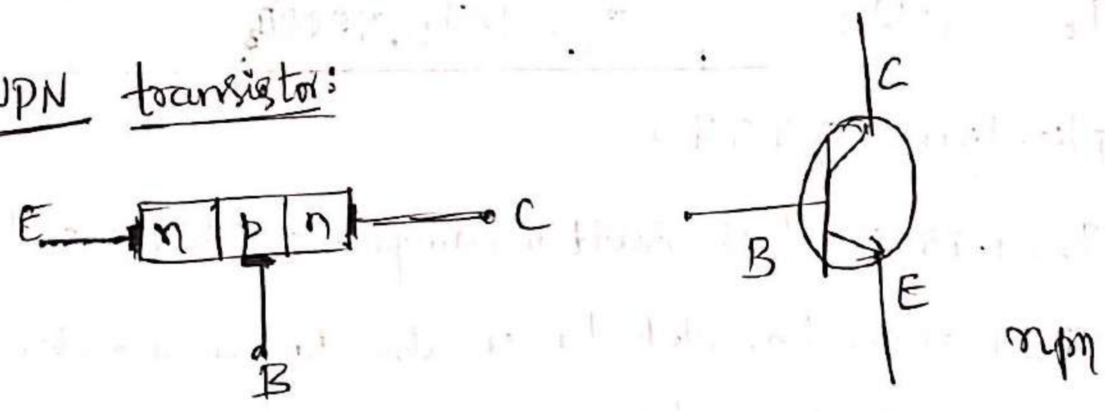
(i) PNP transistor.

(ii) NPN transistor.

(i) PNP transistor:



(ii) NPN transistor:



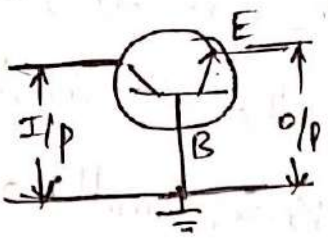
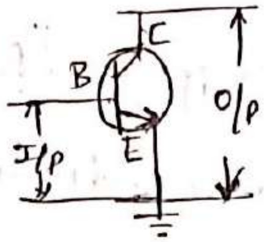
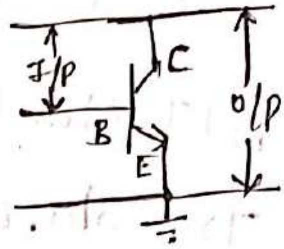
→ BJT operate in three regions,

(i) Active Region: The region in which the transistor operates as an amplifier.

(ii) Saturation Region: In this region transistor is fully on & operates as switch

(iii) Cut-off Region: In this region transistor is fully off & I_C is zero.

BJT Can be configured in three modes,

(i) Common Base Configuration	(ii) Common Emitter Configuration	(iii) Common Collector Configuration
		
→ Has Low power gain	→ Very high power gain	→ Medium power gain
→ Low current gain	→ Medium current gain	→ High current gain
→ High voltage gain	→ Medium Voltage gain	→ Low voltage gain
→ Very high output Impedance	→ High output Impedance	→ Low output Impedance
→ Low input Impedance	→ Medium input Impedance	→ High Input Impedance
→ $I_C = \alpha I_E$ $I_C = \alpha I_E + I_{CBO}$	→ $I_C = \alpha (I_C + I_B) + I_{CBO}$ $I_{CEO} = \frac{I_{CBO}}{(1-\alpha)} \Big/ _{I_B = 0}$, $I_E = (\beta+1) I_B$	→ $I_E = \gamma I_B$ $\gamma = (\beta + 1)$ $\alpha . \gamma = \beta$
→ $I_E = I_C + I_B$	$I_C = \beta I_B$,	

Applications of BJT :

(1) BJT is used as switch, amplifier, filter and oscillator.

(2) BJT is used as detector or also known as a demodulator.

(3) BJT is used in clipping circuits

(4) Logic Circuits & switching circuits use BJT..

Operating Point:- Module-1 Chapter-1 → BJT Biasing

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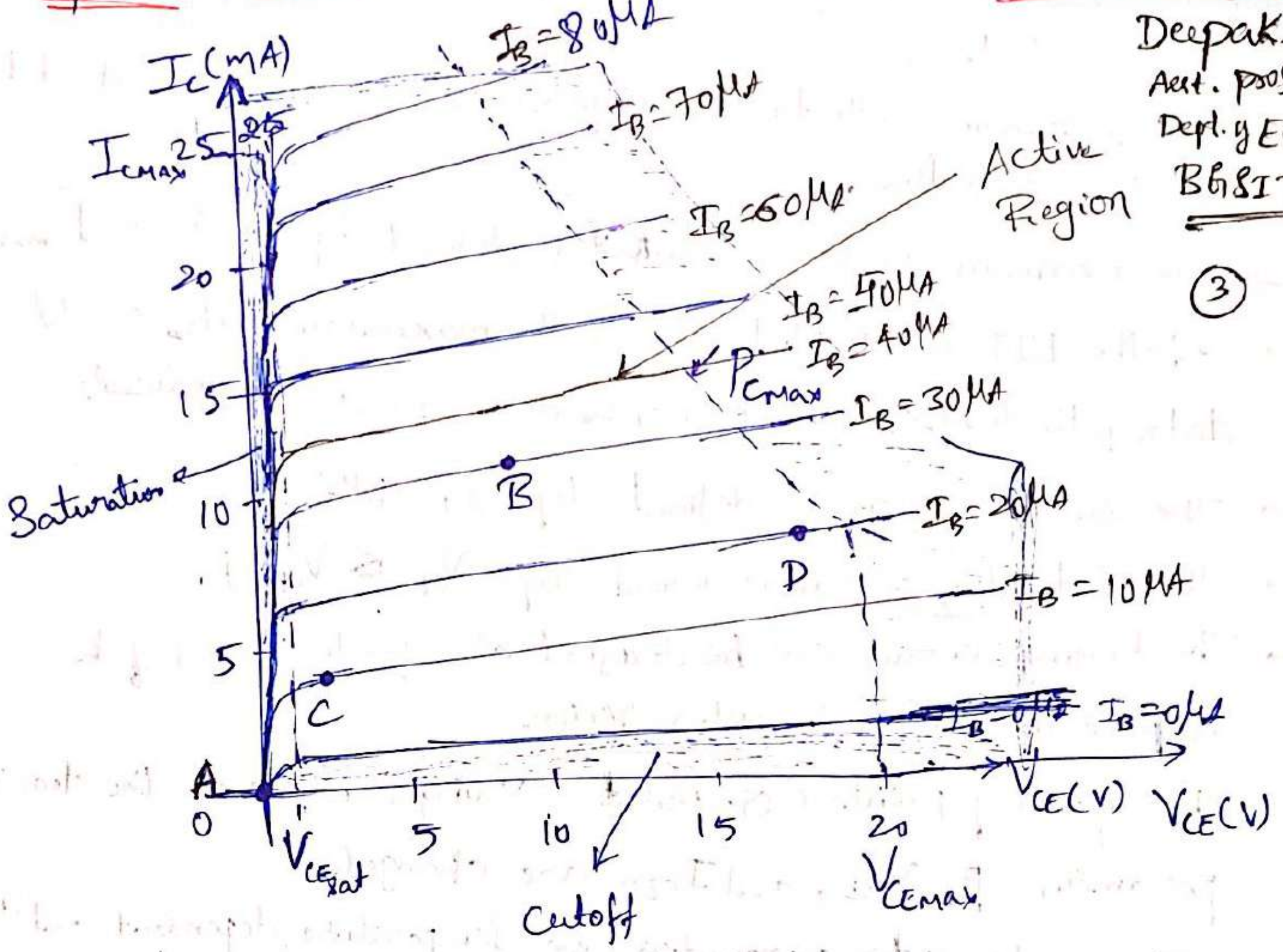

Fig: Various Operating points within the limits of operation of a transistor.

→ The process of applying DC voltage to the BJT is known as Biasing.

→ For transistor amplifiers the resulting DC current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.

→ The operating point is a fixed point on the characteristics, it is also called the quiescent point (Q-point). {Quiet, Still, Inactive}

→ The above Figure shows a general output device characteristics with Four operating points indicated. (A, B, C, D).

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→ The BJT to be biased in its linear or active region, then,

(a) the base-emitter junction must be forward-biased &,

(b) The base-collector junction must be reverse-biased.

The BJT to be biased in its cut-off region (or operation in cut-off region) then,

(a) the base-emitter junction must be reverse-biased and

(b) the base-collector junction must be reverse-biased.

The BJT to be biased in its saturation region then,

(a) the base-emitter junction must be forward biased and

(b) the base-collector junction must be forward biased.

→ The maximum collector current I_{Cmax} is indicated in the horizontal line. The maximum collector to emitter voltage V_{CEMax} is indicated in the vertical line. The maximum power constrait is defined by the curve P_{CMax}.

→ If the BJT is operated outside the maximum limits, it may reduce the lifespan of the device or would destroy the device.

→ The cut-off region is defined by $I_B \leq 0\,\mu A$. The saturation region is defined by $V_{CE} \leq V_{CEsat}$. The biasing circuit can be designed to operate at any of the Q-point or with in the active region.

→ The operating points (Q-points) changes whenever the transistor parameter β, V_{BE} & I_{CEO} are changed, these parameters (β, V_{BE}, I_{CEO}) are temperature dependent and thus the operating points are also temperature dependent.

→ The operating point should be made independent of transistor parameters β, I_{CEO}, and V_{BE}.

→ The biasing circuits can be designed to fix the operating point and can be made independent of transistor parameters β, I_{CEO}, V_{BE}.

→ Types of Biasing:

(1) Fixed Bias or Base Bias circuit.

(2) Emitter Bias or Emitter Stabilized biasing (Not in syllabus)

(3) Voltage Divider / current gain stabilized or β independent / Universal bias.

(4) DC Bias with feedback. (Not in syllabus).

→ (1) Fixed Bias or Base Bias Circuit:

Consider the circuit shown below for fixed bias. Neglect capacitor C1 and C2 for DC analysis.

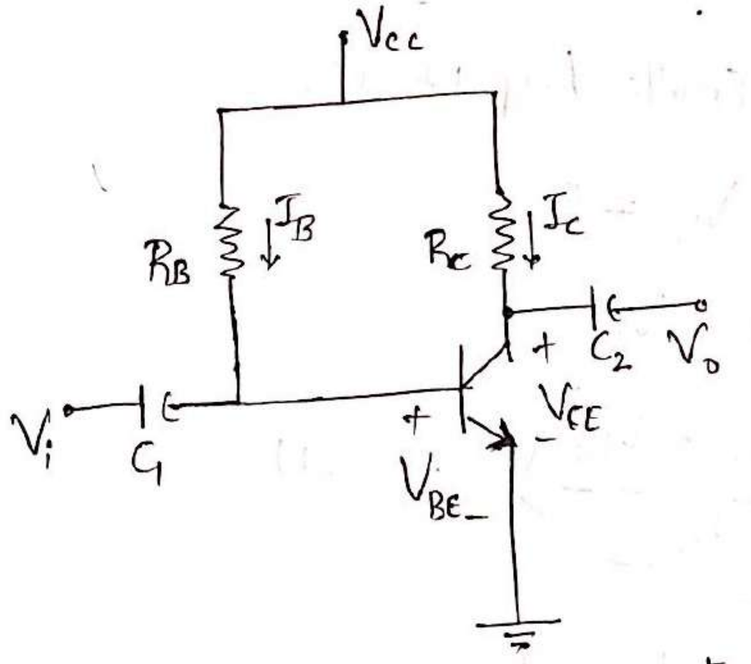


Fig: Fixed Bias ckt with Capacitor

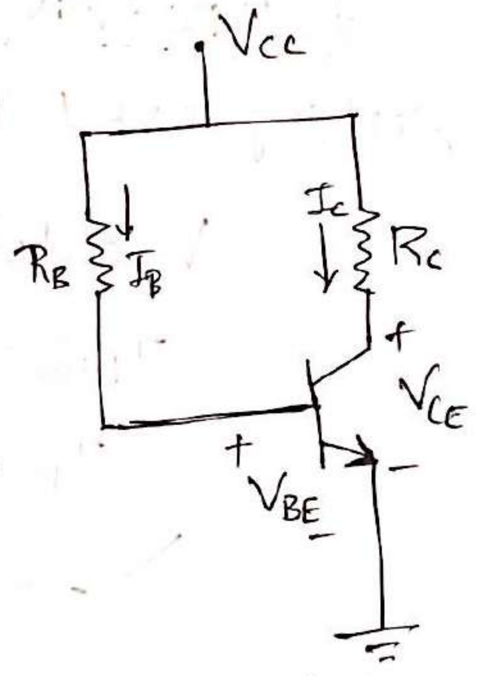
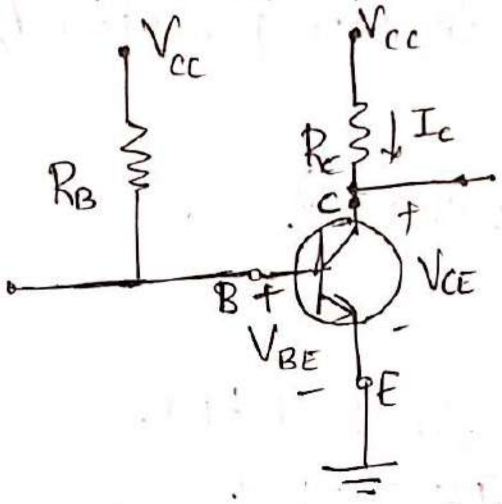
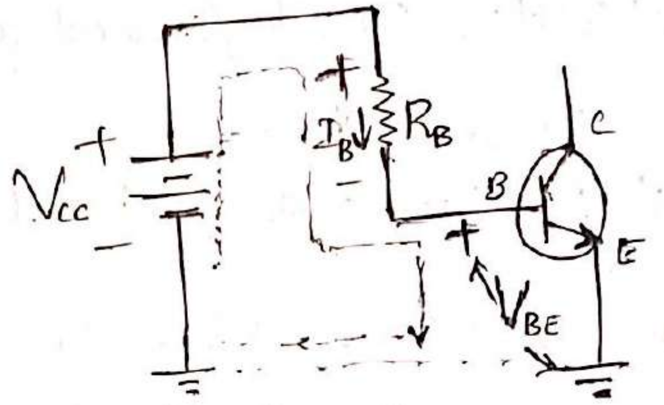


Fig: DC Bias

In fixed bias configuration the supply voltage V_{cc} and V_{BE} are constant, once the resistance R_B is selected, the base current I_B is also fixed. Hence the circuit is called Fixed bias circuit.

The Base-Emitter loop is considered for analysis of Base current and collector current (I_C) and circuit is as shown below figure(b). The figure (a) shows that, the dc supply V_{CC} separated into two supplies.





Fig(a): DC Equivalent Circuit   Fig (b): Base-Emitter Loop&

Applying KVL to Base-Emitter loop we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad \cdots (1)$$

where,

$V_{BE} \Rightarrow$ Base Emitter voltage

$R_B \rightarrow$ Base Resistance

$I_B \rightarrow$ Base Current.

The collector current is given by,

$$\boxed{I_C = \beta I_B} \quad \cdots (2)$$

→ The collector Emitter loop is considered for the analysis of V_{CE} and circuit is as shown in below Figure.

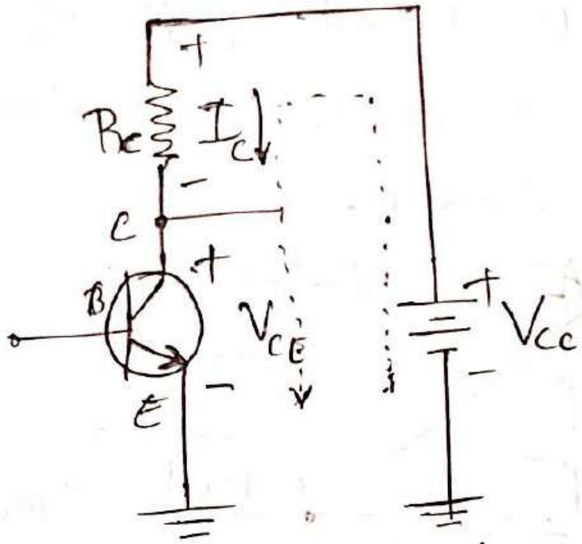


Fig: Collector - Emitter Loop

Apply KVL to Collector - Emitter Loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \quad \cdots (3)$$

where V_{CE} is the Voltage from Collector to Emitter.

from double - Subscription notation we know that,

$$V_{CE} = V_C - V_E$$

and in Fixed bias $V_E = 0$ hence $V_{CE} = V_C$.

And also,

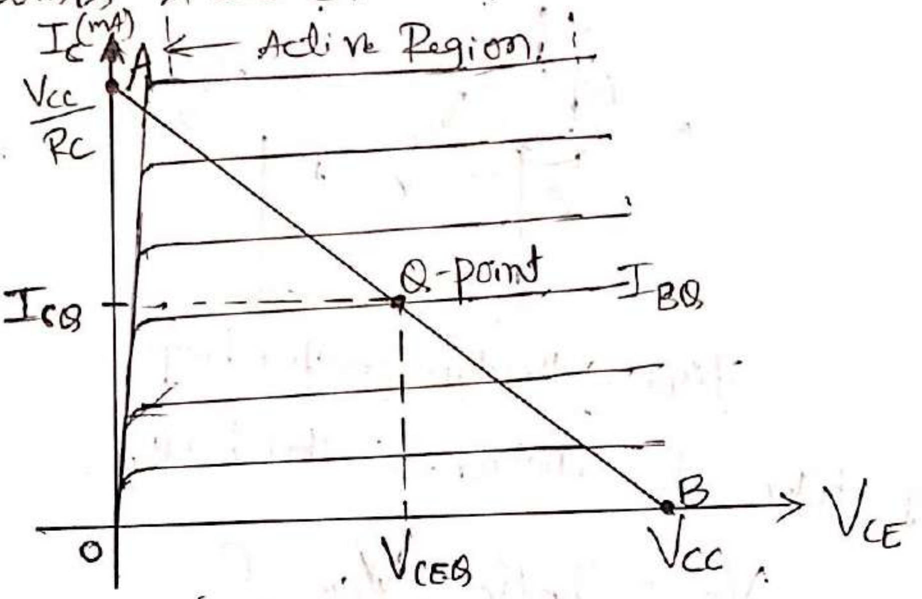
$$V_{BE} = V_B - V_E$$

$$\boxed{V_{BE} = V_B} \quad \cdots\cdots (4)$$

Since $V_E = 0$

Load-Line Analysis: (Fixed-Bias Circuit)

The output characteristics of the transistor relate the two variables I_c and V_{CE}, the o/p characteristics is as shown in below Figure and the load-line is drawn between points A and B.



To obtain point 'A':

W.K.T $\quad V_{CE} = V_{CC} - I_c R_c$

If we choose $V_{CE} = 0V$ then,

$$V_{CC} = I_c R_c$$

$$\boxed{I_c = \frac{V_{CC}}{R_C}\Big|_{V_{CE}=0V}} \quad \text{---(1)}$$

To obtain point 'B':

W.K.T $\quad V_{CE} = V_{CC} - I_c R_C$

If $I_c = 0mA$ then

$$\boxed{V_{CE} = V_{CC}\Big|_{I_c=0mA}} \quad \text{---(2)}$$

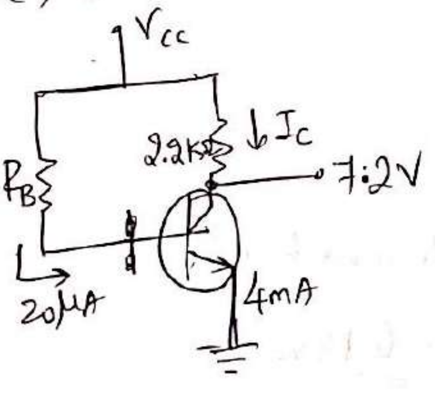
Advantages:

1. Circuit is simple.
2. The operating point can be fixed anywhere in the active region by simply changing the value of R_B. Therefore it is called Base-bias circuit or Fixed bias circuit.

Disadvantages:

1. Stabilization of operating point is very poor in the fixed bias circuit.
2. The collector current I_C depends on β and β is temperature dependent hence I_C also depends on temperature and hence operating point becomes unstable.

(1) For the circuit shown below find (a) I_C (b) V_{CC} (c) β (d) R_B



Solution: Given $R_C = 2.2\,k\Omega$

$I_B = 20\,\mu A$

$V_C = 7.2V$

$I_E = 4mA$

(a) $I_C = ?$ W.K.T $I_E = I_C + I_B$ hence,

$$I_C = I_E - I_B = (4\times10^{-3}) - (20\times10^{-6})$$

$$\boxed{I_C = 3.98mA}$$

(b) $V_{CC} = I_C R_C + V_{CE}$

$$= (3.98\times10^{-3})(2.2\times10^{3}) + 7.2$$

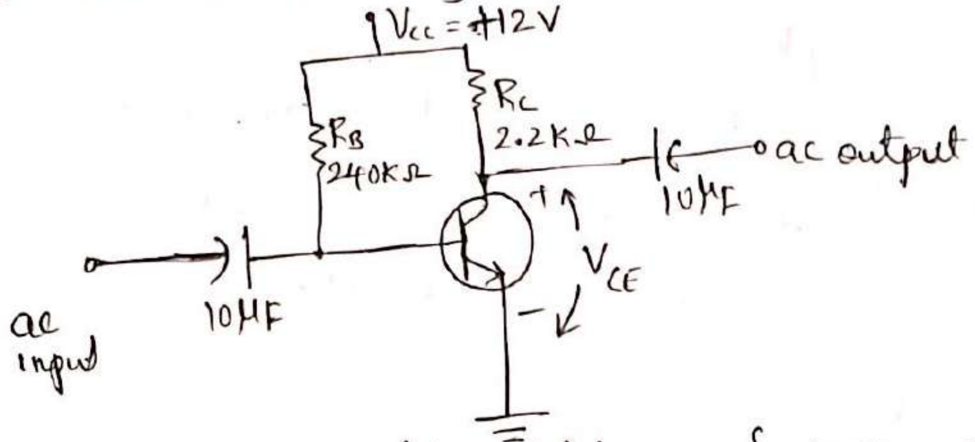
$$\boxed{V_{CC} = 15.956V}$$

(c) $\beta = \dfrac{I_C}{I_B} = \dfrac{3.98\times10^{-3}}{20\times10^{-6}} = 199$

$$\boxed{\beta = 199}$$

(d) $R_B = \dfrac{V_{CC} - V_{BE}}{I_B} = \dfrac{16 - 0.7}{20\times10^{-6}} = 765k\Omega$ $\boxed{R_B = 765k\Omega}$

Q) Determine the following for the fixed-bias configuration.



(a) I_{BQ} and I_{CQ} (c) V_B and V_E. {Assume $\beta = 50$}

(b) V_{CEQ} (d) V_{BC}.

Solution:

(a) $I_{BQ} = \dfrac{V_{cc} - V_{BE}}{R_B} = \dfrac{12 - 0.7}{240K} \doteq 47.08\mu A$

(a) $I_{CQ} = \beta I_{BQ} = (50) \times (47.08\mu A) = 2.35 mA$

(b) $V_{CEQ} = V_{cc} - I_C R_c = 12 - (2.35 mA)(2.2K\Omega)$

$= \underline{6.83V}$

(c) $V_B = V_{BE} = \underline{0.7V}$, $V_C = V_{CE} = \underline{6.83V}$ (Since $V_E = 0$).

(d) $V_{BC} = ?$ Using Double subscription notation we have,

$V_{BC} = V_B - V_c = 0.7 - 6.83 = \underline{-6.13V}$.

(2) Voltage Divider Bias :

In the Fixed bias circuit the Quiescent Value of I_C and V_{CE} are function of dc current gain 'β' & this 'β' is sensitive to temperature and its Value Keep Varying.

The Q-point Values I_C and V_{CE} can be made independent or less independent of 'β' using voltage divider bias configuration.

The voltage divider bias circuit is as shown in below Figure.

In this circuit biasing is provided by three resistors R_1, R_2 & R_E.

The Resistor R_1 and R_2 act as a potential divider giving a Fixed Voltage to point 'B', i.e., Base.

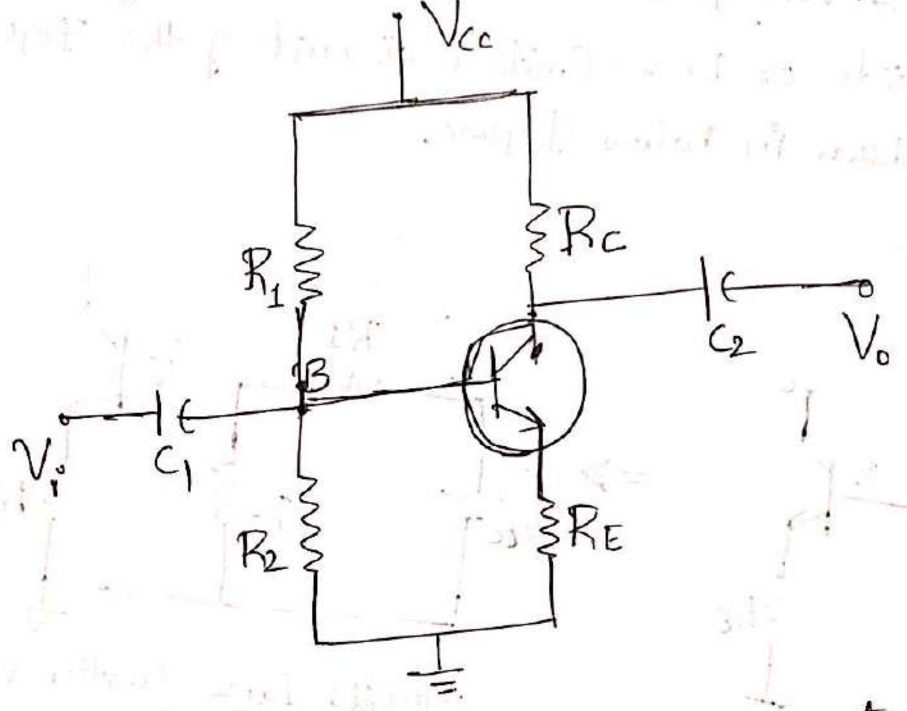


Fig: Voltage Divider Bias circuit

The Voltage divider bias circuit can be analyzed in two methods

(i) Exact Method.

(ii) Approximate Method.

(i) Exact Analysis: The Voltage divider or universal bias circuit is as shown in below Figure.

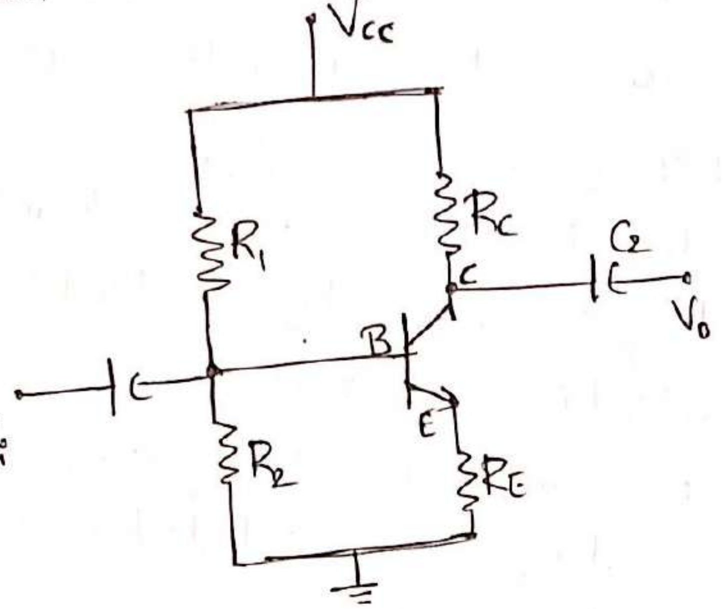


Fig 1: Voltage Divider Bias or Universal Bias

The input side or Base-Emitter circuit of the Figure is drawn as shown in below Figure.

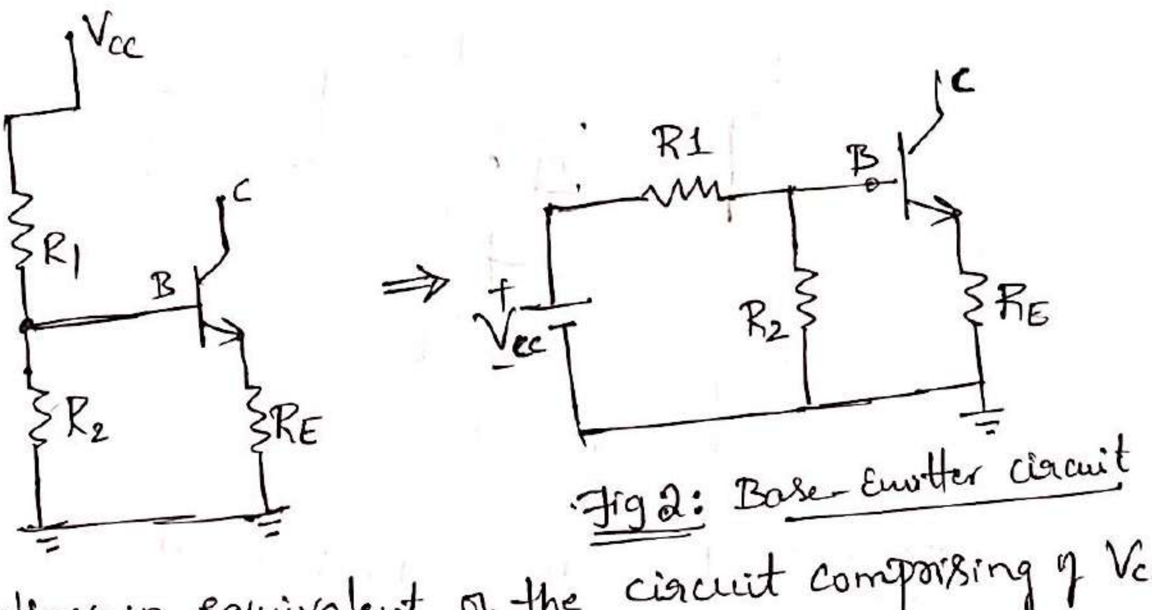
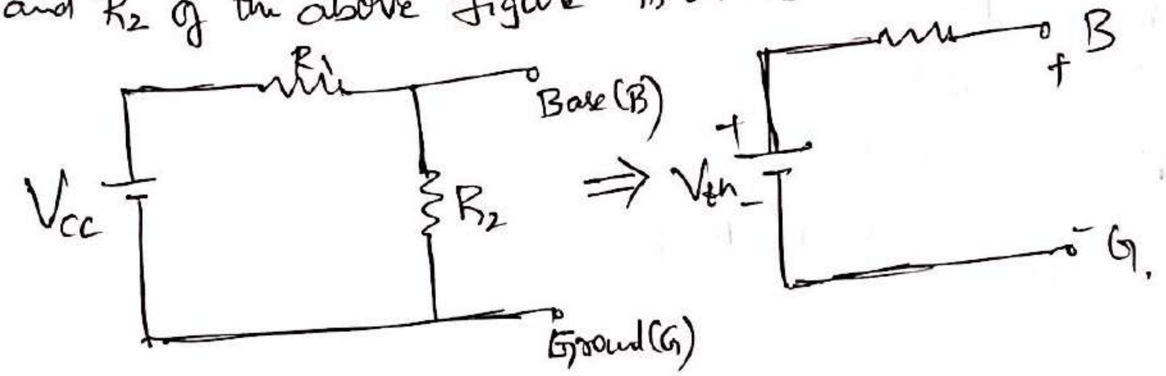
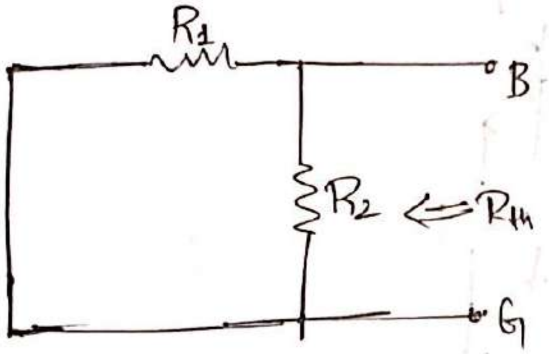


Fig 2: Base-Emitter circuit

The thevnin equivalent of the circuit comprising of V_{CC}, R_1 and R_2 of the above figure is as shown below.



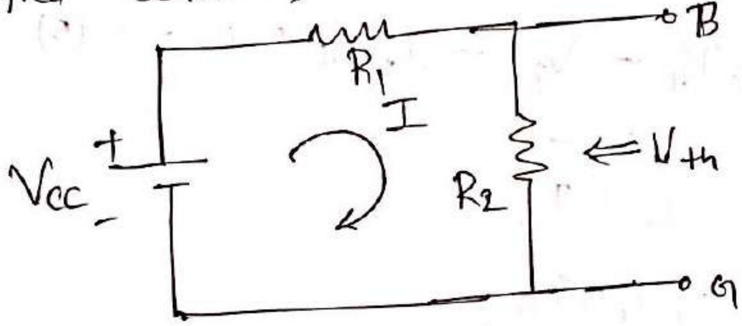
To find R_{th} i.e thevenin resistance, V_{cc} is reduced to zero in the previous circuit.



Since $R_1 \parallel R_2$ the thevnin resistance R_{th} is given by,

$$\boxed{R_{th} = \frac{R_1 R_2}{R_1 + R_2}} \quad \ldots (1)$$

To find V_{th} i.e thevenin voltage consider the below modified circuit,



Apply KVL to the loop we get,

$$V_{cc} - IR_1 - IR_2 = 0$$

$$V_{cc} = I(R_1 + R_2)$$

$$\boxed{I = \frac{V_{cc}}{R_1 + R_2}} \quad \ldots (2)$$

Voltage drop across R_2 is called thevenin voltage V_{th} and is given by

$$\boxed{V_{th} = IR_2} \quad \ldots (3)$$

Substitute equation (3) in equation (2) we get,

$$\boxed{V_{th} = \frac{V_{cc} R_2}{R_1 + R_2}} \quad \ldots (4)$$

The Figure 2 can be redrawn to below equivalent circuit,

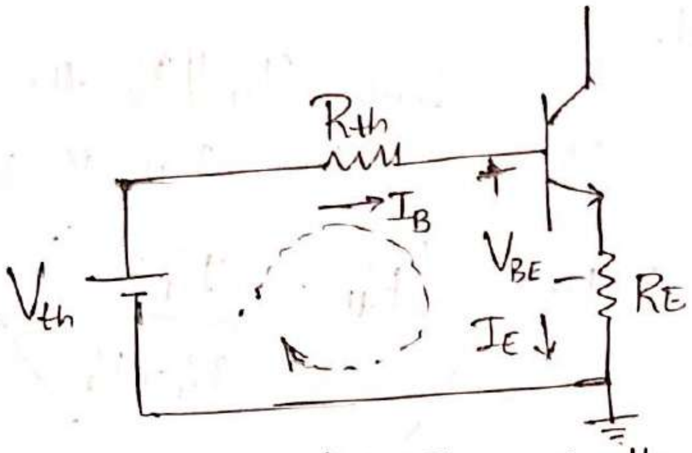


Fig 3: Modified Base-Emitter Loop.

Apply KVL to the above circuit loop, we get,

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0 \quad \ldots (5)$$

w.k.T $\quad I_E = I_c + I_B$

$$= \beta I_B + I_B$$

$$\boxed{I_E = I_B(\beta+1)} \quad \ldots (6)$$

Substituting equation (6) in (5) we get,

$$V_{th} - I_B R_{th} - V_{BE} - I_B(\beta+1)R_E = 0$$

$$V_{th} = I_B\left(R_{th} + (\beta+1)R_E\right) + V_{BE}$$

$$\boxed{I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta+1)R_E}} \quad \ldots (7)$$

The collector current I_c is given by

$$\boxed{I_c = \beta I_B} \quad \ldots (8)$$

Now let us consider common-Emitter section of Figure 1, and is shown as below Figure. 15

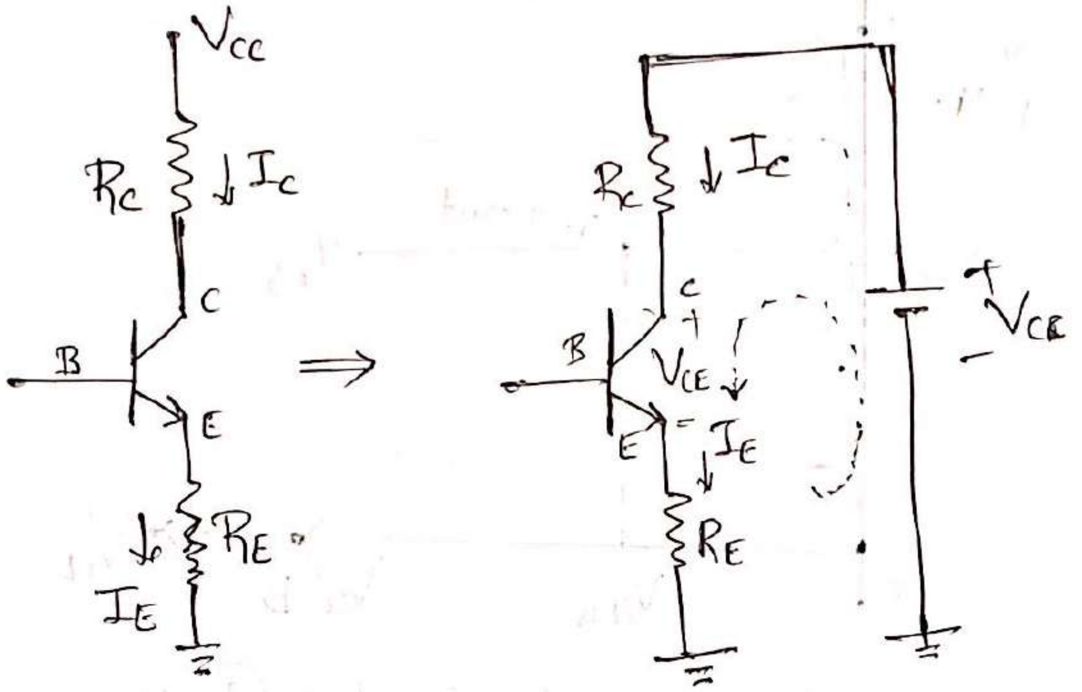


Fig: Common-Emitter Loop.

Apply KVL to circuit

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

w.k.t $I_E \cong I_C$ hence above equation can be written as,

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad \text{......(9)}$$

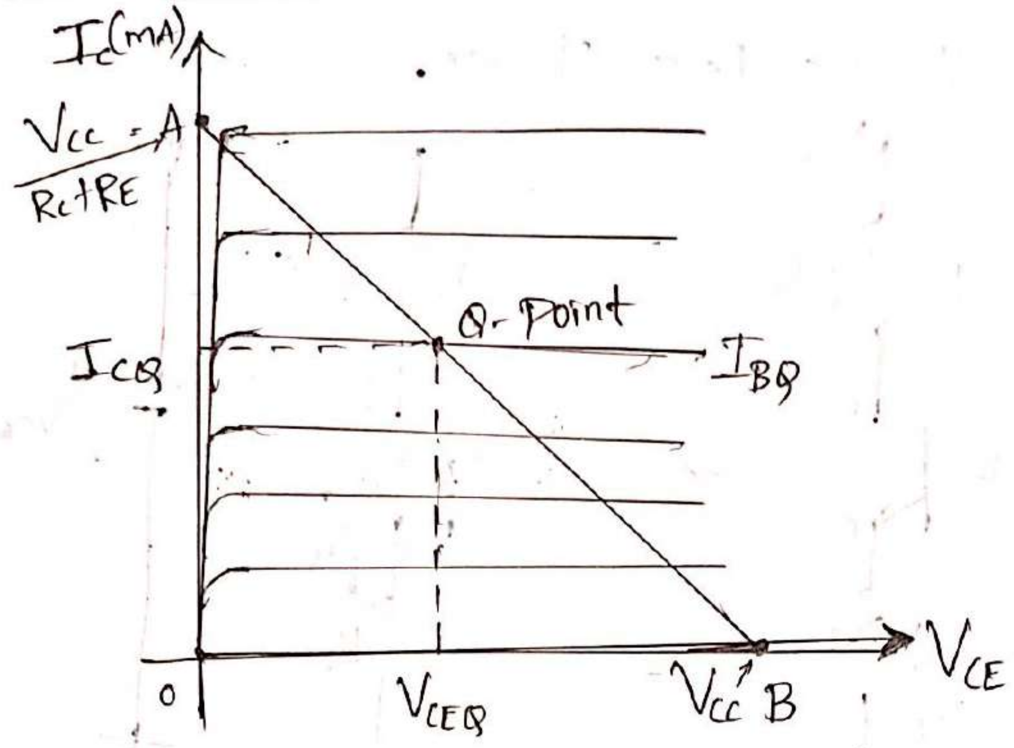
The voltage across Emitter is given by,

$$V_E = I_E R_E \quad \text{......(10)}$$

$$V_C = V_{CE} + V_E \quad \text{......(11)}$$

$$V_B = V_{BE} + V_E \quad \text{......(12)}$$

Load - Line Analysis : (Voltage - Divider Bias Circuit)



To obtain point 'A', consider Equation (9) i.e

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

If $V_{CE} = 0$ V then,

$$V_{CC} = I_C (R_C + R_E)$$

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\Bigg|_{V_{CE}=0}} \quad \text{---} (13)$$

To obtain point 'B',

w.k.t $V_{CE} = V_{CC} - I_C (R_C + R_E)$

If $I_C = 0$ mA then

$$\boxed{V_{CE} = V_{CC}\Big|_{I_C = 0\,mA}} \quad \text{---} (14)$$

* (ii) Approximate Analysis: (Approximate Method)

The input section of the voltage-divider configuration can be represented by the network shown below.

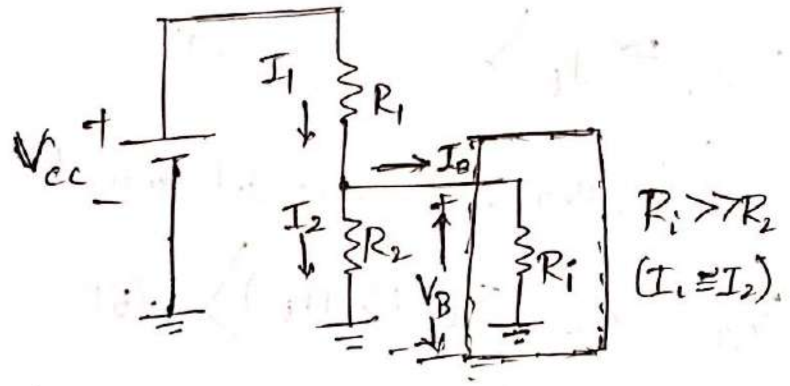


Fig: partial-bias circuit for calculating the base voltage V_B.

The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E.

The reflected resistance between base and emitter is defined by

$R_i = (\beta+1)R_E$.

The voltage across R_2, which is actually the base voltage, can be determined using the voltage divider rule, i.e.,

$$\left\{ V_B = \frac{V_{cc} R_2}{R_1 + R_2} \right\} \quad \cdots (1)$$

Since $R_i = (\beta+1)R_E \cong \beta R_E$ & the approximate condition is given by

$$\langle \beta R_E \geq 10 R_2 \rangle \quad \cdots (2)$$

Once V_B is determined, V_E is given by,

$$\langle V_E = V_B - V_{BE} \rangle \quad \cdots (3)$$

The Emitter current is determined by,

$$\left\langle I_E = \frac{V_E}{R_E} \right\rangle \quad \cdots (4)$$

and

$$\left\langle I_{CQ} \cong I_E \right\rangle \quad \cdots (5)$$

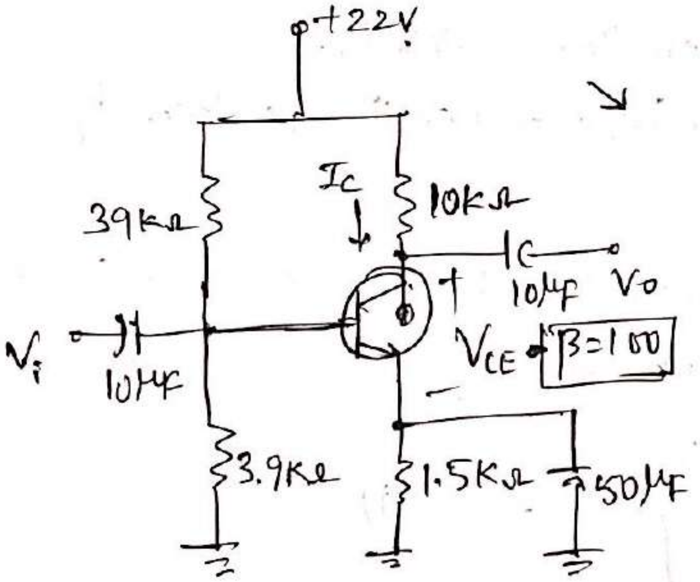
The Collector-to Emitter voltage is determined by,

$$\left\langle V_{CE} = V_{CC} - I_C(R_C + R_E) \right\rangle \quad \cdots (6)$$

Exact Method:

$$\left\{ \begin{array}{l} I_C = 0.84\,mA \\ V_{CE} = 12.34V \end{array} \right\}$$

(1) Approximate Method:



Solution:

$\beta R_E \geq 10 R_2$

$(100)(1.5k) \geq (10)(3.9k\Omega)$

$\langle 150k\Omega \geq 39k\Omega \rangle$

Satisfied.

Then $V_B = \dfrac{R_2 V_{CC}}{R_1 + R_2} = \dfrac{(3.9K)(22V)}{(39K)+(3.9K)\Omega} = 2V$

$V_E = V_B - V_{BE} = 2 - 0.7 = 1.3$

$I_E = \dfrac{V_E}{R_E} = \dfrac{1.3}{1.5k} = 0.867mA$

$I_E \cong I_{CQ} = 0.867mA$

$V_{CEQ} = V_{CC} - I_C(R_C + R_E) = 22V - (0.867mA)(10k\Omega + 1.5k\Omega)$
$= 22V - 9.97V = 12.03V$

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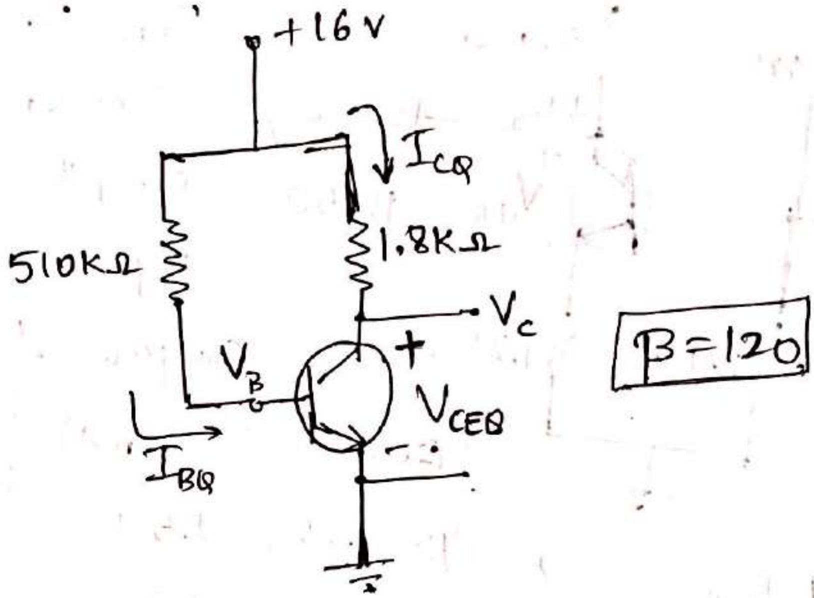
Problems

1. For the fixed-bias configuration of below figure determine

(a) I_{BQ} (b) I_{CQ} (c) V_{CEQ} (d) V_C (e) V_B (f) V_E (19)

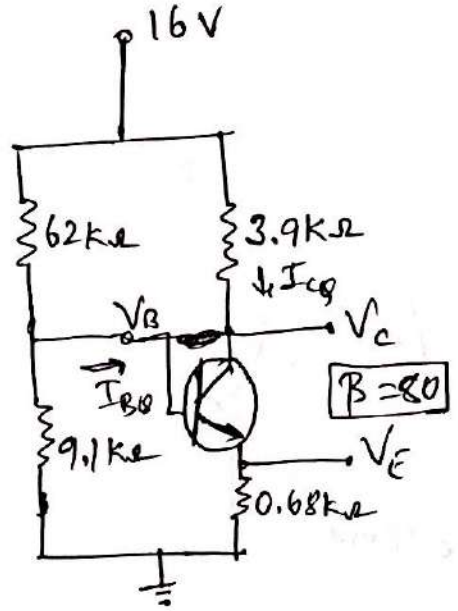


2. For the Voltage-divider bias configuration of below figure determine

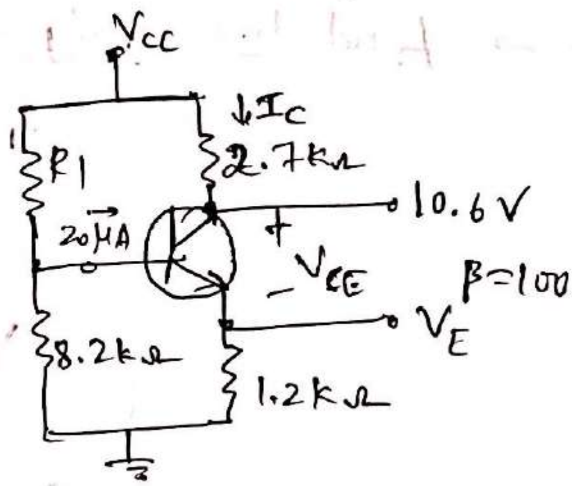
(a) I_{BQ} (b) I_{CQ} (c) V_{CEQ} (d) V_C (e) V_E (f) V_B.

→ Exact Method

→ Approximate Method.



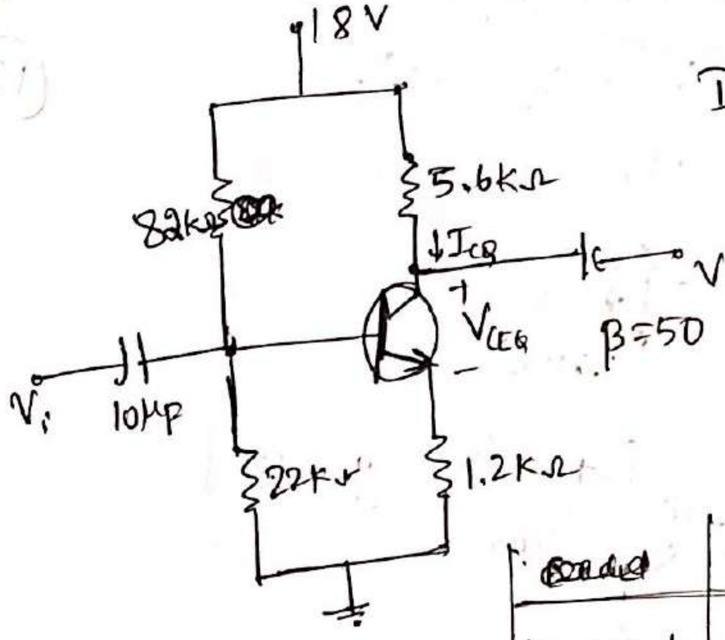
(3) Repeat the problem (2). for $\beta = 140$.



4. Given the information in above figure ↑ determine

(a) I_C (b) V_E (c) V_{CC} (d) V_{CE} (e) V_B (f) R_1.

(5)



Determine the levels of I_{CQ} & V_{CEQ} for the voltage-Divider Configuration using the exact methods & approximate techniques & Compare solutions.

Solution →

	I_{CQ} (mA)	V_{CEQ} (V)
Approximate	2.59	4.54
Exact	1.98	3.88

→ Transistor Saturation: $I_{Csat} = \dfrac{V_{CC}}{R_C + R_E}$

→ Load-line Analysis:

$$\left\{ \begin{aligned} I_C &= \frac{V_{CC}}{R_C + R_E}\Bigg|_{V_{CE}=0} \\ V_{CE} &= V_{CC}\Big|_{I_C = 0\,mA} \end{aligned} \right\}$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

NOTE:

→ Refer Class Notes For the problems.

MODULE-1 PRINCIPLES OF COMBINATION LOGIC

Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-2,3,4variables, Quine-McCluskey Minimization Technique, Quine-McCluskey using don't care terms.

1.1 COMBINATIONAL LOGIC

Introduction Logic circuit may be classified into two categories

1. Combinational logic circuits

2. Sequential logic circuits

A combinational logic circuit contains logic gates only but does not contain storage elements. A sequential logic circuit contains storage elements in addition to logic gates. When logic gates are connected together to give a specified output for certain specified combination of input variables, with no storage involved, the resulting network is known as combinational logic circuit.

In combinational logic circuit the output level is at all times dependent on the combination of input level. The block diagram is shown

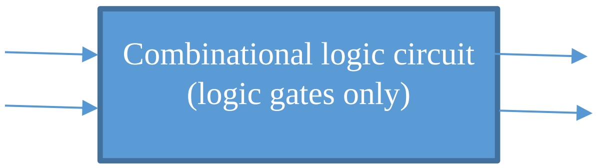


Fig : Block diagram of Combinational circuit

The combinational logic circuit with memory elements(s) is called sequential logic circuit. It consists of a combinational circuit to which memory elements are connected to form a feedback path. The memory elements are devices, capable of storing binary information within them. The block diagram is shown.

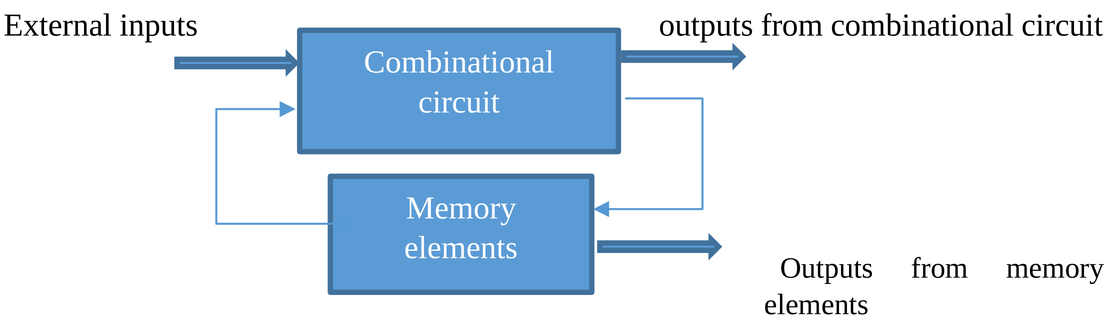


Fig : Block diagram of Sequential circuit

By block diagram, it can be said that the output(s) of sequential logic circuit is (are) dependent not only on external input(s) but also on the present state of the memory element(s). The next state of the memory element(s) is also dependent on external input and the present state. Applications Logic gates find wide applications in Calculators and computers, digital measuring techniques, digital processing of communications, musical instruments, games and domestic appliances etc, for decision making in automatic control of machines and various industrial processes and for building more complex devices such as binary counters etc.

Laws and Rules of Boolean Algebra

- Laws of Boolean Algebra

The basic laws of Boolean algebra-the commutative laws for addition and multiplication, the associative laws for addition and multiplication, and the distributive law-are the same as in ordinary algebra.

The commutative law A+B = B+A

A.B = B.A

The associative law A + (B + C) = (A + B) + C

A(BC) = (AB)C

Distributive Law A(B + C) = AB + AC

- Rules of Boolean Algebra

1. $A + 0 = A$	**7.** $A \cdot A = A$
2. $A + 1 = 1$	**8.** $A \cdot \overline{A} = 0$
3. $A \cdot 0 = 0$	**9.** $\overline{\overline{A}} = A$
4. $A \cdot 1 = A$	**10.** $A + AB = A$
5. $A + A = A$	**11.** $A + \overline{A}B = A + B$
6. $A + \overline{A} = 1$	**12.** $(A + B)(A + C) = A + BC$

A, B, or C can represent a single variable or a combination of variables.

(Referring to the table above)

Proof Rule 10: A + AB = A

This rule can be proved by applying the distributive law, rule 2, and rule 4 as follows:

A + AB = A (1 + B) Factoring (distributive law)

= A. l Rule 2: (1 + B) = 1

= A Rule 4: A. 1 = A

Rule 11.
A + AB = A + B
This rule can be proved as follows:
A + AB = (A + AB) + AB Rule 10: A = A + AB

= (AA + AB) + AB Rule 7: A = AA
=AA +AB +AA +AB Rule 8: adding AA = 0
= (A + A) (A + B) Factoring
= 1. (A + B) Rule 6: A + A = 1
=A + B Rule 4: drop the 1

Rule 12. (A + B) (A + C) = A + BC
This rule can be proved as follows:
(A + B) (A + C) = AA + AC + AB + BC Distributive law
= A + AC + AB + BC Rule 7: AA = A
= A (1 + C) + AB + BC Rule 2: 1 + C = 1
= A. 1 + AB + BC Factoring (distributive law)
= A (1 + B) + BC Rule 2: 1 + B = 1
= A. 1 + BC Rule 4: A. 1 = A
= A + BC

DEMORGAN'S THEOREMS

The complement of a product of variables is equal to the sum of the individual complements of the variables.

$$\overline{X.Y} = \bar{X} + \bar{Y}$$

The complement of a sum of variables is equal to the product of the individual complements of the variables.

$$\overline{X+Y} = \bar{X}.\bar{Y}$$

1.2. CANONICAL FORMS AND NORMAL FORMS

We will get four Boolean product terms by combining two variables x and y with logical AND operation. These Boolean product terms are called as **min terms** or **standard product terms**. The min terms are x'y', x'y, xy' and xy.

Similarly, we will get four Boolean sum terms by combining two variables x and y with logical OR operation. These Boolean sum terms are called as **Max terms** or **standard sum terms**. The Max terms are x+y, x+y', x'+y and x'+y'.

The following table shows the representation of min terms and MAX terms for 2 variables.

x	y	Min terms	Max terms
0	0	m_0=x'y'	M_0=x+y
0	1	m_1=x'y	M_1=x+y'
1	0	m_2=xy'	M_2=x'+y

1	1	$m_3=xy$	$M_3=x'+y'$

If the binary variable is ‘0’, then it is represented as complement of variable in min term and as the variable itself in Max term. Similarly, if the binary variable is ‘1’, then it is represented as complement of variable in Max term and as the variable itself in min term.

From the above table, we can easily notice that min terms and Max terms are complement of each other. If there are ‘n’ Boolean variables, then there will be 2^n min terms and 2^n Max terms.

1.3 GENERATION OF SWITCHING EQUATION FROM TRUTH TABLE

Canonical SoP and PoS forms

A truth table consists of a set of inputs and output(s). If there are ‘n’ input variables, then there will be 2^n possible combinations with zeros and ones. So the value of each output variable depends on the combination of input variables. So, each output variable will have ‘1’ for some combination of input variables and ‘0’ for some other combination of input variables.

Therefore, we can express each output variable in following two ways.

- Canonical SoP form
- Canonical PoS form

Canonical SoP form (Minterm canonical form)

Canonical SoP form means Canonical Sum of Products form. In this form, each product term contains all literals. So, these product terms are nothing but the min terms. Hence, canonical SoP form is also called as **sum of min terms** form.

First, identify the min terms for which, the output variable is one and then do the logical OR of those min terms in order to get the Boolean expression (function) corresponding to that output variable. This Boolean function will be in the form of sum of min terms.

Follow the same procedure for other output variables also, if there is more than one output variable.

Example:

Consider the following **truth table**.

Inputs			**Output**
p	**q**	**r**	**F**
0	0	0	0

0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Here, the output (f) is ‘1’ for four combinations of inputs. The corresponding min terms are p’qr, pq’r, pqr’, pqr. By doing logical OR of these four min terms, we will get the Boolean function of output (f).

Therefore, the Boolean function of output is, f=p’qr + pq’r + pqr’ + pqr. This is the **canonical SoP form** of output, f. We can also represent this function in following two notations.

f=m3+m5+m6+m7

f=∑m(3,5,6,7)

In one equation, we represented the function as sum of respective min terms. In other equation, we used the symbol for summation of those min terms.

Canonical PoS form (Maxterm canonical form)

Canonical PoS form means Canonical Product of Sums form. In this form, each sum term contains all literals. So, these sum terms are nothing but the Max terms. Hence, canonical PoS form is also called as **product of Max terms** form.

First, identify the Max terms for which, the output variable is zero and then do the logical AND of those Max terms in order to get the Boolean expression (function) corresponding to that output variable. This Boolean function will be in the form of product of Max terms.

Follow the same procedure for other output variables also, if there is more than one output variable.

Example

Consider the same truth table of previous example. Here, the output (f) is ‘0’ for four combinations of inputs. The corresponding Max terms are p+q+r, p+q+r’, p+q’+r, p’+q+r. By doing logical AND of these four Max terms, we will get the Boolean function of output (f).

Therefore, the Boolean function of output is, f=(p+q+r).(p+q+r’).(p+q’+r).(p’+q+r). This is the **canonical PoS form** of output, f. We can also represent this function in following two notations.

f=M0.M1.M2.M4

f=∏M(0,1,2,4)

In one equation, we represented the function as product of respective Max terms. In other equation, we used the symbol for multiplication of those Max terms.

The Boolean function, f=(p+q+r).(p+q+r’).(p+q’+r).(p’+q+r) is the dual of the Boolean function, f=p’qr + pq’r + pqr’ + pqr.

Therefore, both canonical SoP and canonical PoS forms are **Dual** to each other. Functionally, these two forms are same. Based on the requirement, we can use one of these two forms.

Standard SoP and PoS forms

We discussed two canonical forms of representing the Boolean output(s). Similarly, there are two standard forms of representing the Boolean output(s). These are the simplified version of canonical forms.

- Standard SoP form
- Standard PoS form

We will discuss about Logic gates in later chapters. The main **advantage** of standard forms is that the number of inputs applied to logic gates can be minimized. Sometimes, there will be reduction in the total number of logic gates required.

Standard SoP form

Standard SoP form means **Standard Sum of Products** form. In this form, each product term need not contain all literals. So, the product terms may or may not be the min terms. Therefore, the Standard SoP form is the simplified form of canonical SoP form.

We will get Standard SoP form of output variable in two steps.

- Get the canonical SoP form of output variable
- Simplify the above Boolean function, which is in canonical SoP form.

Follow the same procedure for other output variables also, if there is more than one output variable. Sometimes, it may not possible to simplify the canonical SoP form. In that case, both canonical and standard SoP forms are same.

Example

Convert the following Boolean function into Standard SoP form.

$$f=p'qr + pq'r + pqr' + pqr$$

The given Boolean function is in canonical SoP form. Now, we have to simplify this Boolean function in order to get standard SoP form.

Step 1 − Use the **Boolean postulate**, x + x = x. That means, the Logical OR operation with any Boolean variable 'n' times will be equal to the same variable. So, we can write the last term pqr two more times.

$$\Rightarrow f= p'qr + pq'r + pqr' + pqr + pqr + pqr$$

Step 2 − Use **Distributive law** for 1st and 4th terms, 2nd and 5th terms, 3rd and 6th terms.

$$\Rightarrow f= qr(p' + p) + pr(q'+q) + pq(r'+r)$$

Step 3 − Use **Boolean postulate**, x + x' = 1 for simplifying the terms present in each parenthesis.

$$\Rightarrow f= qr(1) + pr(1) + pq(1)$$

Step 4 − Use **Boolean postulate**, x.1 = x for simplifying above three terms.

$$\Rightarrow f= qr + pr + pq$$

$$\Rightarrow f= pq + qr + pr$$

This is the simplified Boolean function. Therefore, the **standard SoP form**corresponding to given canonical SoP form is **f= pq + qr + pr**

Standard PoS form

Standard PoS form means **Standard Product of Sums** form. In this form, each sum term need not contain all literals. So, the sum terms may or may not be the Max terms. Therefore, the Standard PoS form is the simplified form of canonical PoS form.

We will get Standard PoS form of output variable in two steps.

- Get the canonical PoS form of output variable
- Simplify the above Boolean function, which is in canonical PoS form.

Follow the same procedure for other output variables also, if there is more than one output variable. Sometimes, it may not possible to simplify the canonical PoS form. In that case, both canonical and standard PoS forms are same.

Example

Convert the following Boolean function into Standard PoS form.

$$f=(p+q+r).(p+q+r').(p+q'+r).(p'+q+r)$$

The given Boolean function is in canonical PoS form. Now, we have to simplify this Boolean function in order to get standard PoS form.

Step 1 − Use the **Boolean postulate**, x.x=x. That means, the Logical AND operation with any Boolean variable 'n' times will be equal to the same variable. So, we can write the first term p+q+r two more times.

$$\Rightarrow f=(p+q+r).(p+q+r).(p+q+r).(p+q+r').(p+q'+r).(p'+q+r)$$

Step 2 − Use **Distributive law,** x + (y.z) = (x+y).(x+z) for 1st and 4thparenthesis, 2nd and 5th parenthesis, 3rd and 6th parenthesis.

$$\Rightarrow f=(p+q+rr').(p+r+qq').(q+r+pp')$$

Step 3 − Use **Boolean postulate**, x.x'=0 for simplifying the terms present in each parenthesis.

$$\Rightarrow f=(p+q+0).(p+r+0).(q+r+0)$$

Step 4 − Use **Boolean postulate**, x+0=x for simplifying the terms present in each parenthesis

$$\Rightarrow f=(p+q).(p+r).(q+r)$$

$$\Rightarrow f=(p+q).(q+r).(p+r)$$

This is the simplified Boolean function. Therefore, the **standard PoS form**corresponding to given canonical PoS form is **f=(p+q).(q+r).(p+r)**. This is the **dual** of the Boolean function, f=pq+qr+pr.

Therefore, both Standard SoP and Standard PoS forms are Dual to each other.

1.4. K-MAPS FOR 2 TO 5 VARIABLES

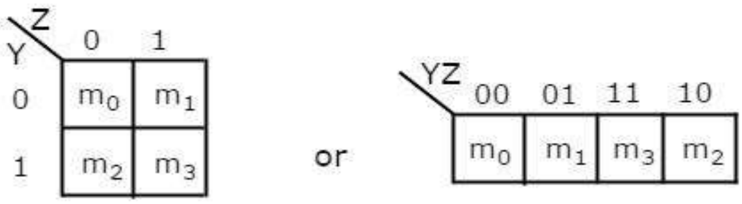
We have simplified the Boolean functions using Boolean postulates and theorems. It is a time-consuming process and we have to re-write the simplified expressions after each step.

To overcome this difficulty, **Karnaugh** introduced a method for simplification of Boolean functions in an easy way. This method is known as Karnaugh map method or K-map method. It is a graphical method, which consists of 2^n cells for 'n' variables. The adjacent cells are differed only in single bit position.

K-Map method is most suitable for minimizing Boolean functions of 2 variables to 5 variables. Now, let us discuss about the K-Maps for 2 to 5 variables one by one.

2 Variable K-Map

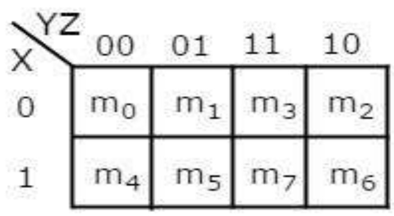
The number of cells in 2 variable K-map is four, since the number of variables is two. The following figure shows **2 variable K-Map**.



- There is only one possibility of grouping 4 adjacent min terms.
- The possible combinations of grouping 2 adjacent min terms are {(m_0, m_1), (m_2, m_3), (m_0, m_2) and (m_1, m_3)}.

3 Variable K-Map

The number of cells in 3 variable K-map is eight, since the number of variables is three. The following figure shows **3 variable K-Map**.



- There is only one possibility of grouping 8 adjacent min terms.
- The possible combinations of grouping 4 adjacent min terms are {(m_0, m_1, m_3, m_2), (m_4, m_5, m_7, m_6), (m_0, m_1, m_4, m_5), (m_1, m_3, m_5, m_7), (m_3, m_2, m_7, m_6) and (m_2, m_0, m_6, m_4)}.
- The possible combinations of grouping 2 adjacent min terms are {(m_0, m_1), (m_1, m_3), (m_3, m_2), (m_2, m_0), (m_4, m_5), (m_5, m_7), (m_7, m_6), (m_6, m_4), (m_0, m_4), (m_1, m_5), (m_3, m_7) and (m_2, m_6)}.
- If x=0, then 3 variable K-map becomes 2 variable K-map.

4 Variable K-Map

The number of cells in 4 variable K-map is sixteen, since the number of variables is four. The following figure shows **4 variable K-Map**.

WX \ YZ	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

- There is only one possibility of grouping 16 adjacent min terms.
- Let R_1, R_2, R_3 and R_4 represents the min terms of first row, second row, third row and fourth row respectively. Similarly, C_1, C_2, C_3 and C_4represents the min terms of first column, second column, third column and fourth column respectively. The possible combinations of grouping 8 adjacent min terms are {(R_1, R_2), (R_2, R_3), (R_3, R_4), (R_4, R_1), (C_1, C_2), (C_2, C_3), (C_3, C_4), (C_4, C_1)}.
- If w=0, then 4 variable K-map becomes 3 variable K-map.

Minimization of Boolean Functions using K-Maps

If we consider the combination of inputs for which the Boolean function is '1', then we will get the Boolean function, which is in **standard sum of products** form after simplifying the K-map.

Similarly, if we consider the combination of inputs for which the Boolean function is '0', then we will get the Boolean function, which is in **standard product of sums** form after simplifying the K-map.

Follow these **rules for simplifying K-maps** in order to get standard sum of products form.

- Select the respective K-map based on the number of variables present in the Boolean function.
- If the Boolean function is given as sum of min terms form, then place the ones at respective min term cells in the K-map. If the Boolean function is given as sum of products form, then place the ones in all possible cells of K-map for which the given product terms are valid.

- Check for the possibilities of grouping maximum number of adjacent ones. It should be powers of two. Start from highest power of two and upto least power of two. Highest power is equal to the number of variables considered in K-map and least power is zero.

- Each grouping will give either a literal or one product term. It is known as **prime implicant**. The prime implicant is said to be **essential prime implicant**, if atleast single '1' is not covered with any other groupings but only that grouping covers.

- Note down all the prime implicants and essential prime implicants. The simplified Boolean function contains all essential prime implicants and only the required prime implicants.

Note 1 − If outputs are not defined for some combination of inputs, then those output values will be represented with **don't care symbol 'x'**. That means, we can consider them as either '0' or '1'. **Note 2** − If don't care terms also present, then place don't cares 'x' in the respective cells of K-map. Consider only the don't cares 'x' that are helpful for grouping maximum number of adjacent ones. In those cases, treat the don't care value as '1'.

1.5. THE TABULATION METHOD (QUINE-MC CLUSKEY ALGORITHM)

For function of five or more variables, it is difficult to be sure that the best selection is made. In such case, the tabulation method can be used to overcome such difficulty. The tabulation method was first formulated by Quine and later improved by McCluskey. It is also known as Quine-McCluskey method.

The Quine–McCluskey algorithm (or the method of prime implicants) is a method used for minimization of boolean functions. It is functionally identical to Karnaugh mapping, but the tabular form makes it more efficient for use in computer algorithms, and it also gives a deterministic way to check that the minimal form of a Boolean function has been reached.

The method involves two steps:

- Finding all prime implicants of the function.
- Use those prime implicants in a prime implicant chart to find the essential prime implicants of the function, as well as other prime implicants that are necessary to cover the function.

Finding prime implicants : Minimizing an arbitrary function:

	A B C D	f
m0	0 0 0 0	0
m1	0 0 0 1	0
m2	0 0 1 0	0
m3	0 0 1 1	0
m4	0 1 0 0	1
m5	0 1 0 1	0
m6	0 1 1 0	0
m7	0 1 1 1	0
m8	1 0 0 0	1
m9	1 0 0 1	x
m10	1 0 1 0	1
m11	1 0 1 1	1
m12	1 1 0 0	1
m13	1 1 0 1	0
m14	1 1 1 0	x
m15	1 1 1 1	1

One can easily form the canonical sum of products expression from this table, simply by summing the minterms (leaving out don't-care terms) where the function evaluates to one:

F(A,B,C,D) = A′BC′D′ + AB′C′D′ + AB′CD′ + AB′CD + ABC′D′ + ABCD

Of course, that's certainly not minimal. So to optimize, all minterms that evaluate to one are first placed in a minterm table. Don't-care terms are also added into this table, so they can be combined with minterms:

Number of 1s	Minterm	Binary Representation
1	m4	0100
	m8	1000
2	m9	1001
	m10	1010
	m12	1100
3	m11	1011
	m14	1110
4	m15	1111

At this point, one can start combining minterms with other minterms. If two terms vary by only a single digit changing, that digit can be replaced with a dash indicating that the digit doesn't matter. Terms that can't be combined any more are marked with a "*". When going from Size 2 to Size 4, treat '-' as a third bit value. Ex: -110 and -100 or -11- can be combined, but not -110 and 011-. (Trick: Match up the '-' first.)

```
Number of 1s  Minterm  0-Cube       | Size 2 Implicants     | Size 4 Implicants
------------------------------      |-------------------    |----------------------
1             m4       0100         | m(4,12)  -100*        | m(8,9,10,11)   10--*
              m8       1000         | m(8,9)   100-         | m(8,10,12,14)  1--0*
------------------------------      | m(8,10)  10-0         |----------------------
2             m9       1001         | m(8,12)  1-00         | m(10,11,14,15) 1-1-*
              m10      1010         |----------------------  |
              m12      1100         | m(9,11)  10-1         |
------------------------------      | m(10,11) 101-         |
3             m11      1011         | m(10,14) 1-10         |
              m14      1110         | m(12,14) 11-0         |
------------------------------      |-------------------    |
4             m15      1111         | m(11,15) 1-11         |
                                    | m(14,15) 111-         |
```

At this point, the terms marked with * can be seen as a solution. That is the solution is

F=AB′+AD′+AC+BC′D′

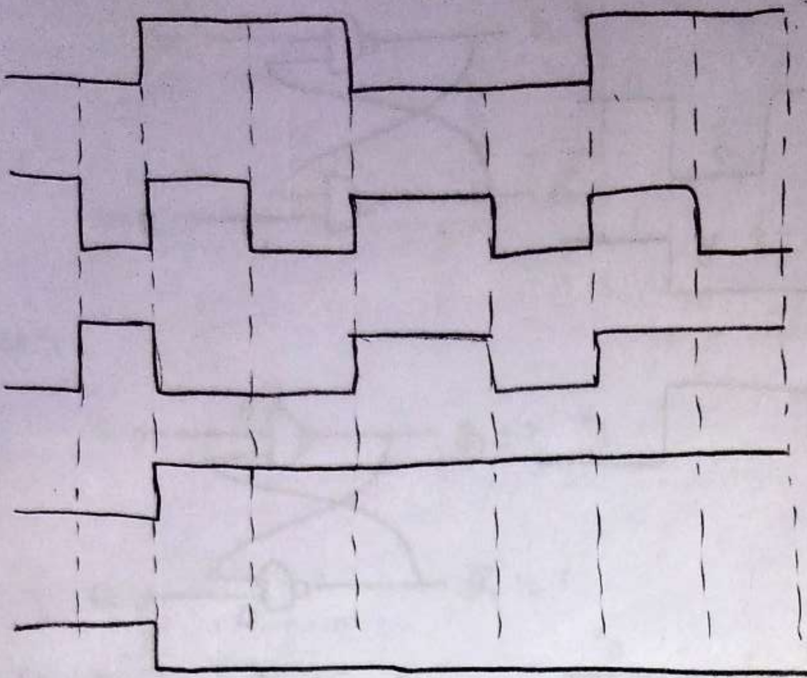
If the karnaugh map was used, we should have obtain an expression simplier than this.

Prime implicant chart

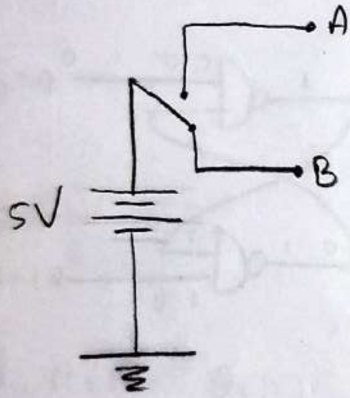
None of the terms can be combined any further than this, so at this point we construct an essential prime implicant table. Along the side goes the prime implicants that have just been generated, and along the top go the minterms specified earlier. The don't care terms are not placed on top - they are omitted from this section because they are not necessary inputs.

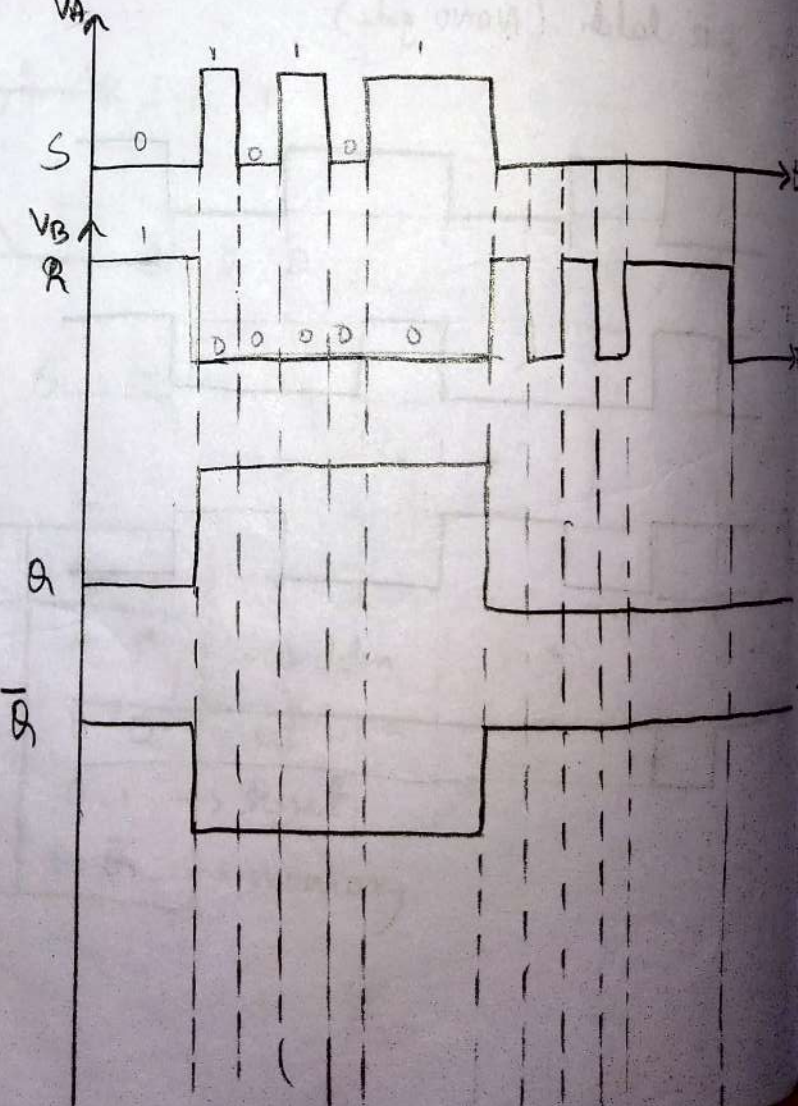
	4	8	10	11	12	15	
m(4,12)	X				X		-100 (BC′D′)
m(8,9,10,11)		X	X	X			10--(AB′)
m(8,10,12,14)		X	X		X		1--0 (AD′)
m(10,11,14,15)			X	X		X	1-1- (AC)

Gated SR latch :-

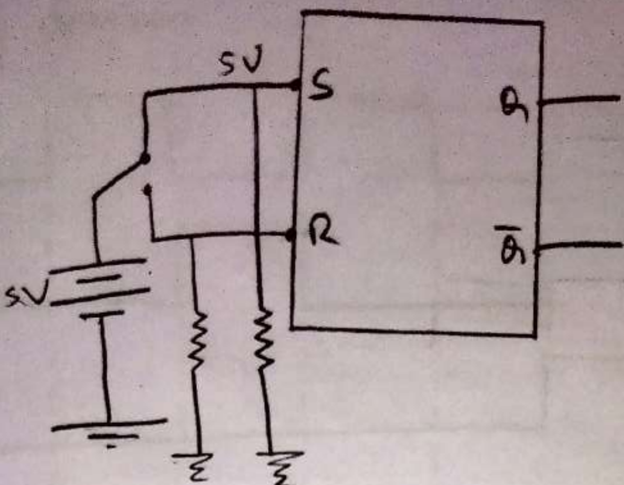


** Switch de-bounces [Application of S-R latch] :-



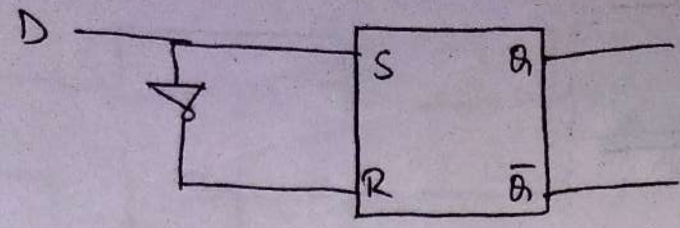


S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	forbidden	

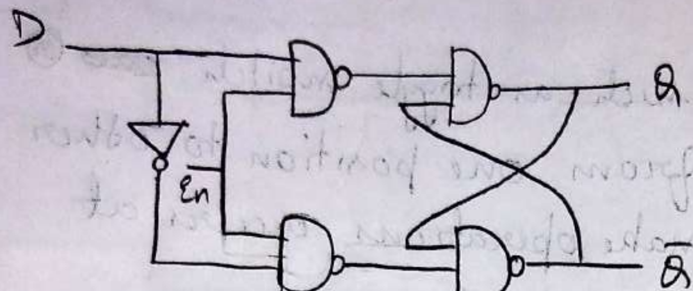


* When a mechanical switches such as toggle switch (or) push buttons are switched from one position to other several break and make operations occurs at second position is called switch de-bounce.
* When centre contact is moved from B to A at time t_1 the voltage at B is 0volts as soon as it leaves the terminal B however when it touches A terminal serval make and break operation (bouncing operation) takes place due to the spring like nature of the contact.
* A similar occurrance can be seen at B terminal when the centre contact is moved from A to B ~~at time~~ resulting waveform is as shown in the figure. These effect is called switch bounce.
* Such a switch bounce can be eliminated by using SR latch.

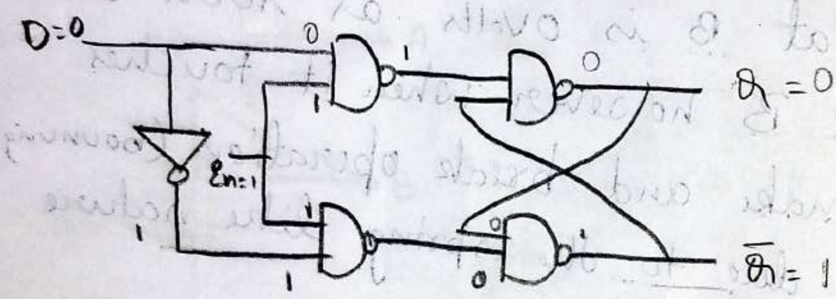
6)a D-latch:



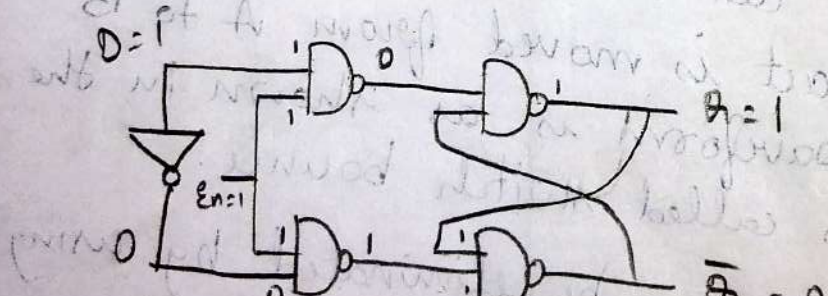
Symbol.



Case 1:- $En = 1$ $D = 0$ $Q = 0$ $\bar{Q} = 1$



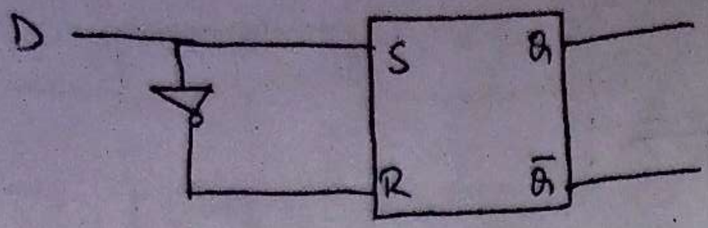
Case 2:- $En = 1$ $D = 1$ $Q = 1$ $\bar{Q} = 0$



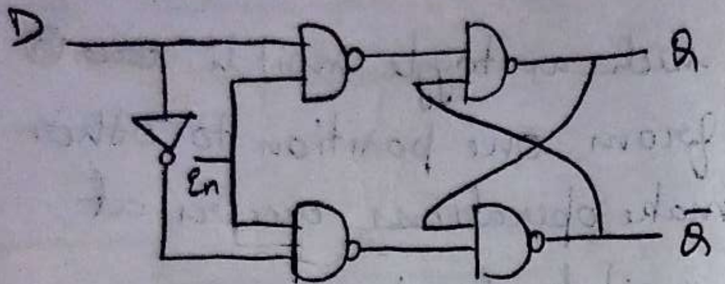
Truth table

En	D	Q	$\bar{Q}$
0	x	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

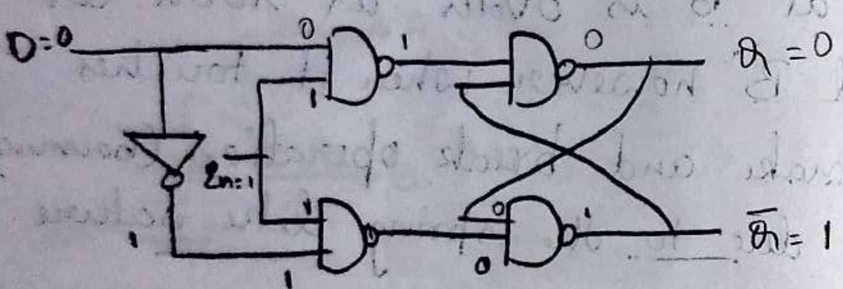
D-latch:



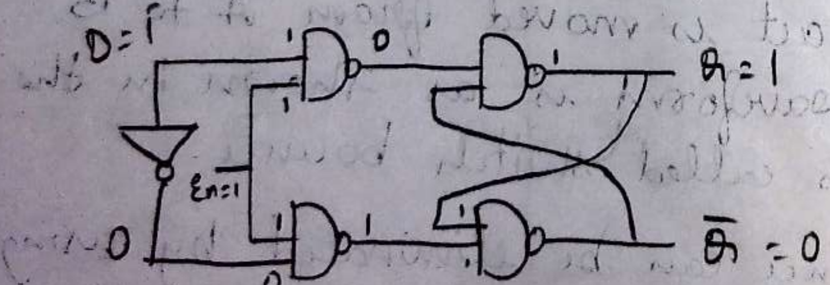
Symbol.



Case 1 :- $En = 1$; $D = 0$; $Q = 0$; $\bar{Q} = 1$



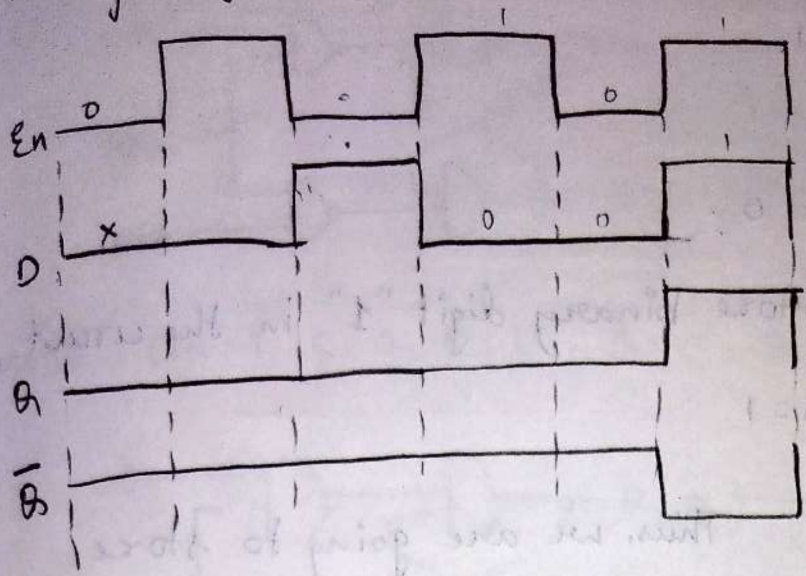
Case 2 :- $En = 1$; $D = 1$; $Q = 1$; $\bar{Q} = 0$

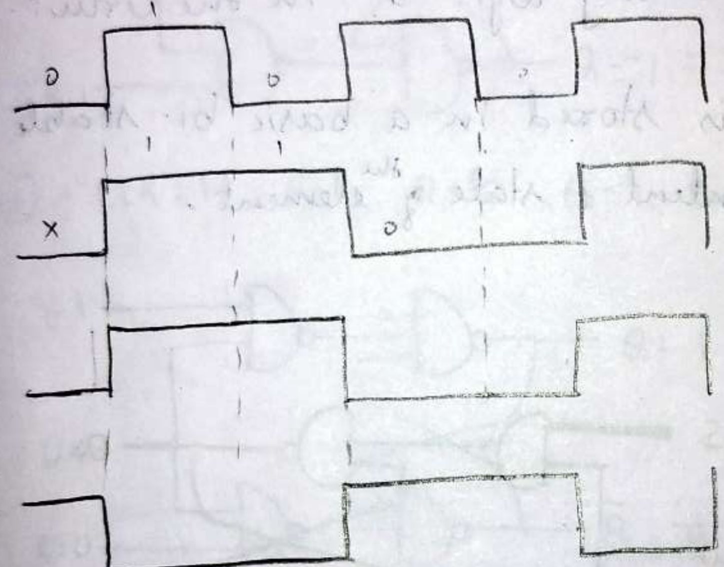


Truth table

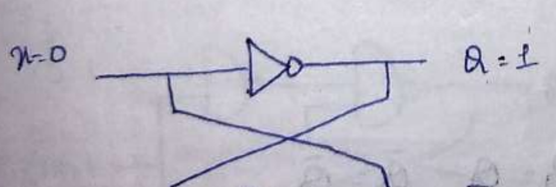
En	D	Q	$\bar{Q}$
0	X	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

Timing diagram :-





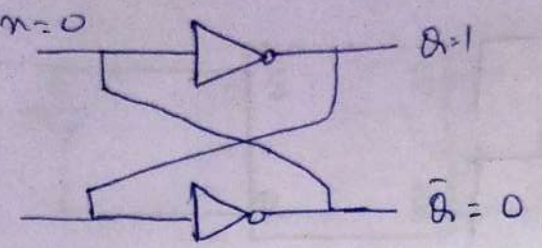
Basic bi-stable element :-



~~case~~ desc:- The basic bi-stable element is a circuit having two stable state the logical diagram is as shown. The circuit has two output's Q & $\bar{Q}$.

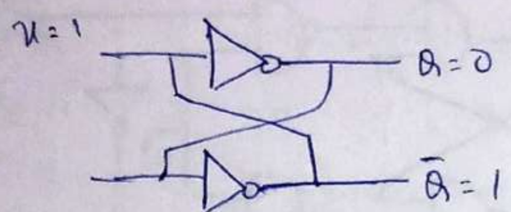
Working:-

Case 1 :- if $x = 0$, $Q = 1$ $\bar{Q} = 0$



Thus, we are going to store binary digit "1" in the circuit.

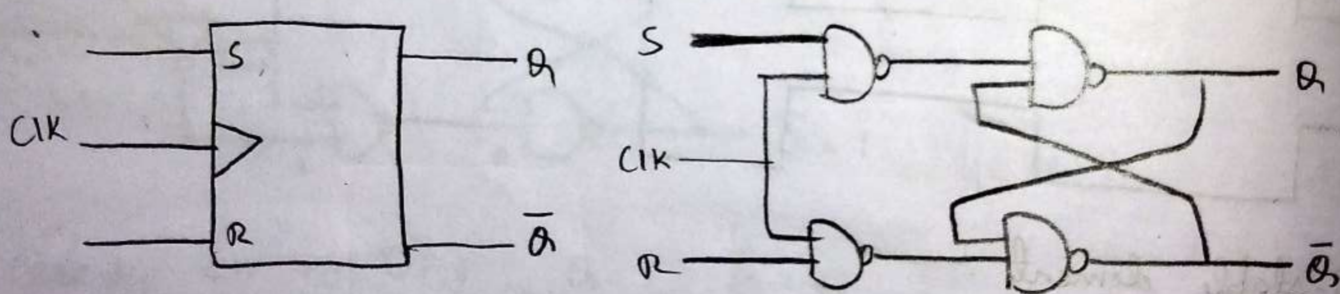
Case 2 :- if $x = 1$, $Q = 0$. $\bar{Q} = 1$



Thus, we are going to store binary digit "0" in the circuit.

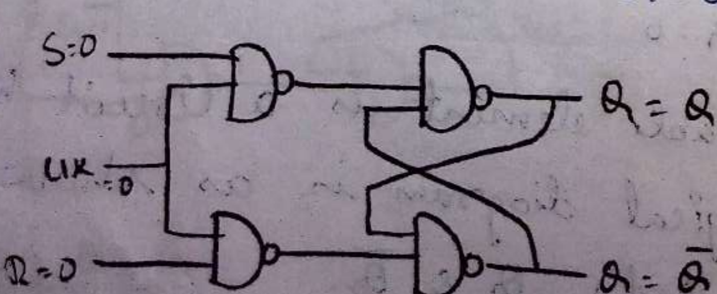
The binary digit 0 or 1 is stored in a basic bi-stable element is known as Content / state of the element.

SR flip flop :-



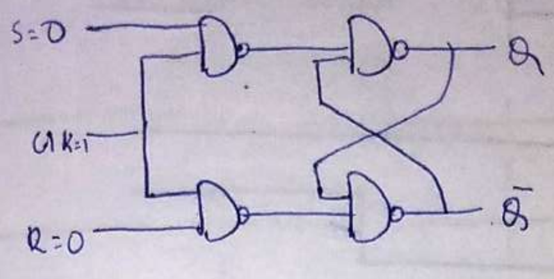
Symbol

Case ① :- $Clk = 0$, $S = 0$. $R = 0$ $Q = Q$ $\bar{Q} = \bar{Q}$

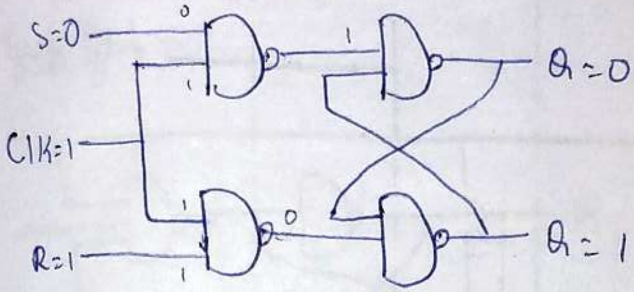


Flip-Flop is said to be previous state.

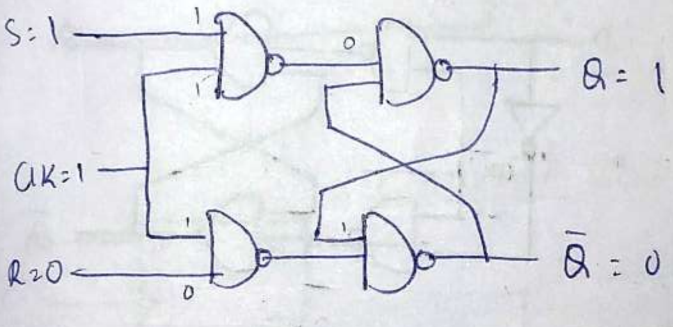
case (ii) :- Clk = 1, S = 0, R = 0 · $Q = Q$, $\bar{Q} = \bar{Q}$



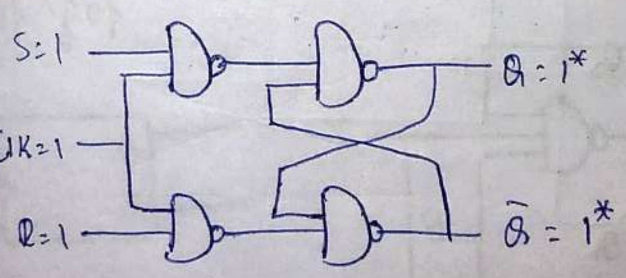
case (iii) :- Clk = 1, S = 0, R = 1 $Q = 0$, $\bar{Q} = 1$



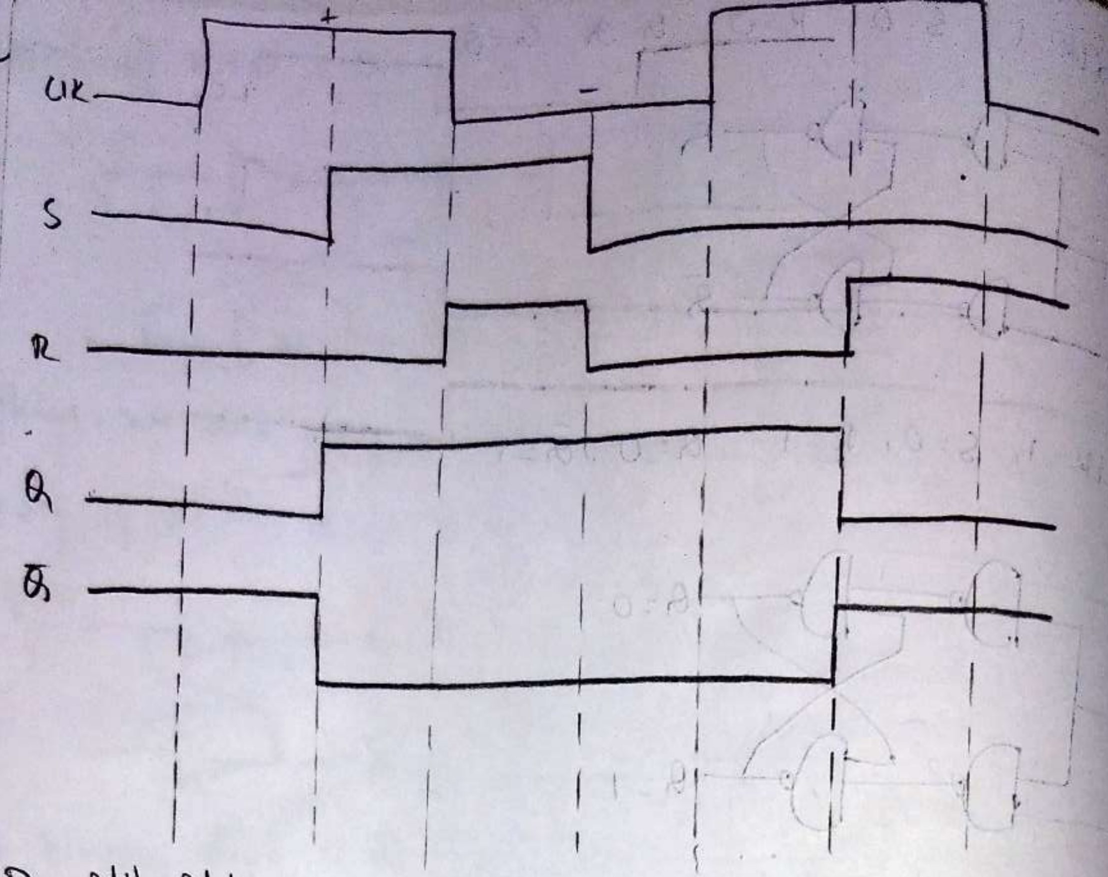
case (iv) :- Clk = 1, S = 1, R = 0 $Q = 1$, $\bar{Q} = 0$



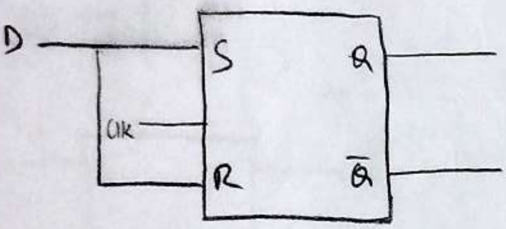
case (v) :- Clk = 1, S = 1, R = 1 $Q = 1^*$ $\bar{Q} = 1^*$

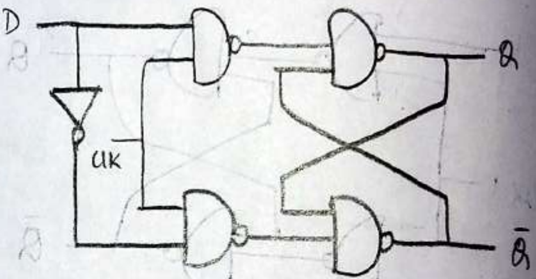


Clk	S	R	Q	$\bar{Q}$
0	X	X	Q	$\bar{Q}$
⎍	0	0	Q	$\bar{Q}$
⎍	0	1	0	1
⎍	1	0	1	0
⎍	1	1	1*	1* Forbidden state

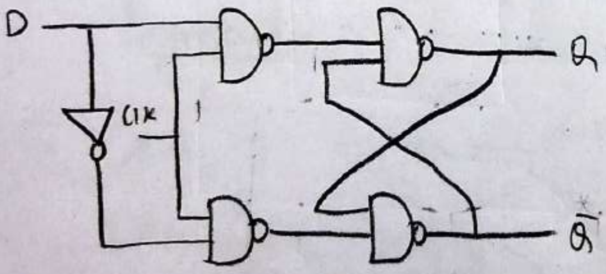


D - flip flop.



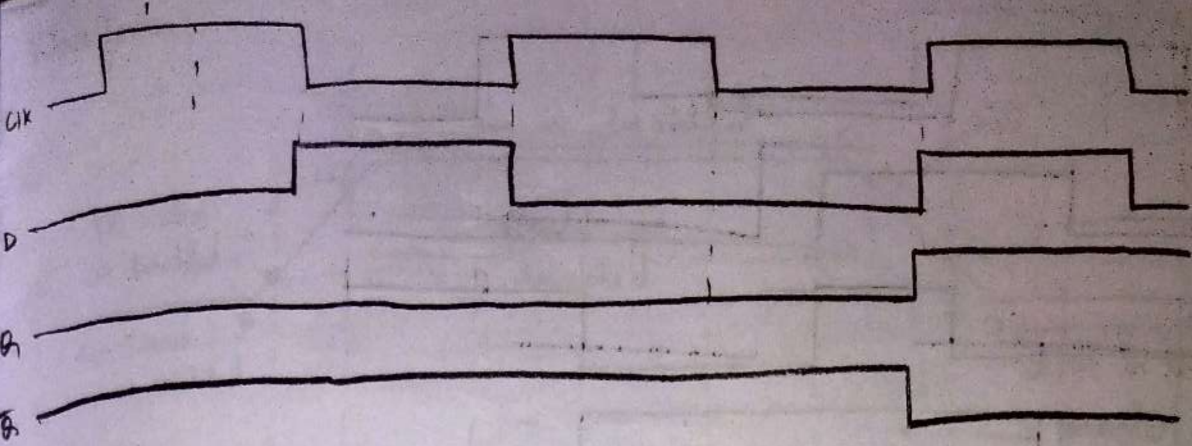


case①:- Clk = 0, D = 0, $Q = Q$, $\bar{Q} = \bar{Q}$

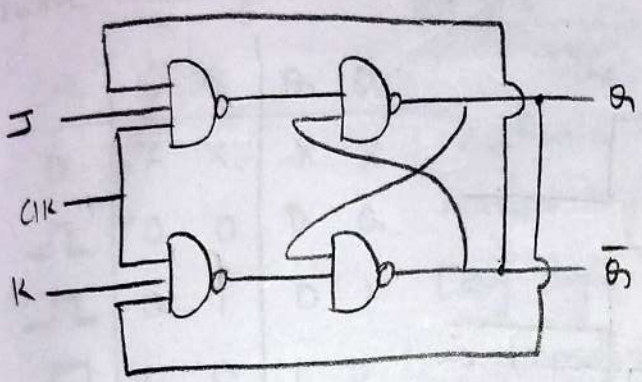


Truth table

Clk	D	Q	$\bar{Q}$
0	X	Q	$\bar{Q}$
⎍	0	0	1
⎍	1	1	0

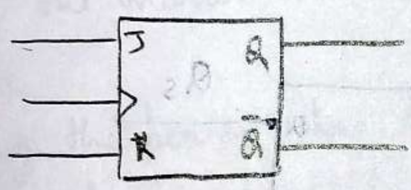


JK flip flop:-

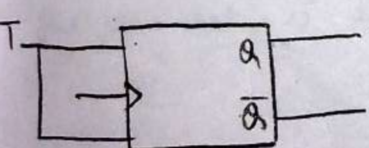


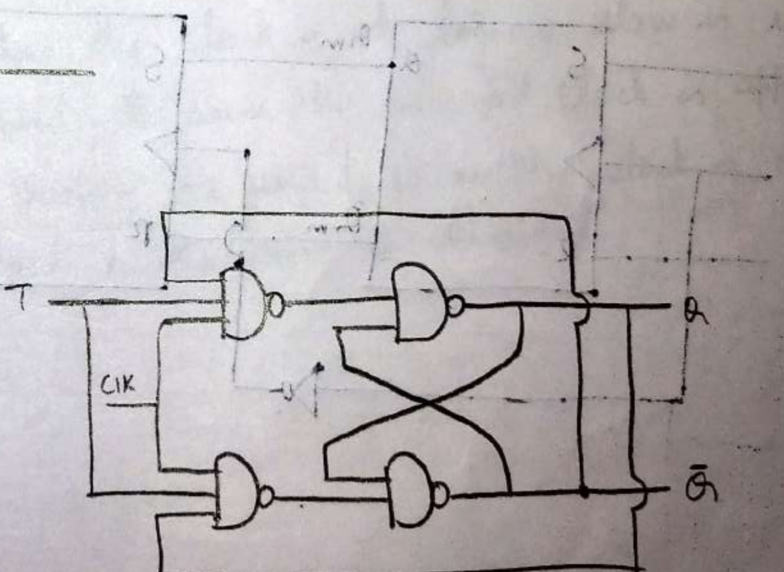
Truth table:-

Clk	J	K	Q	$\bar{Q}$	
0	X	X	Q	$\bar{Q}$	memory
⎍	0	0	Q	$\bar{Q}$	memory
⎍	0	1	0	1	Reset
⎍	1	0	1	0	set
⎍	1	1	$\bar{Q}$	Q	toggle.



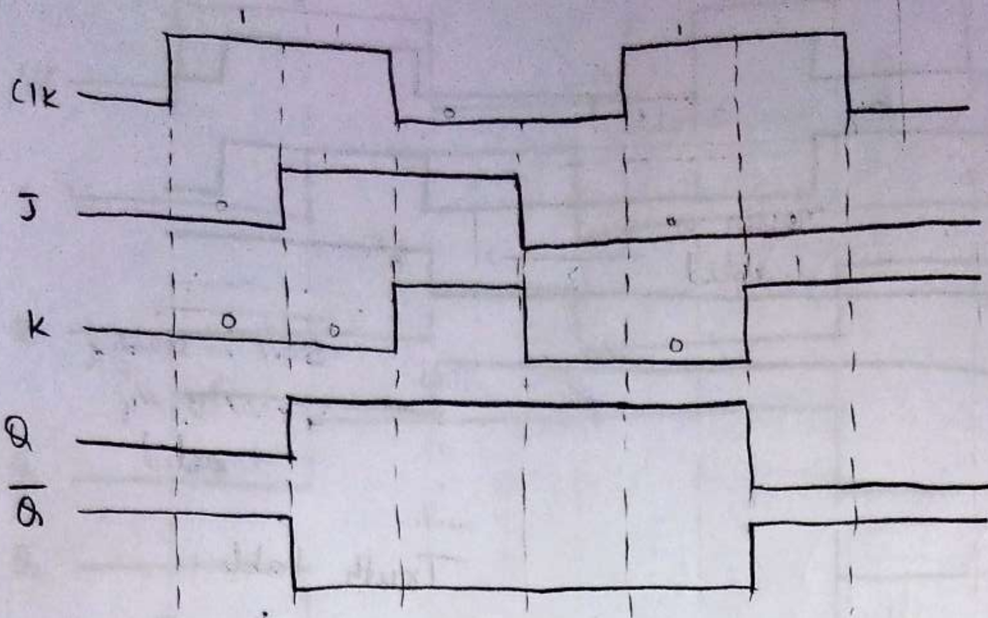
T-flip flop:

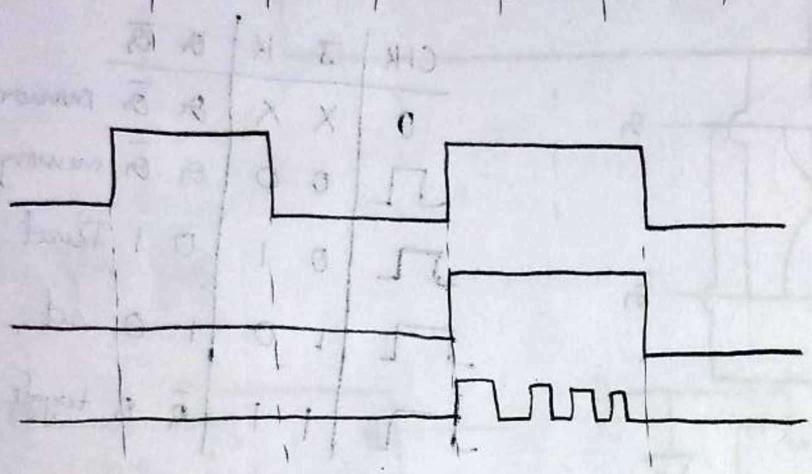




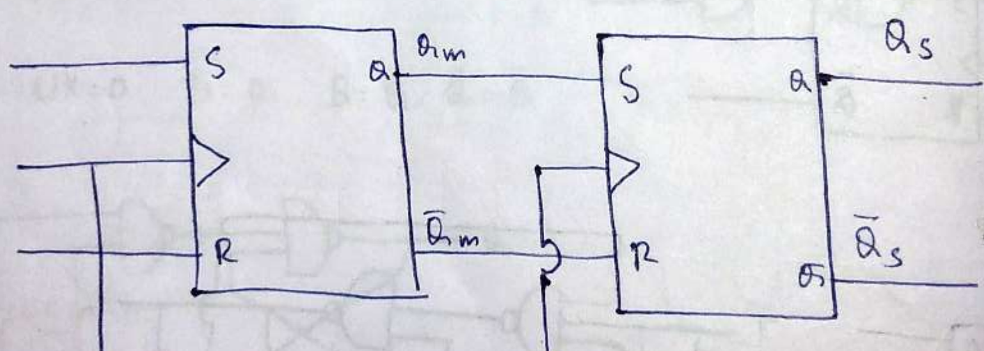
Truth table:-

Clk	T	Q	$\bar{Q}$	state
0	X	Q	$\bar{Q}$	memory
⎍	0	Q	$\bar{Q}$	memory
⎍	1	$\bar{Q}$	Q	Toggle

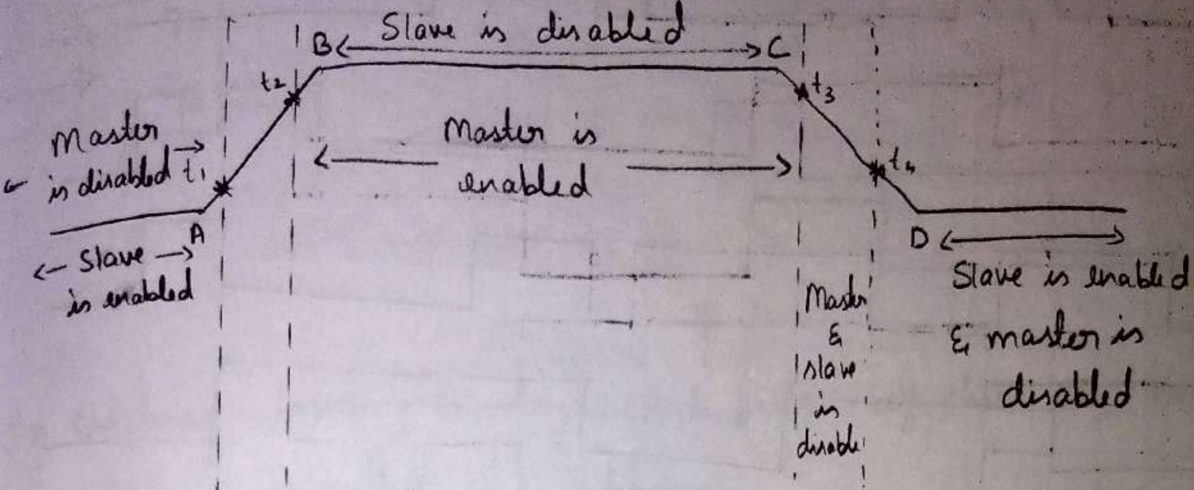




Master slave SR flip flop [Pulse triggered]:-



Wave form :-

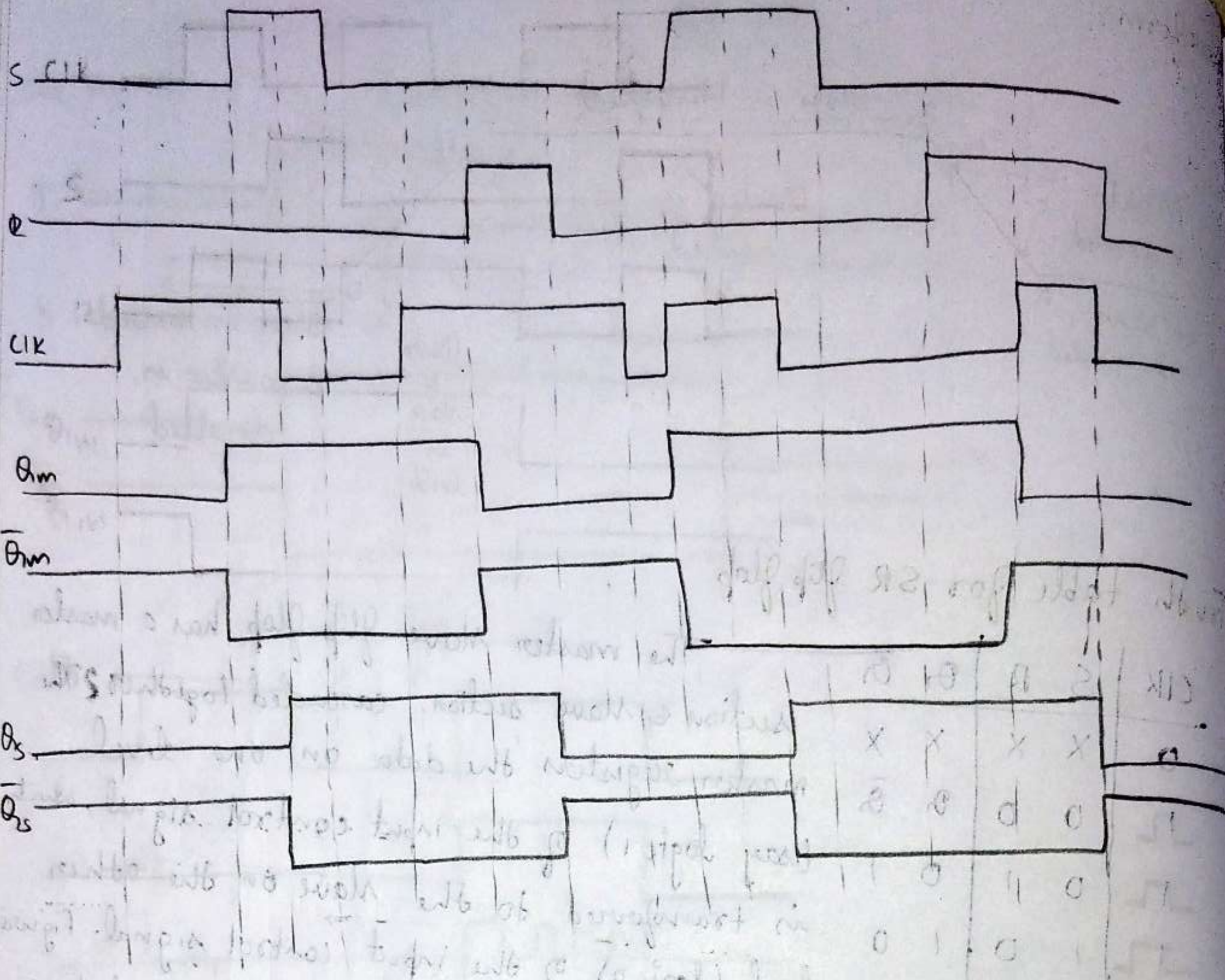


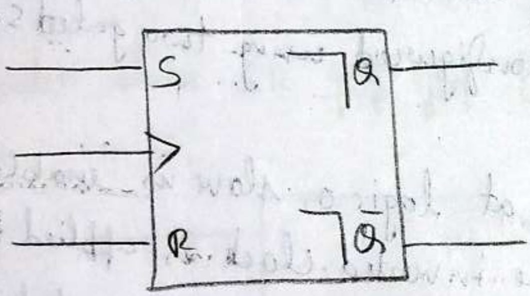
Truth table for SR flip flop

Clk	S	R	Q	$\bar{Q}$
0	X	X	X	X
⎍	0	0	Q	$\bar{Q}$
⎍	0	1	0	1
⎍	1	0	1	0
⎍	1	1	1*	1*

The master slave flip flop has a master section & slave section, cascaded together. The master registers the data on one level (say logic 1) of the input control signal, which is transferred to the slave on the other level (logic 0) of the input control signal. Figure shows the master slave SR flip flop configured using two gated SR latch.

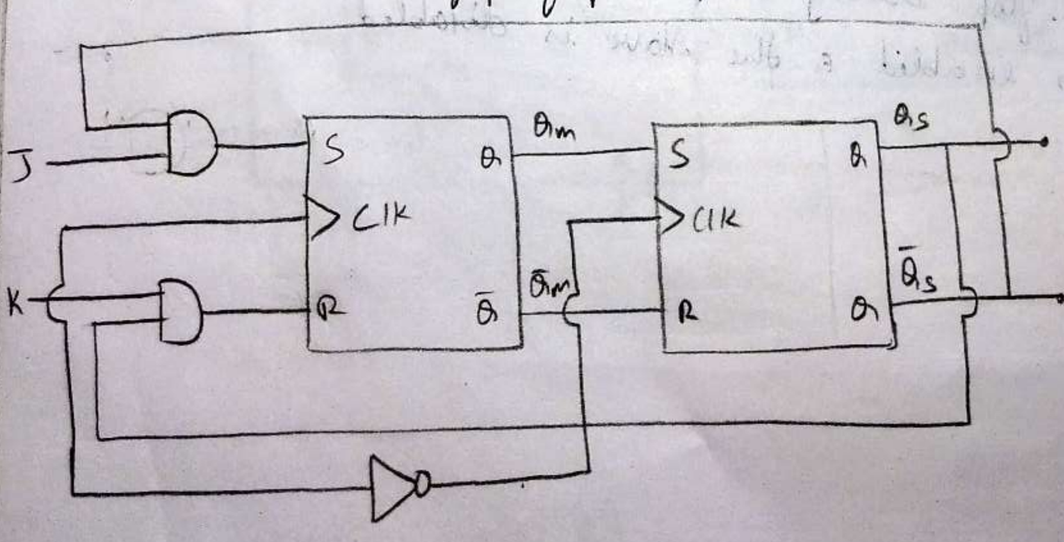
During the period when the clock is at logic 0, slave is enabled while master is disabled. Because the inverted clock is applied to the slave flip-flop. During the period, when the clock is at logic 1, the master is enabled & the slave is disabled.



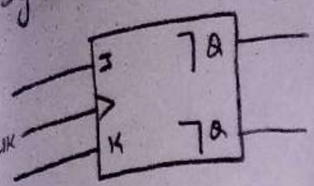


⌐ → postpone indicator

Master slave J K flip-flop



Symbol:

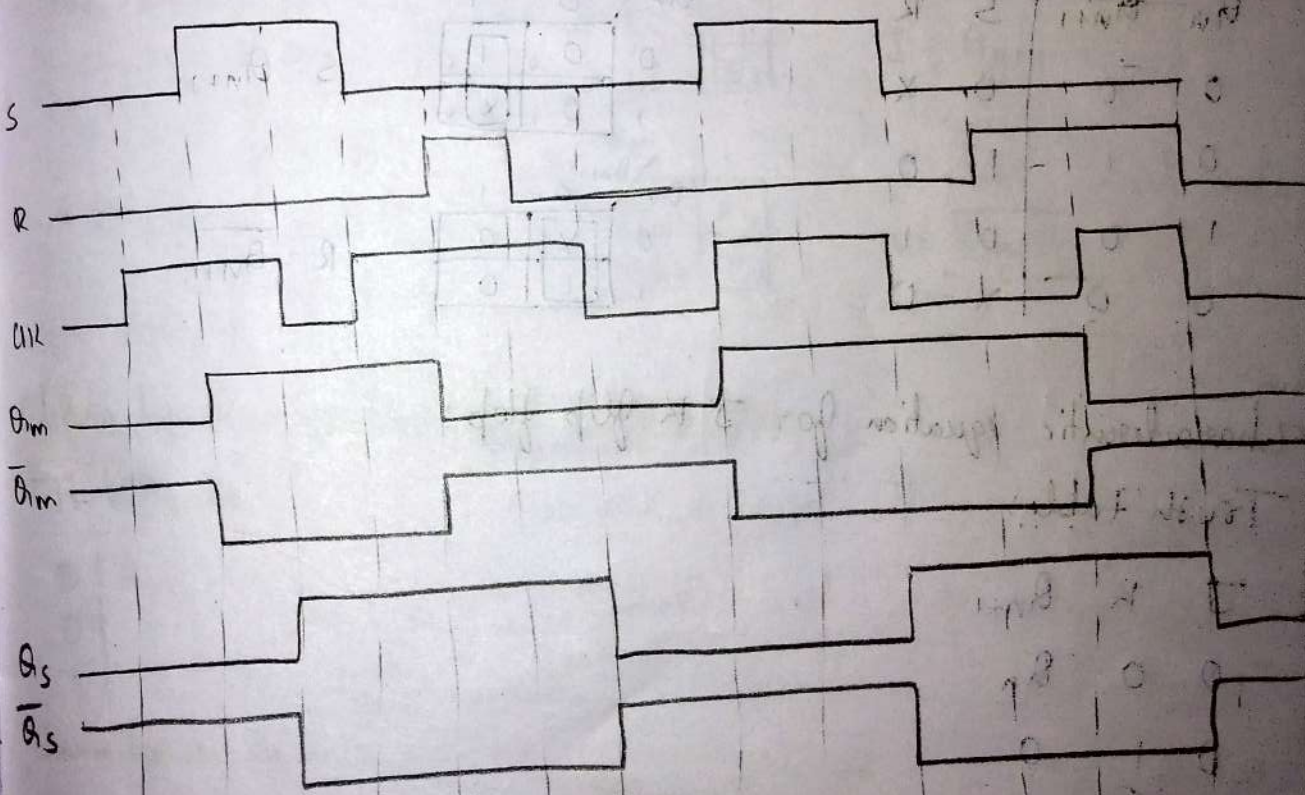


Truth table:-

Clk	J	K	Q	$\bar{Q}$
0	x	x	Q	$\bar{Q}$
1	0	0	Q	$\bar{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\bar{Q}$	Q

0's catching:- During a single clock pulse, if there is a transition from 1 to 0 is called 0's catching.

1's catching:- During a single clock pulse, if there is a transition from 0 to 1 is called 1's catching.



Characteristic equation for SR flip flop

characteristic table, excitation table: for SR flip flop.

Truth table:

S	R	
0	0	Q_n -> previous state
0	1	0 -> Reset
1	0	1 -> set
1	1	forbidden

Q_{n+1} -> next state

Characteristic table:

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

K-map

Q_n \ SR	00	01	11	10
0	0 (0)	0 (1)	X (3)	1 (2)
1	1 (4)	0 (5)	X (7)	1 (6)

$$Q_{n+1} = R + Q_n\overline{R}$$

Transition table:

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
0	0	X	0

Q_n \ Q_{n+1}	0	1
0	0 (0)	1 (1)
1	0 (2)	X (3)

$$S = Q_{n+1}$$

Q_n \ Q_{n+1}	0	1
0	X	0
1	1	0

$$R = \overline{Q_{n+1}}$$

Characteristic equation for J K flip flop:

Truth table:

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Characteristic table:-

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Q_n \ JK	00 ($\bar{J}\bar{K}$)	01	11 (J K)	10 (J $\bar{K}$)
0	0	0	1	1
1	1	0	0	1

$Q_{n+1} = \bar{Q}_n \bar{J} + \cancel{Q_n \bar{K}} + J Q_n$

$Q_{n+1} = \bar{K} Q_n + \bar{Q}_n J$

Transition table:-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_n \ Q_{n+1}	0	1
0	0	1
1	X	X

$J = Q_{n+1}$

Q_n \ Q_{n+1}	0	1
0	X	X
1	1	0

$K = \overline{Q_{n+1}}$

Characteristic equation for D flip flop

Truth table:-

D	Q_{n+1}
0	0
1	1

Characteristic table:-

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Q_n \ D	0	1
0	0	1
1	0	1

$Q_{n+1} = D$

transition table:-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

$Q_n \backslash Q_{n+1}$	0	1
0	0 (0)	1 (1)
1	0 (2)	1 (3)

$D = Q_{n+1}$

T flip-flop

Truth table:-

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

characteristic table:-

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$Q_n \backslash T$	$\overline{T}$ 0	T 1
$\overline{Q_n}$ 0	0 (0)	1 (1)
Q_n 1	1 (2)	0 (3)

$Q_{n+1} = Q_n \overline{T} + \overline{Q_n} T$

$Q_{n+1} = Q_n \oplus T$

Transition table:-

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

$Q_n \backslash Q_{n+1}$	0	1
0	0 (0)	1 (1)
1	0 (2)	1 (3)

~~$T = Q_{n+1}$~~

$Q_n \backslash Q_{n+1}$	0	1
0	0 (0)	1 (1)
1	1 (2)	0 (3)

$T = \overline{Q_n} Q_{n+1} + \overline{Q_{n+1}} Q_n$

$T = Q_n \oplus Q_{n+1}$

Registers:- Is used to store more than one bit of data.

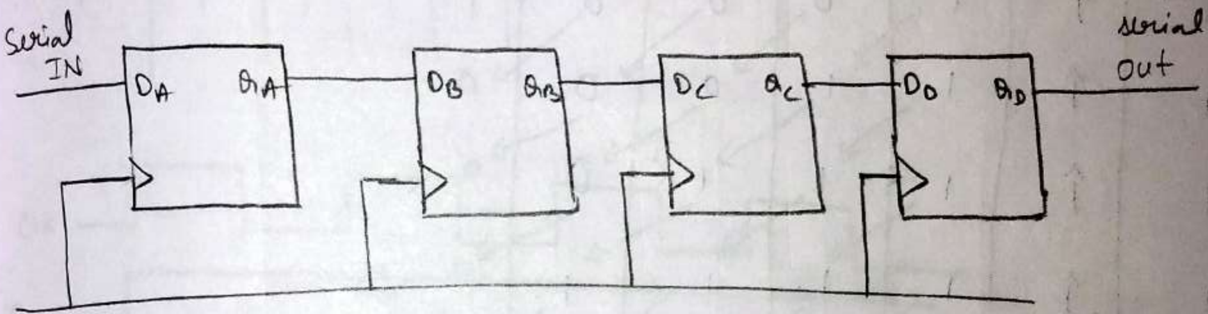
Based on the shifting operation we have two types of registers

* Unidirectional shift register
* Bidirectional shift register.

Depending upon the i/P & o/P register can be classified as

1. Serial in serial out [SISO]
2. Serial in parallel out [SIPO]
3. Parallel in serial out [PISO]
4. Parallel in parallel out [PIPO]

Serial in serial out:-



Serial delta	Clk	Q_A	Q_B	Q_C	Q_D	
	Initially	0	0	0	0	
1	↑	1	0	0	0	0
1	↑	1	1	0	0	0
0	↑	0	1	1	0	0
1	↑	1	0	1	1	0
	↑	0	1	0	1	1
	↑	0	0	1	0	1
	↑	0	0	0	1	0
	↑	0	0	0	0	1

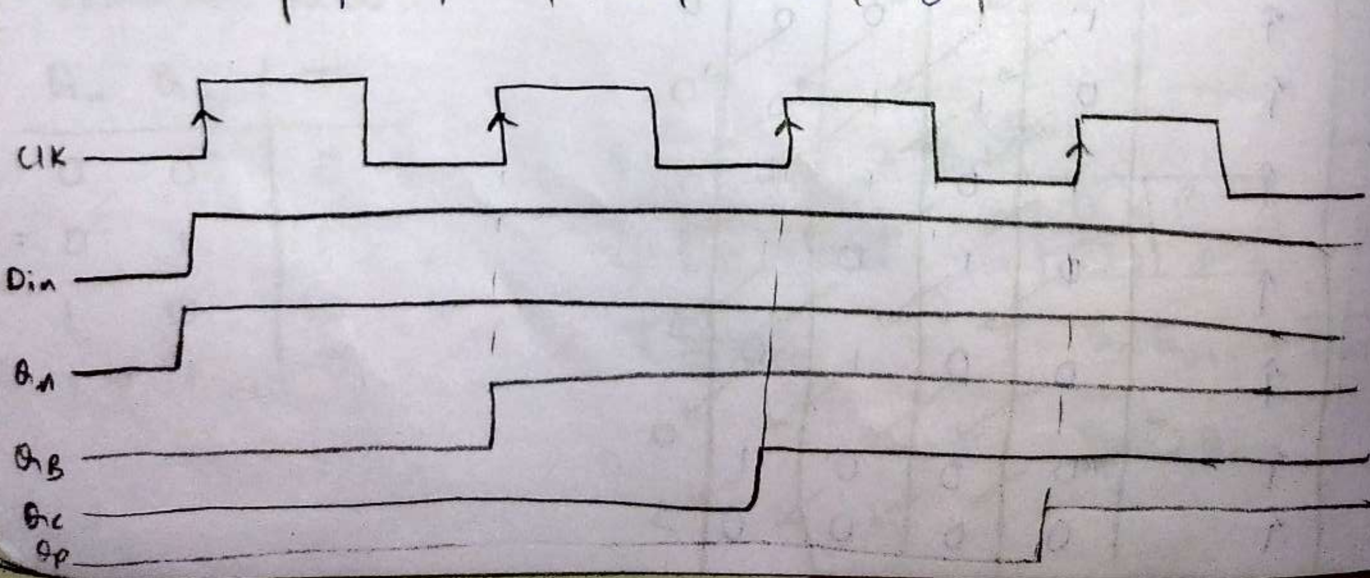
* Serial in serial out unidirectional shift register are constructed from positive edge triggered D-flip flop.

* The Q O/P of each flipflop is connected to the D i/p of flip flop to the right.

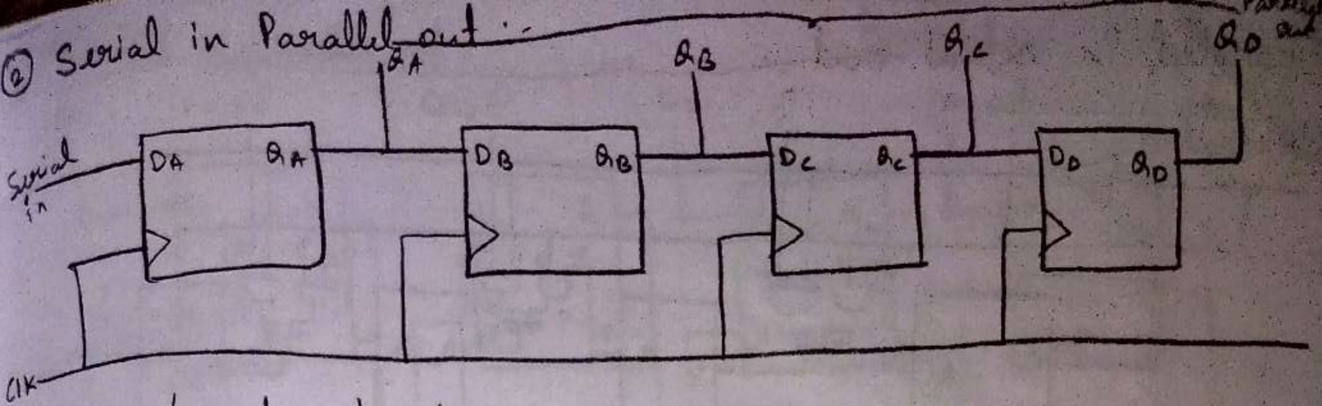
* The control i/p's of all the flipflop are connected together to common synchronizing signal called as the clock.

* Thus upon the occurance of positive edge of the clock signal the content of each flip flop is shifted one position to the right

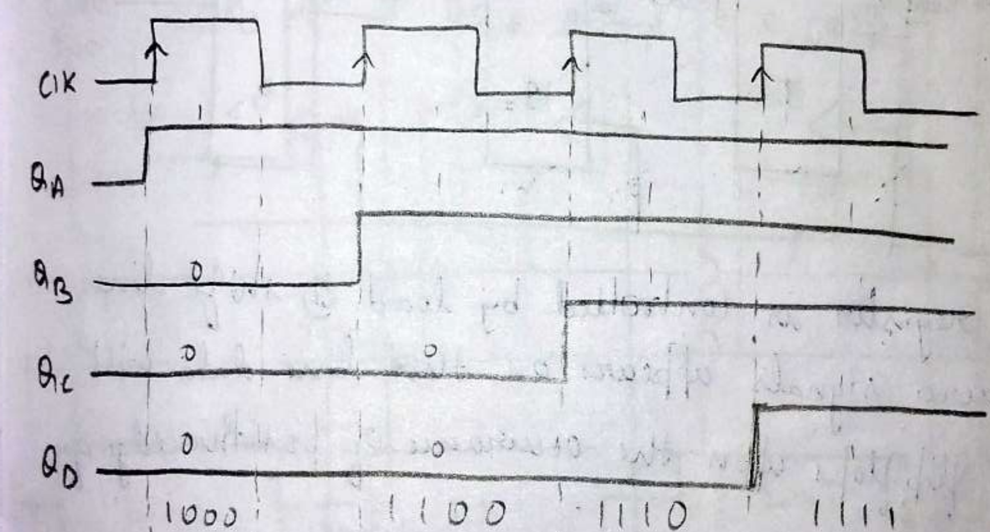
Serial data	Clk	Q_A	Q_B	Q_C	Q_D	
	Initially	0	0	0	0	
1	↑	1	0	0	0	
1	↑	1	1	0	0	0
1	↑	1	1	1	0	0
1	↑	1	1	1	1	0
	↑	0	1	1	1	1
	↑	0	0	1	1	1
	↑	0	0	0	1	1
	↑	0	0	0	0	1



② Serial in Parallel out

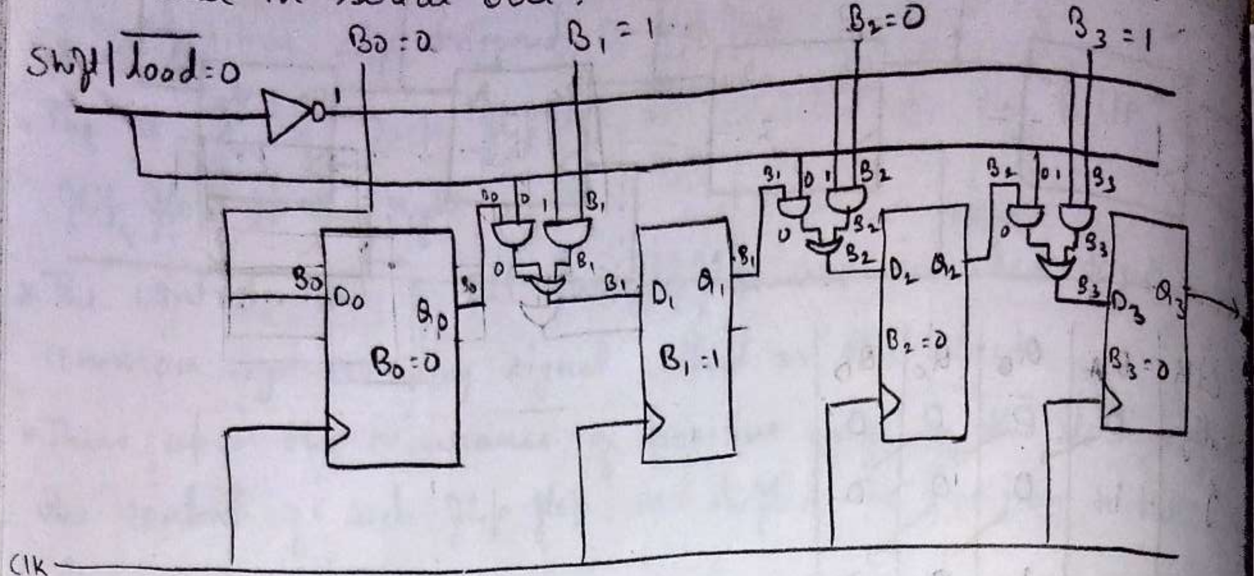


Clk	Q_A	Q_B	Q_C	Q_D
Initially	0	0	0	0
↑	1	0	0	0
↑	1	1	0	0
↑	1	1	1	0
↑	1	1	1	1

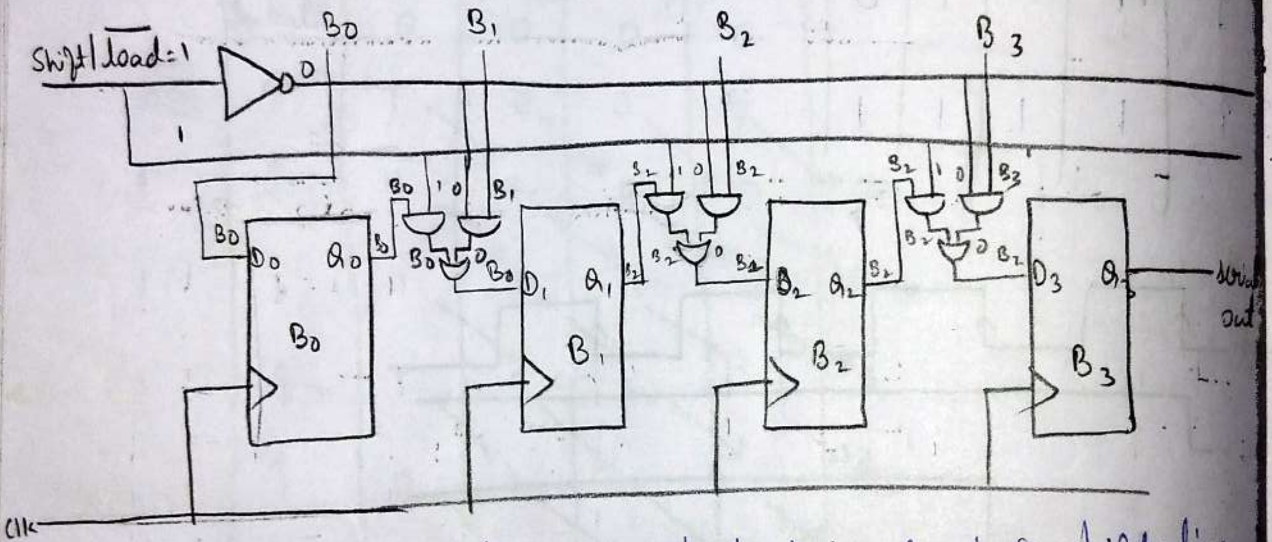


* The serial in parallel out unidirectional shift register is as shown above.
* Once information is shifted into the register that is serial in, the information is available as a single entity i.e., parallel out at the flip flop output terminal.

③ Parallel in serial out :-

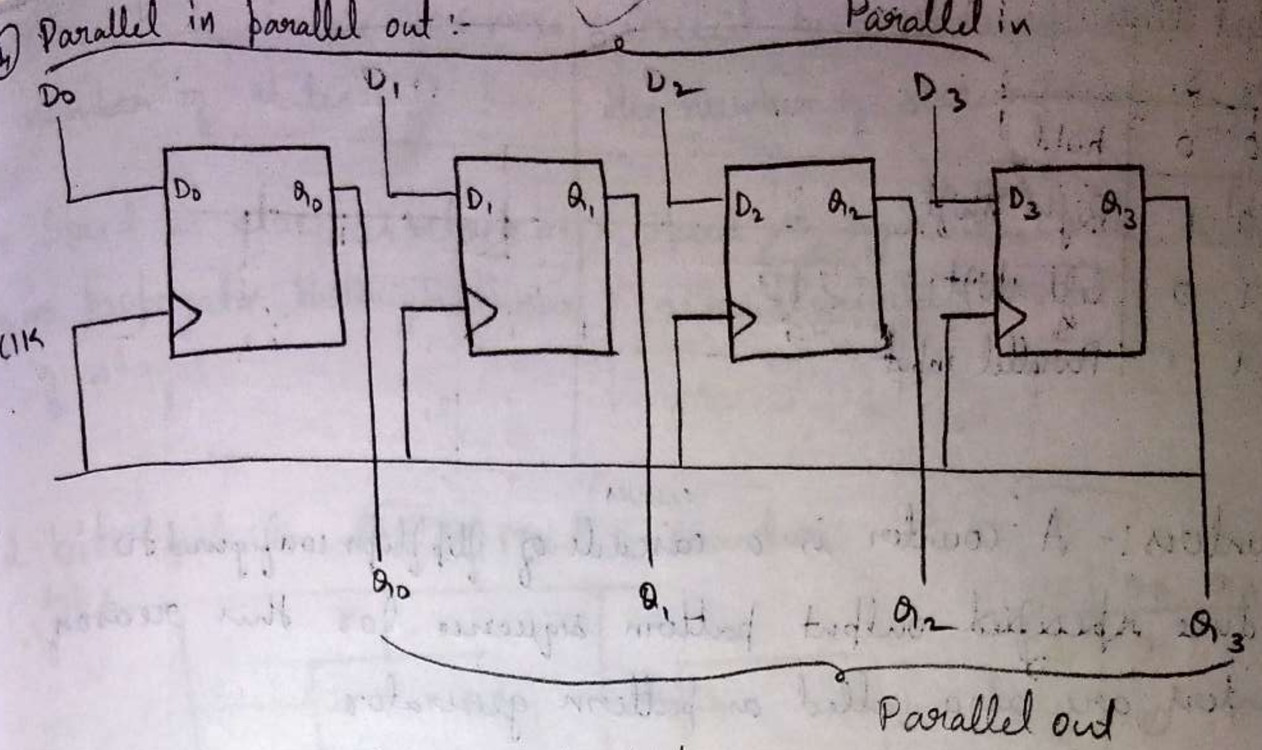


Load mode : 0
Shift mode = 1

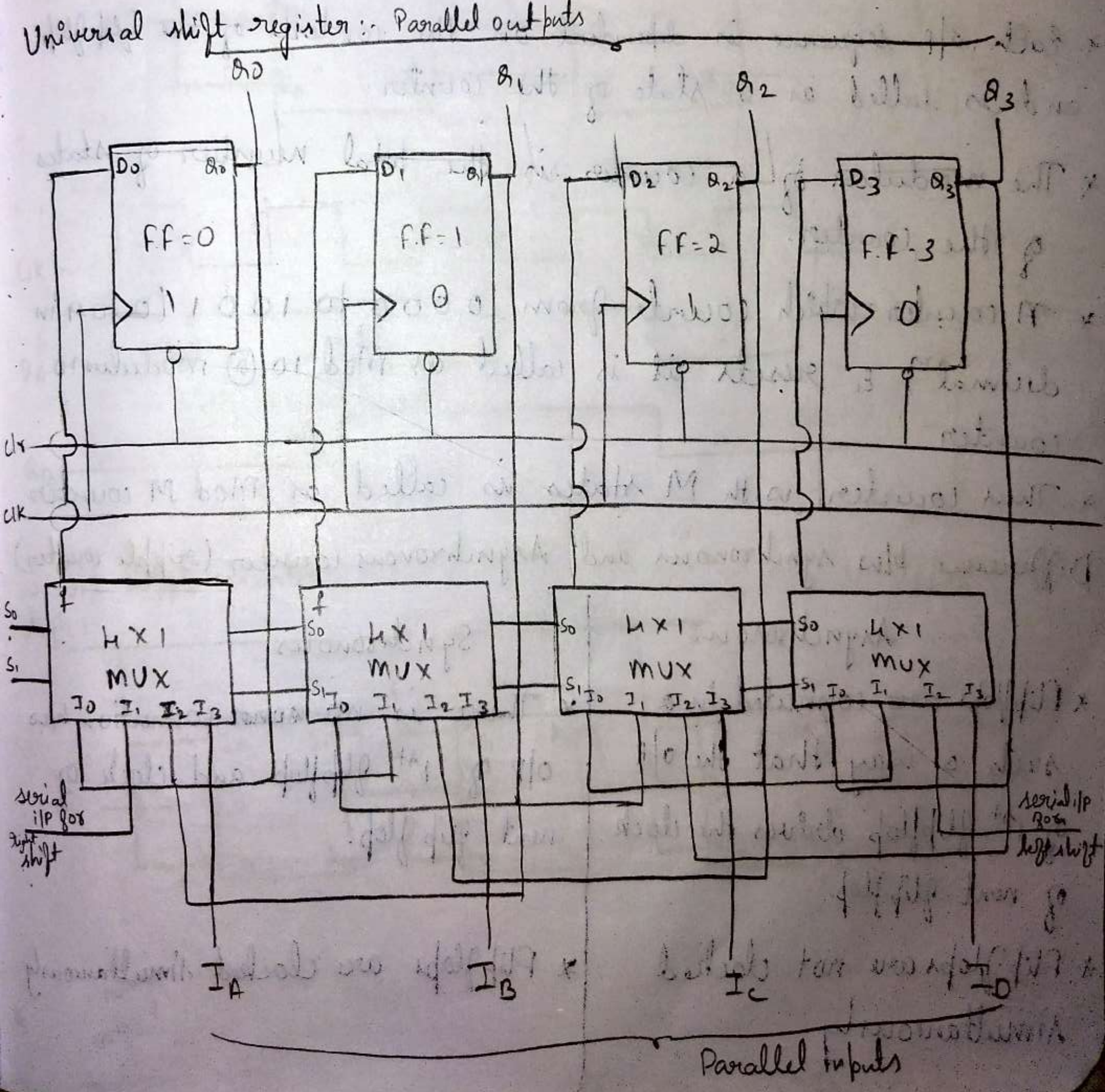


* The operation of register is controlled by load (or) shift line. When a logic zero signals appears on this line data will be loaded into flipflops upon the occurance of positive edge of the clock pulse.
* When logic one signal appears on load (or) shift line the D flip flop becomes a cascade connection that function as a unidirectional shift register providing the serial output

(4) Parallel in parallel out :-



Universal shift register :-



Select lines:

S_0	S_1	
0	0	hold
0	1	Right shift
1	0	left shift
1	1	Parallel input

Counters:- A counter is a cascade (series) of flipflops configured to produce ~~specified~~ output pattern sequence for this reason counters are also called as pattern generator.

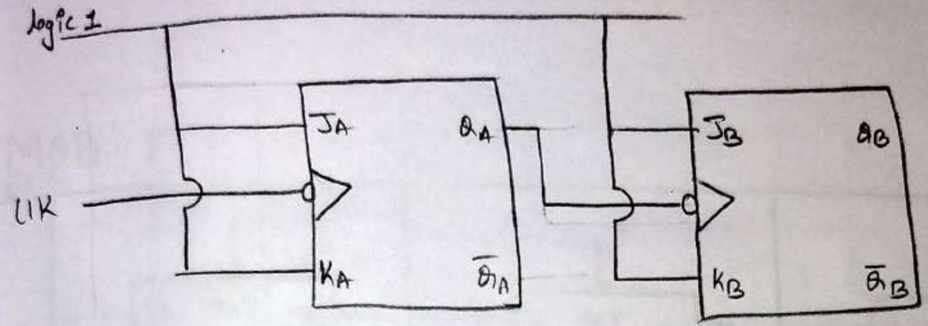
* Each o/p sequence is dependent on the contents of the flipflop and is called as a state of the counter.
* The modulus of a counter is the total number of states of the counter.
* A counter which counts from 0000 to 1001 (0 to 9 in decimal) & resets it is called as Mod 10 (or) modulus 10 counter.
* Thus counter with M states is called as Mod M counter.

Difference b/w synchronous and Asynchronous counter (ripple counter)

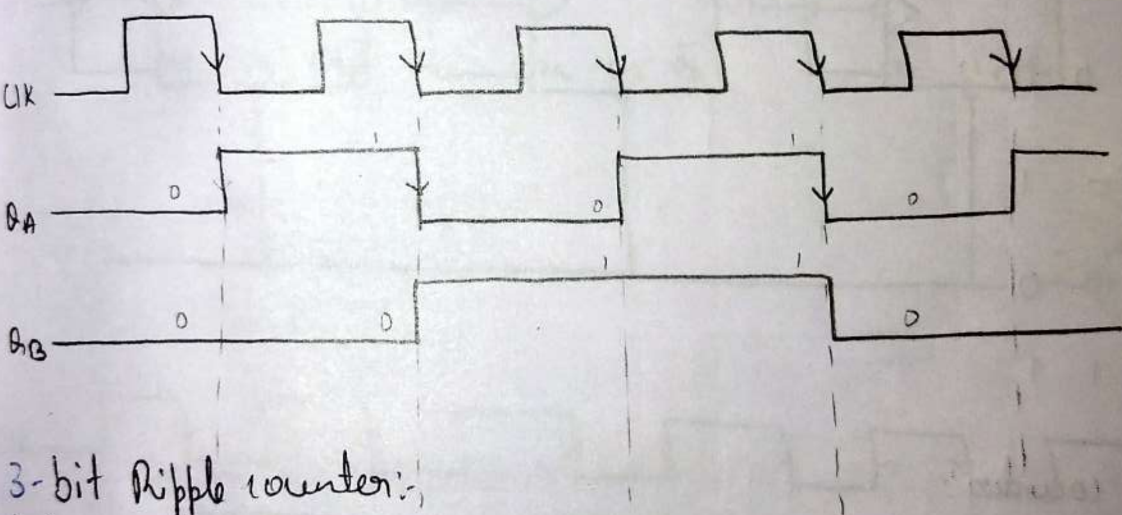
Asynchronous	Synchronous
* Flipflops are connected in a such a way that the o/p of 1st flipflop drives the clock of next flipflop.	* There is no ~~common~~ connection b/w o/p of 1st flipflop and clock of next flip flop.
* Flipflops are not clocked simultaneously	* Flipflops are clocked simultaneously

* Circuit is simple for more number of states	* Circuit becomes complicated as the number of states increases.
* Speed is slow as clock as to propogate through number of stages.	* Speed is high as clock is given simultaneously.

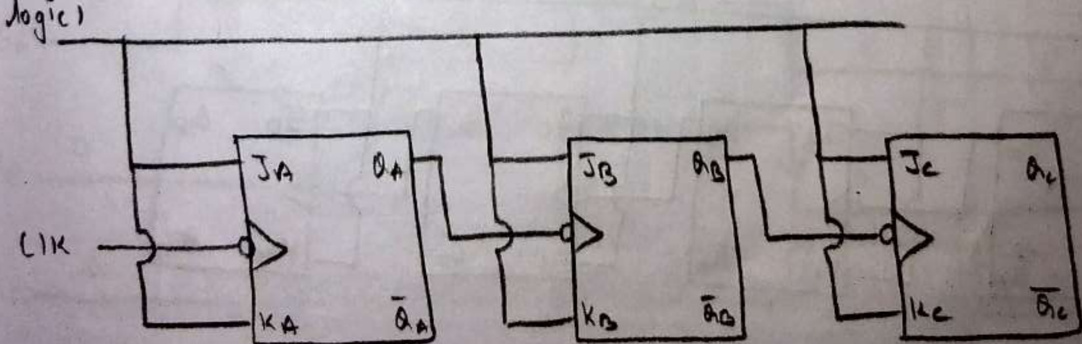
2-bit Ripple counter (or) Mod 4 counter :-

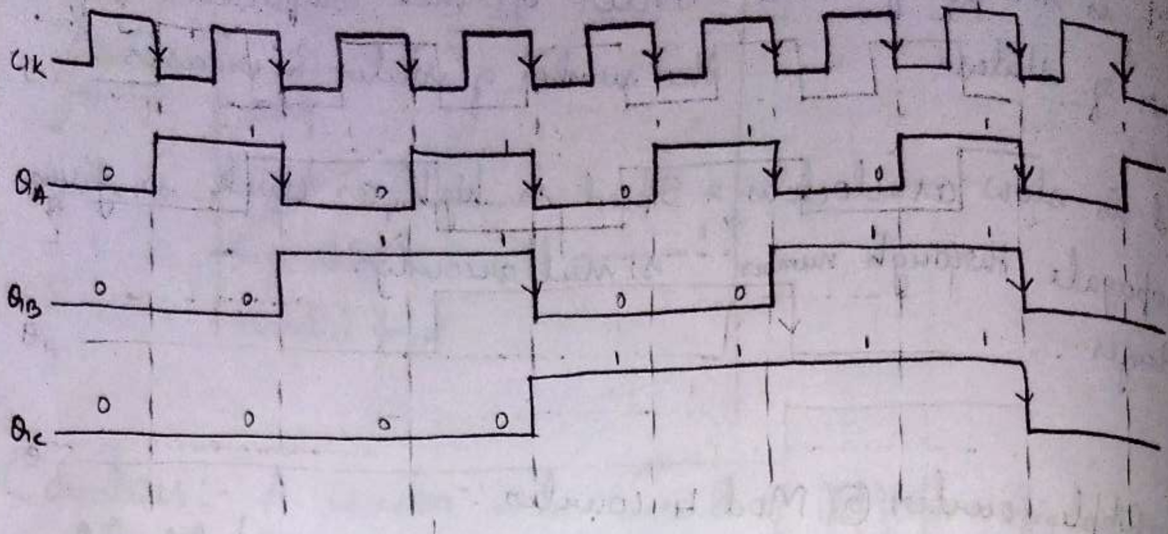


CLK	Q_A	Q_A
↓	0	0
↓	0	1
↓	1	0
↓	1	1



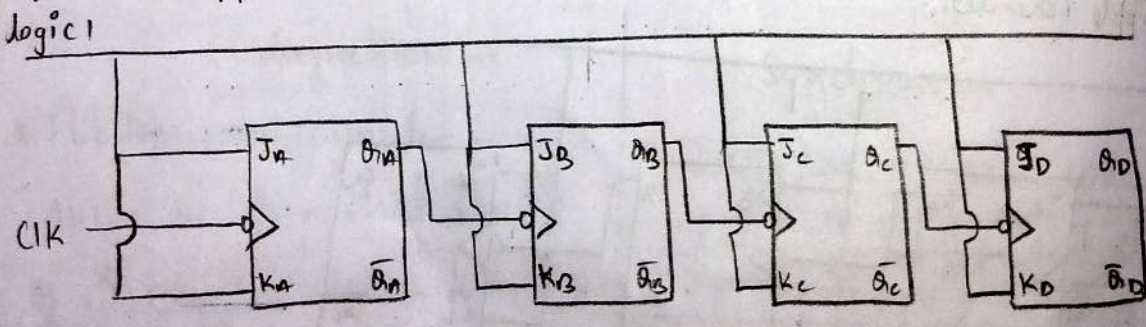
3-bit Ripple counter :-

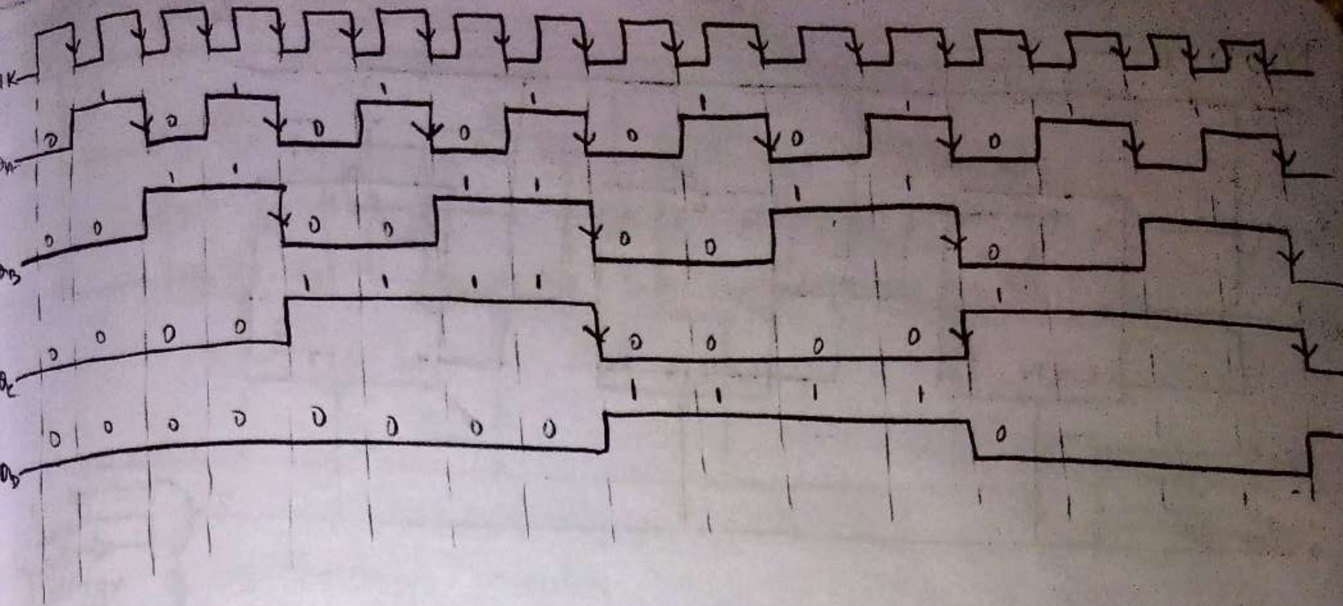




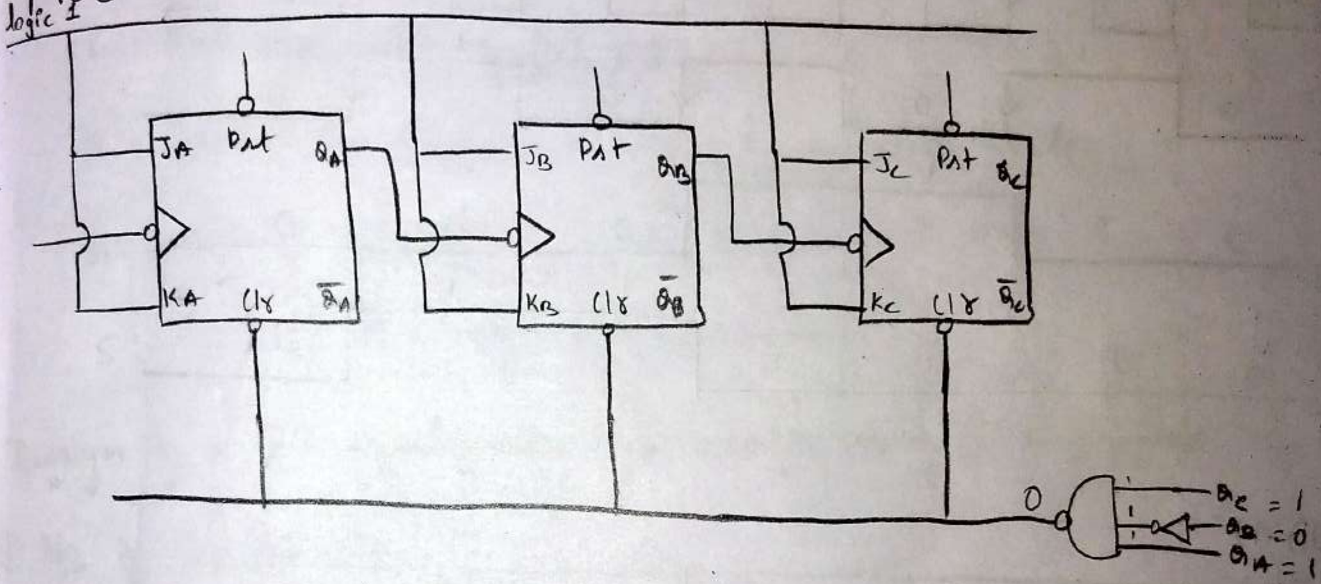
Clk	Q_C	Q_B	Q_A
↓	0	0	0
↓	0	0	1
↓	0	1	0
↓	0	1	1
↓	1	0	0
↓	1	0	1
↓	1	1	0
↓	1	1	1

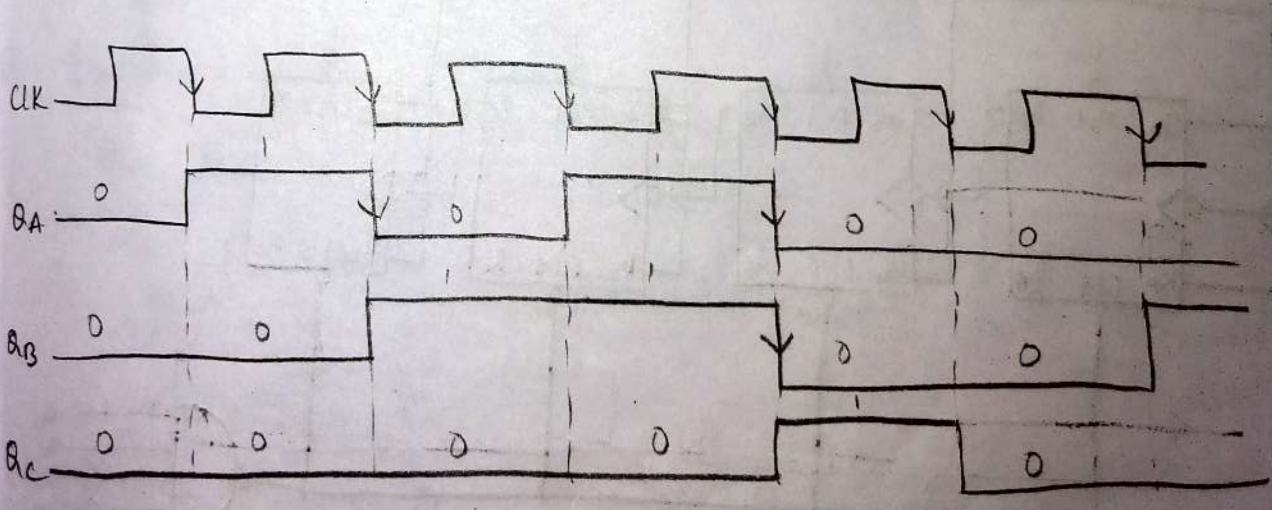
4-bit ripple counter:




CLK
QA
QB
QC
QD

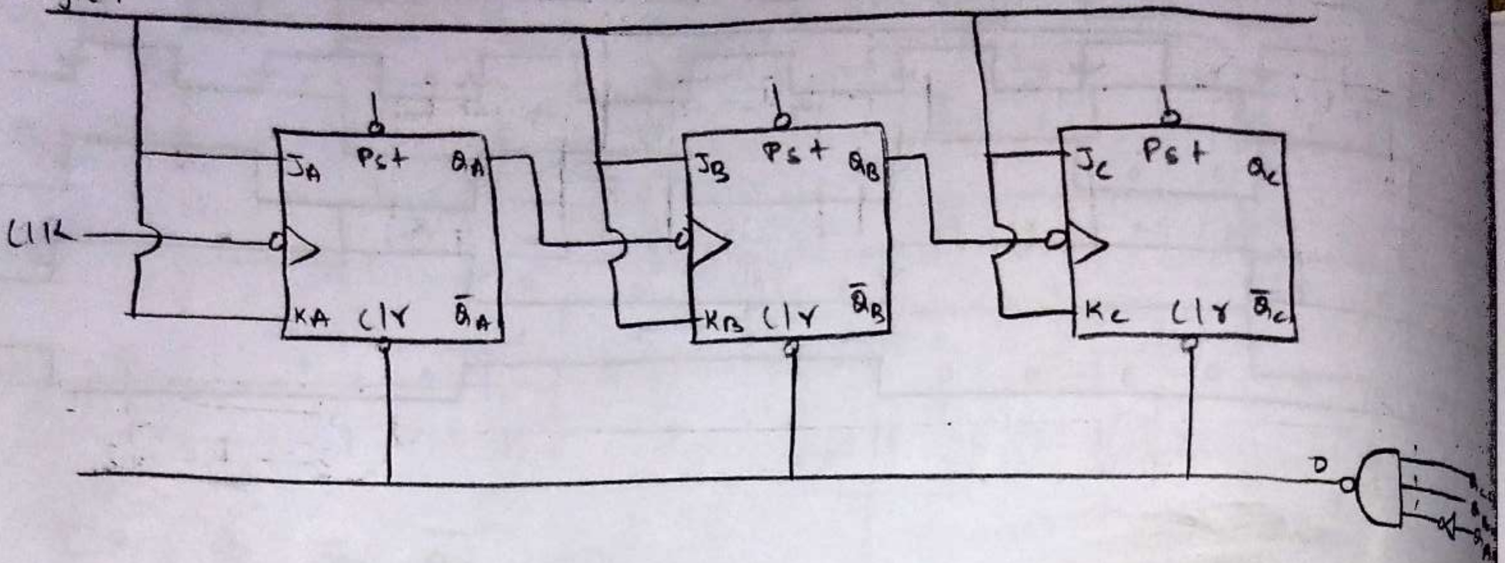
MOD-5

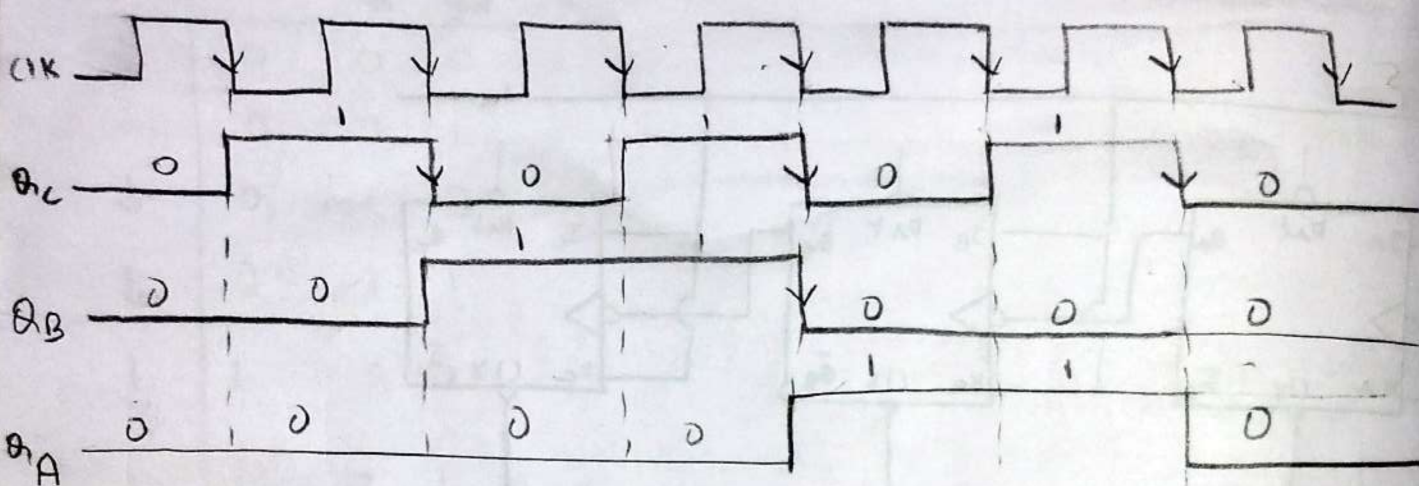

logic 1
JA
Pst
QA
KA
Clr
$\overline{Q_A}$
JB
Pst
QB
KB
Clr
$\overline{Q_B}$
JC
Pst
QC
KC
Clr
$\overline{Q_C}$
0
$Q_C = 1$
$Q_B = 0$
$Q_A = 1$


CLK
QA
QB
QC

MOD-6

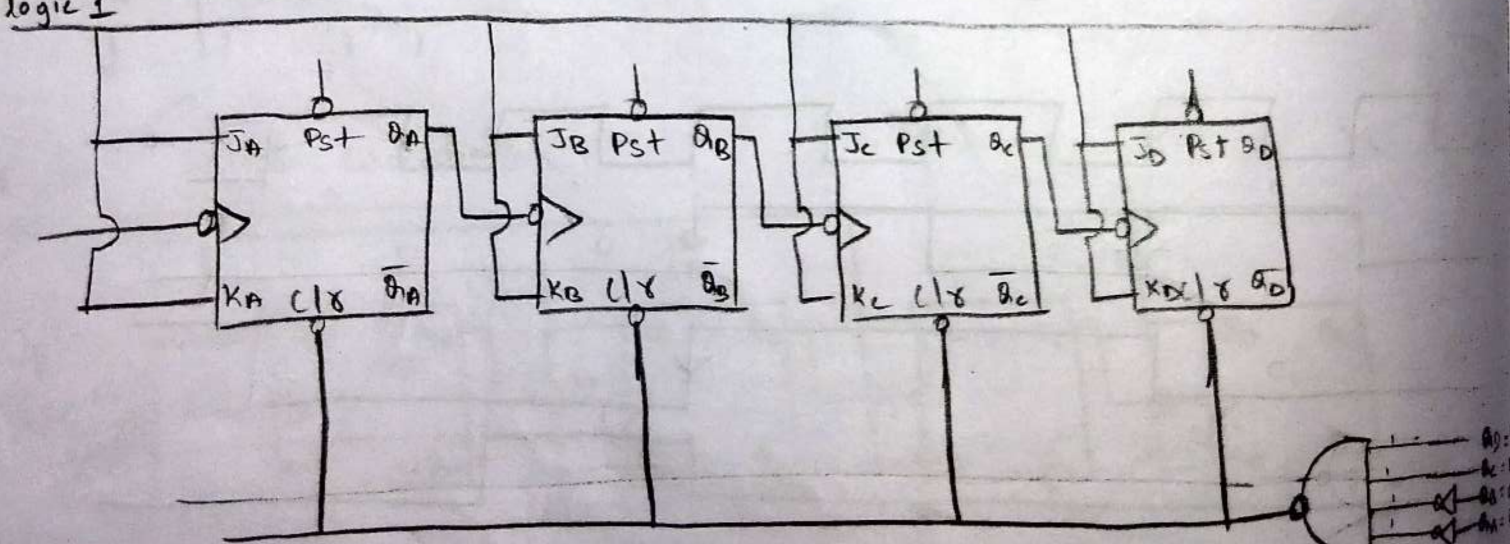
logic 1



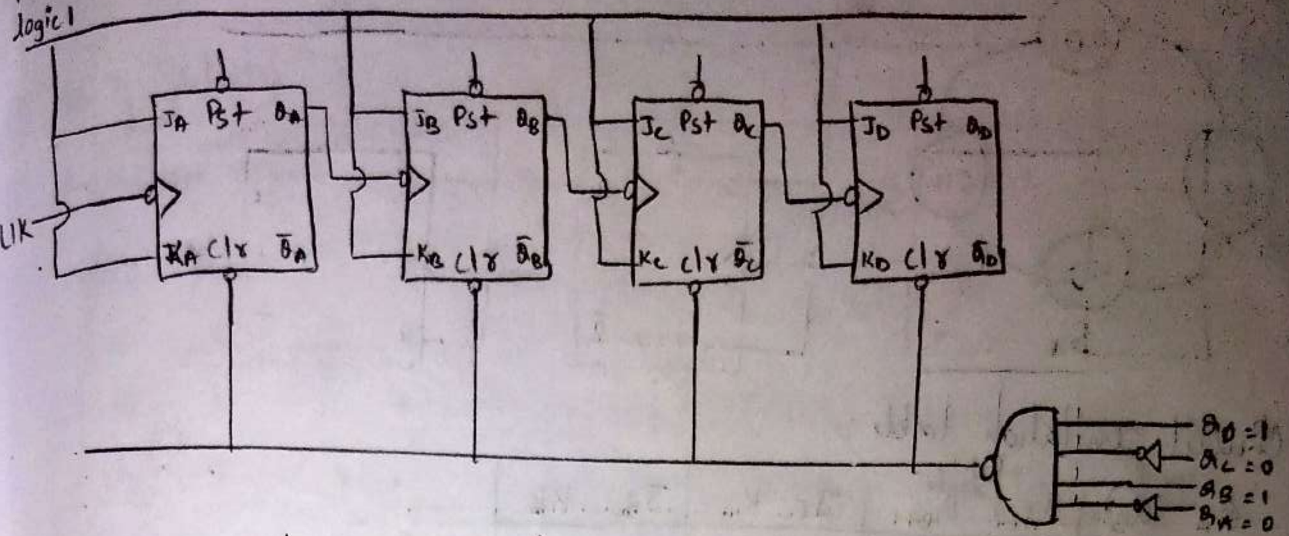


MOD-12

logic 1



MOD-10 | Decade counter:-



Design of synchronous counter:-

Steps 1:- Decide the number of flip flop.

2:- Excitation table of flip flop

3:- State dig diagram & Circuit excitation table.

4:- Obtain simplified equation using K-map.

5:- Draw the logic diagram.

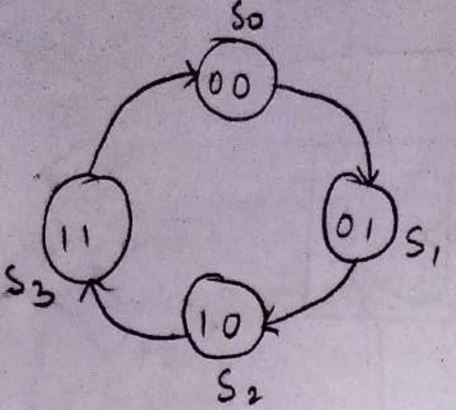
Design of 2 bit synchronous up counter using JK flip flop:-

① No of flip flop - 02

② Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

③ State diagram:-



Circuit excitation table:-

Present state Q_A	Q_B	next state Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

$Q_A \backslash Q_B$	0	1
0	0 (0)	1 (1)
1	X (2)	X (3)

$J_A = Q_B$

$Q_A \backslash Q_B$	0	1
0	X (0)	X (1)
1	0 (2)	1 (3)

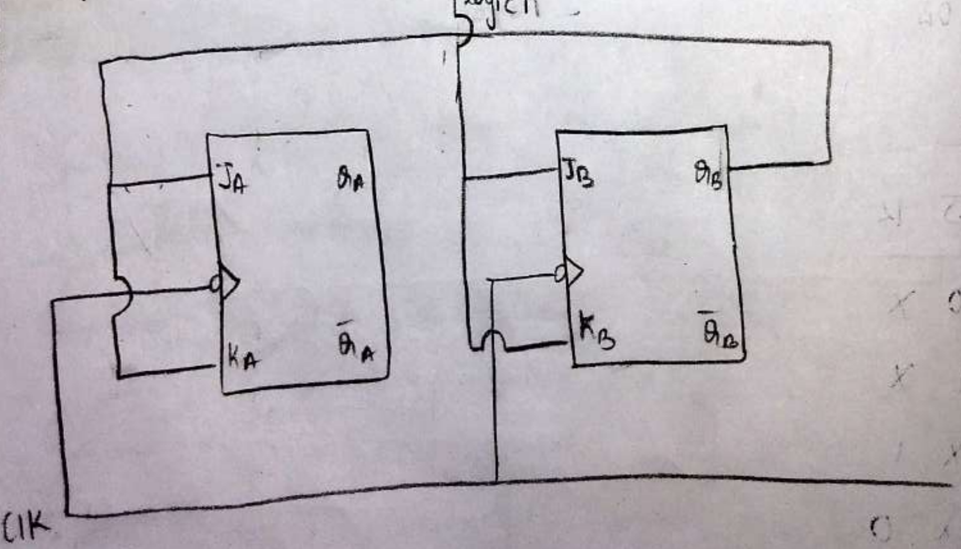
$K_A = Q_B$

$Q_A \backslash Q_B$	0	1
0	1 (0)	X (1)
1	1 (2)	X (3)

$J_B = 1$

$Q_A \backslash Q_B$	0	1
0	X (0)	1 (1)
1	X (2)	1 (3)

$K_B = 1$



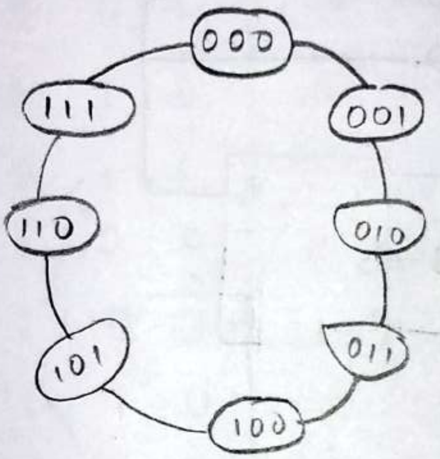
Design of 3-bit synchronous up counter using JK flip flop :-

① No of flip flop = 3

② Excitation table :-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

③ State diagram :-



Circuit excitation table :-

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	0_0	0_1	1_3	0_2
1	X_4	X_5	X_7	X_6

$J_A = Q_B Q_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X_0	X_1	X_3	X_2
1	0_4	0_5	1_7	0_6

$K_A = Q_B Q_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	0_0	1_1	X_3	X_2
1	0_4	1_5	X_7	X_6

$J_B = Q_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X_0	X_1	1_3	0_2
1	X_4	X_5	1_7	0_6

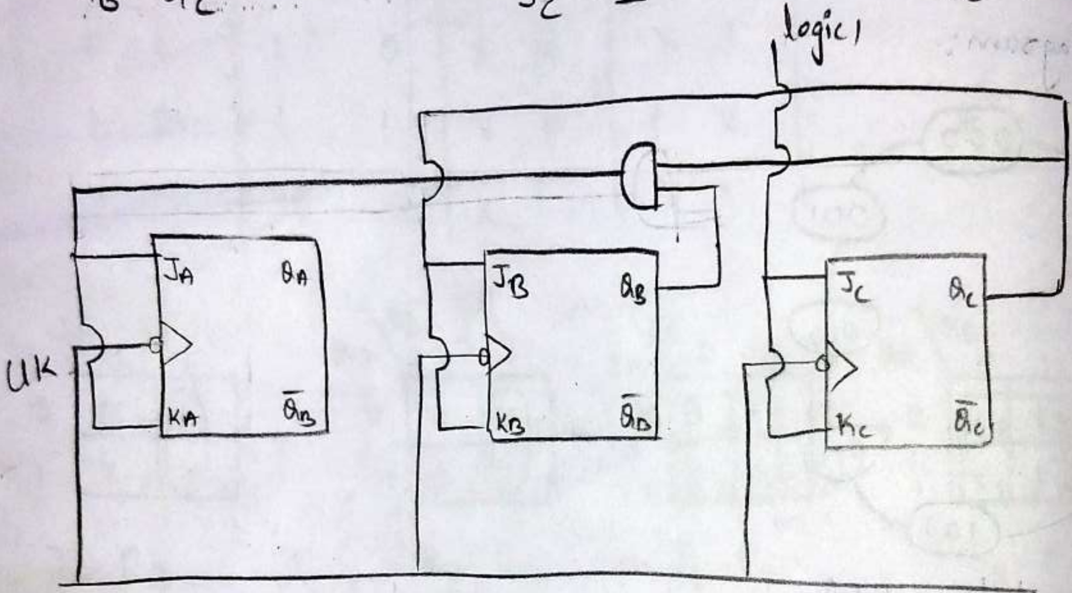
$K_B = Q_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	1_0	X_1	X_3	1_2
1	1_4	X_5	X_7	1_6

$J_C = 1$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X_0	1_1	1_3	X_2
1	X_4	1_5	1_7	X_6

$K_C = 1$



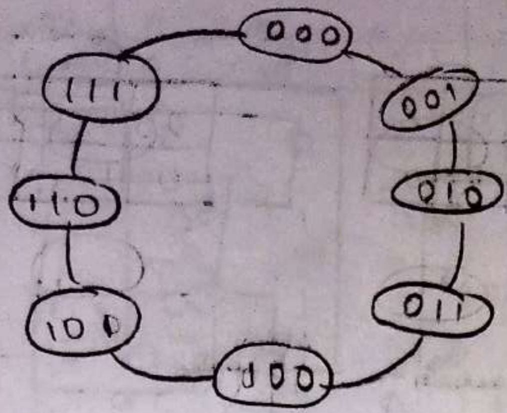
3-bit synchronous upcounter using SR flip flop:

① No of flip flop = 03

② Excitation table:-

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

③ State diagram:-



circuit exitation table

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	R_A	J_B	R_B	S_C	R_C
0	0	0	0	0	1	0	X	0	X	1	0
0	0	1	0	1	0	0	X	1	0	0	1
0	1	0	0	1	1	0	X	X	0	1	0
0	1	1	1	0	0	1	0	0	1	0	1
1	0	0	1	0	1	X	0	0	X	1	0
1	0	1	1	1	0	X	0	1	0	0	1
1	1	0	1	1	1	X	0	X	0	1	0
1	1	1	0	0	0	0	1	0	1	0	1

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	0_0	0_1	1_3	0_2
1	X_4	X_5	0_7	X_6

$S_A = \bar{Q}_A Q_B Q_C$

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	X_0	X_1	0_3	X_2
1	0_4	0_5	1_7	0_6

$R_A = Q_A Q_B Q_C$

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	0_0	1_1	0_3	X_2
1	0_4	1_5	0_7	X_6

$S_B = \bar{Q}_B Q_C$

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	X_0	0_1	1_3	0_2
1	X_4	0_5	1_7	0_6

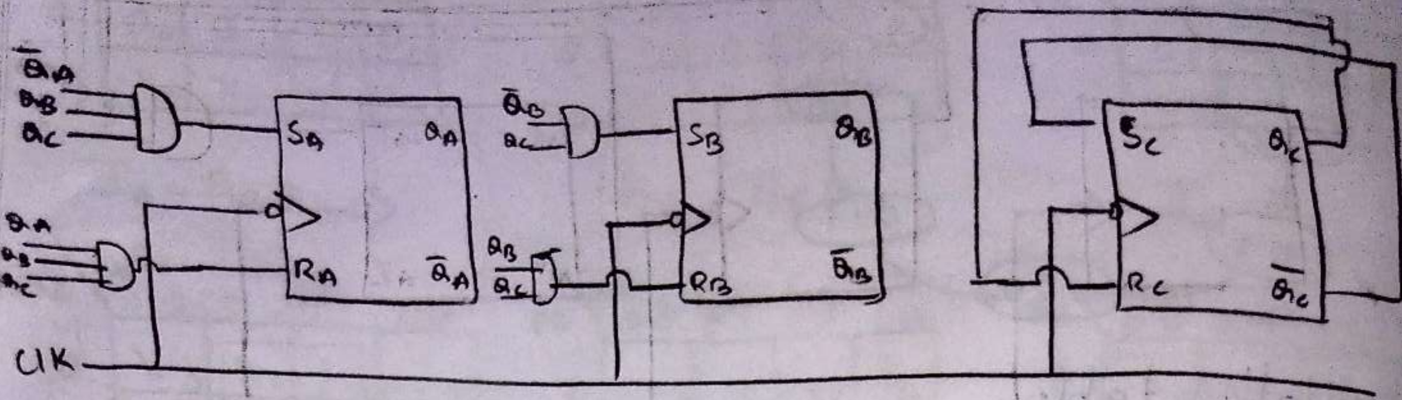
$R_B = Q_B Q_C$

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	1_0	0_1	0_3	1_2
1	1_4	0_5	0_7	1_6

$S_C = \bar{Q}_C \bar{Q}$

$Q_A \backslash Q_B Q_C$	00	01 ($\bar{Q}_B Q_C$)	11 ($Q_B Q_C$)	10
0	0_0	1_1	1_3	0_2
1	0_4	1_5	1_7	0_6

$R_C = Q_C$



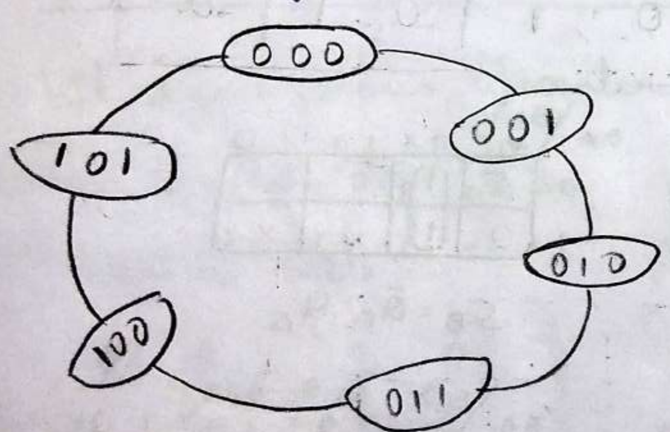
MOD-6 synchronous counter using JK & T flip flop :-

① No of flipflop : 3

② Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

③ State diagram :-



④ Circuit excitation table :-

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

0
1
2
3
4
5

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	0_0	0_1	1_3	0_2
1	X_4	X_5	X_7	X_6

$J_A = Q_B Q_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X_0	X_1	X_3	X_2
1	0_4	1_5	X_7	X_6

$K_A = \bar{Q}_B Q_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	0_0	1_1	X_3	X_2
1	0_4	0_5	X_7	X_6

$J_B = \bar{Q}_C \bar{Q}_A$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X_0	X_1	1_3	0_2
1	X_4	X_5	X_7	X_6

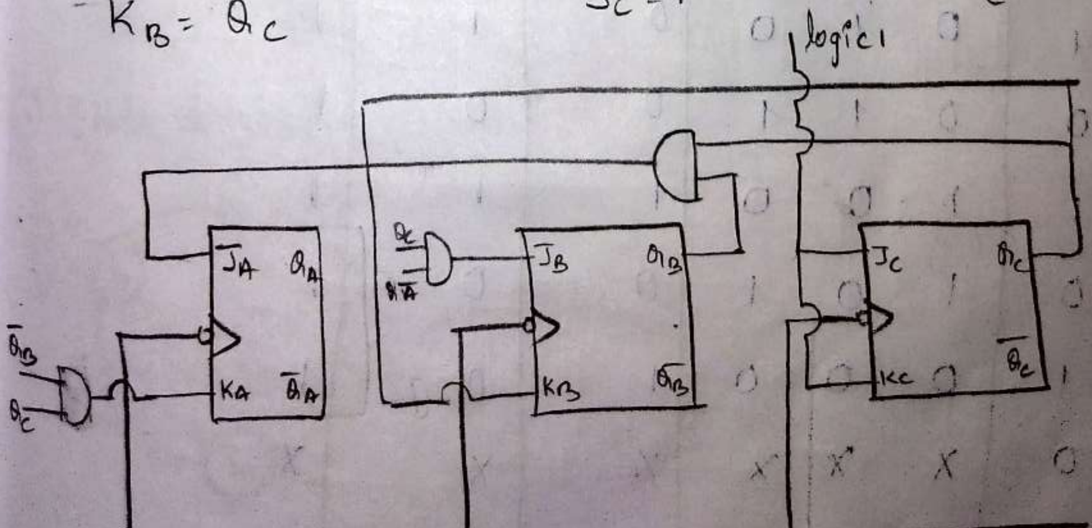
$K_B = Q_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	1_0	X_1	X_3	1_2
1	1_4	X_5	X_7	X_6

$J_C = 1$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X	1	1	X
1	X	1	X	X

$K_C = 1$



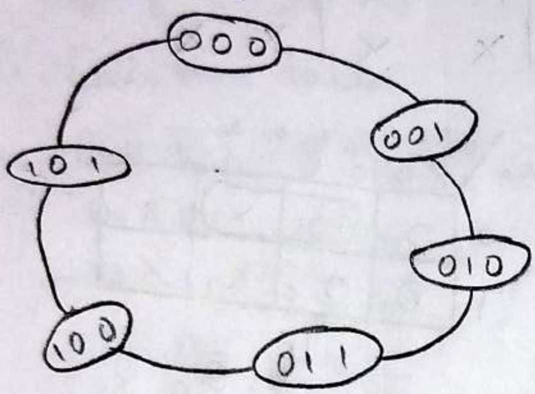
T - flip flop

① Number of flip flop :- 3

② Excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

③ State diagram :-



④ Circuit excitation table :-

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A ~~K_A~~	T_B ~~K_B~~	T_C ~~K_C~~
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	1	0	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	0_0	0_1	1_3	0_2
1	0_4	1_5	X_7	X_6

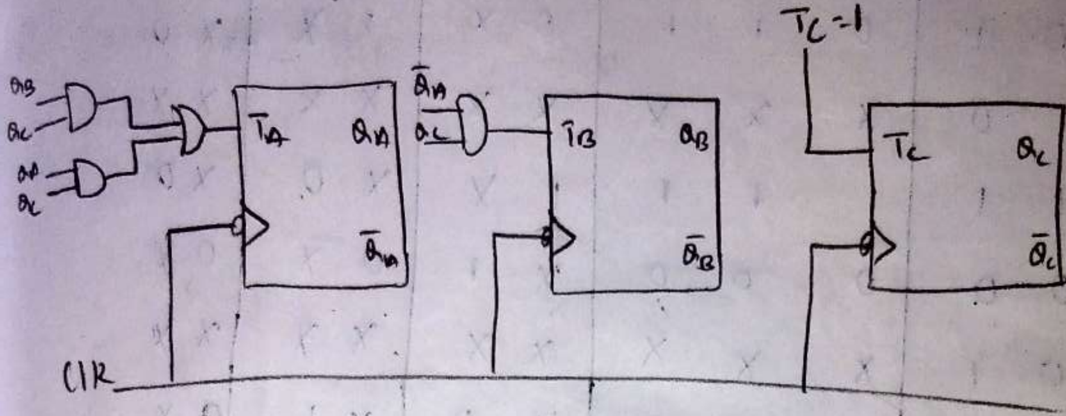
$T_A = Q_BQ_C + Q_AQ_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	0_0	1_1	1_3	0_2
1	0_4	0_5	X_7	X_6

$T_B = \bar{Q}_A Q_C$

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	1_0	1_1	1_3	1_2
1	1_4	1_5	X_7	X_6

$\therefore T_C = 1$



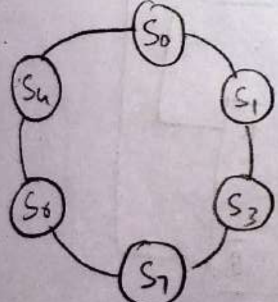
Design a counter with a sequence 0 1 3 7 6 4 0 using JK flip flop.

① No of flip flop :- 03

② Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

③ State diagram :-



Circuit excitation table.

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	0	X	X	X	X	X	X	X	X	X
0	1	1	1	1	1	1	X	X	0	X	0
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	1	0	0	X	0	X	1	0	X
1	1	1	1	1	0	X	0	X	0	X	1

K-map

Q_A \ Q_BQ_C	00	01	11	10
0	0_0	0_1	1_3	X_2
1	X_4	X_5	X_7	X_6

$J_A = Q_B$

Q_A \ Q_BQ_C	00	01	11	10
0	X_0	X_1	X_2	X_3
1	1_4	X_5	0_7	0_6

$K_A = \bar{Q}_B$

Q_A \ Q_BQ_C	00	01	11	10
0	0_0	1_1	X_3	X_2
1	0_4	X_5	X_7	X_6

$J_B = Q_C$

Q_A \ Q_BQ_C	00	01	11	10
0	X_0	X_1	0_3	X_2
1	X_4	X_5	0_7	1_6

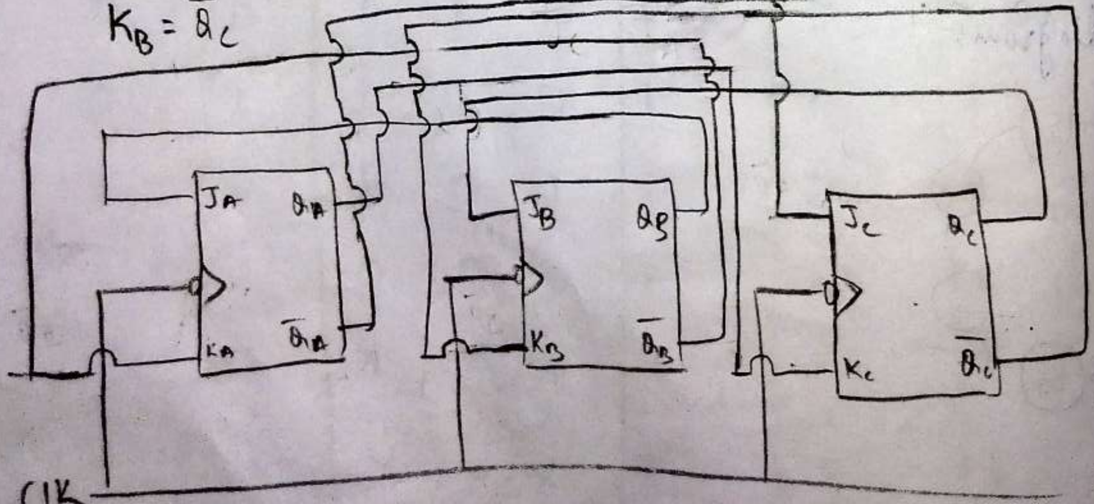
$K_B = \bar{Q}_C$

Q_A \ Q_BQ_C	00	01	11	10
0	1_0	X_1	X_3	X_2
1	0_4	X_5	X_7	0_6

$J_C = \bar{Q}_A$

Q_A \ Q_BQ_C	00	01	11	10
0	X_0	0_1	0_3	X_2
1	X_4	X_5	1_7	X_6

$K_C = Q_A$



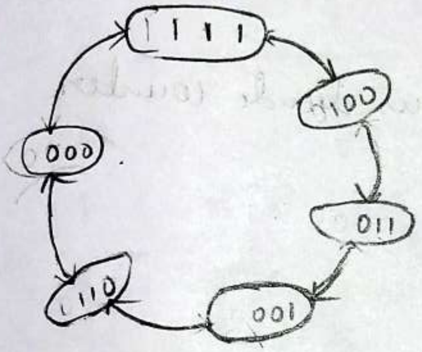
Design a synchronous counter using JK flip flop is count the sequence 7 4 3 1 6 0 7

① 3 flip flop

② Exitation table

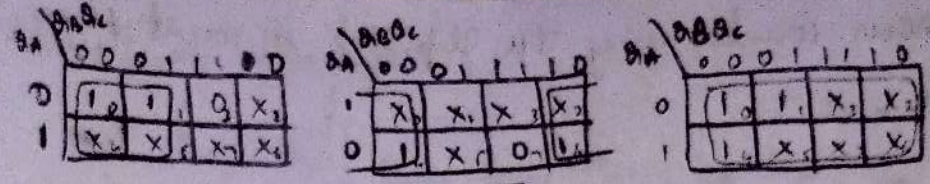
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

③ State diagram:-

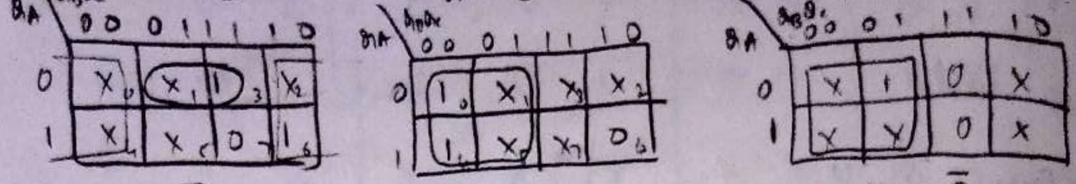


④ Circuit exitation table:-

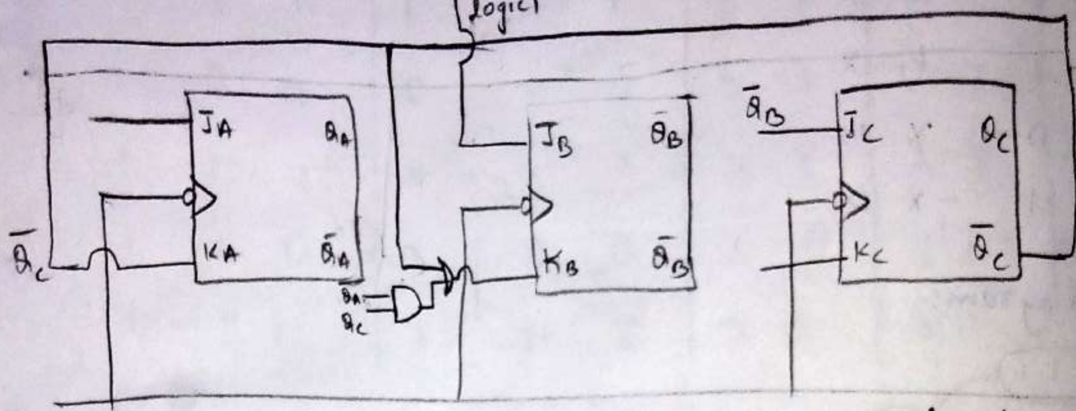
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	1	1	1	1	X	1	X	1	X
0	0	1	1	1	0	1	X	1	X	X	1
0	1	0	X	X	X	X	X	X	X	X	X
0	1	1	0	0	1	0	X	X	1	X	0
1	0	0	0	1	1	X	1	1	X	1	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	1	1	1	X	0	X	0	X	0



$J_A = \bar{Q}_B$ $\quad$ $K_A = \bar{Q}_C$ $\quad$ $J_B : 1$



$K_B = \bar{Q}_C + Q_A Q_C$ $\quad$ $J_C = \bar{Q}_B$ $\quad$ $K_C = \bar{Q}_B$



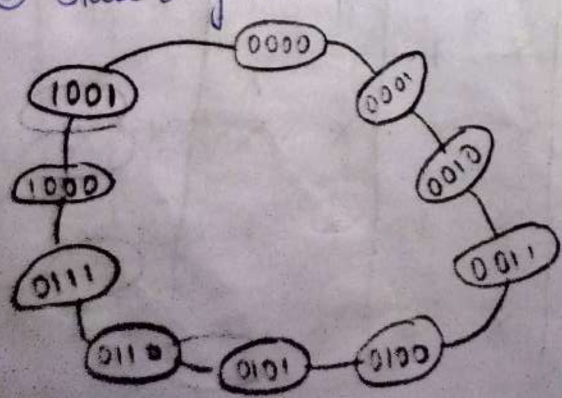
Design and implement ~~decade~~ synchronous decade counter using T flip flop

① No of flip flop :- 4

② Excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

③ State diagram :-



Q_A	Q_B	Q_C	Q_D	Q_{A+1}	Q_{B+1}	Q_{C+1}	Q_{D+1}	T_A	T_B	T_C	T_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X

$Q_AQ_B \backslash Q_CQ_D$	00	01	11	10
00	0_0	0_1	0_3	0_2
01 ($\bar{Q}_A Q_B$)	0_4	0_5	1_7	0_6
11 ($Q_A Q_B$)	X_{12}	X_{13}	X_{15}	X_{14}
10	0_8	1_9	X_{11}	X_{10}

$T_A = Q_C \bar{Q}_D Q_B + Q_A Q_D$

$Q_AQ_B \backslash Q_CQ_D$	00	01	11	10
00	0_0	0_1	1_3	0_2
01	0_4	0_5	1_7	0_6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	0_8	0_9	X_{11}	X_{10}

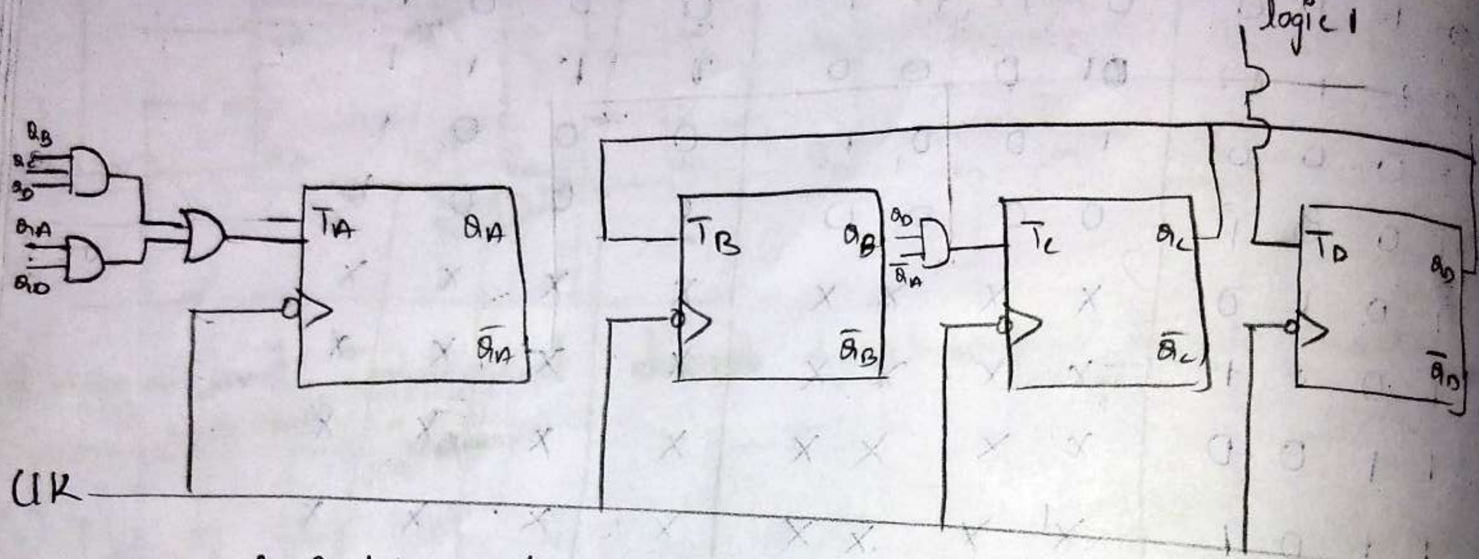
$T_B = Q_C Q_D$

$Q_AQ_B \backslash Q_CQ_D$	00	01	11	10
00	0_0	1_1	1_3	0_2
01	0_4	1_5	1_7	0_6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	0_8	0_9	X_{11}	X_{10}

$T_C = Q_D \bar{Q}_A$

$Q_AQ_B \backslash Q_CQ_D$	00	01	11	10
00	1_0	1_1	1_3	1_2
01	1_4	1_5	1_7	1_6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	1_8	1_9	X_{11}	X_{10}

$T_D = 1$



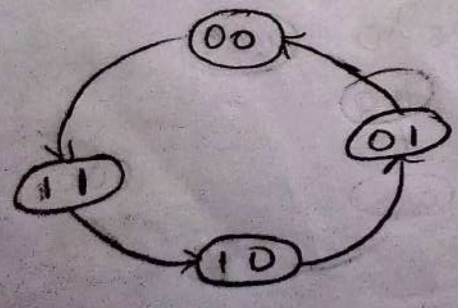
Design and implement MOD 4 synchronous down counter SR flip flop

① No of flip flop = 02

② Excitation table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

③ State diagram



Q_A	Q_B	Q_{A+1}	Q_{B+1}	S_A	R_A	S_B	R_B
0	0	1	1	1	0	1	0
0	1	0	0	0	X	0	1
1	0	0	1	0	1	1	0
1	1	1	0	X	0	0	1

$Q_A \backslash Q_B$	0	1
0	1	0
1	0	X

$S_A = \bar{Q}_A \bar{Q}_B$

$Q_A \backslash Q_B$	0	1
0	0	X
1	1	0

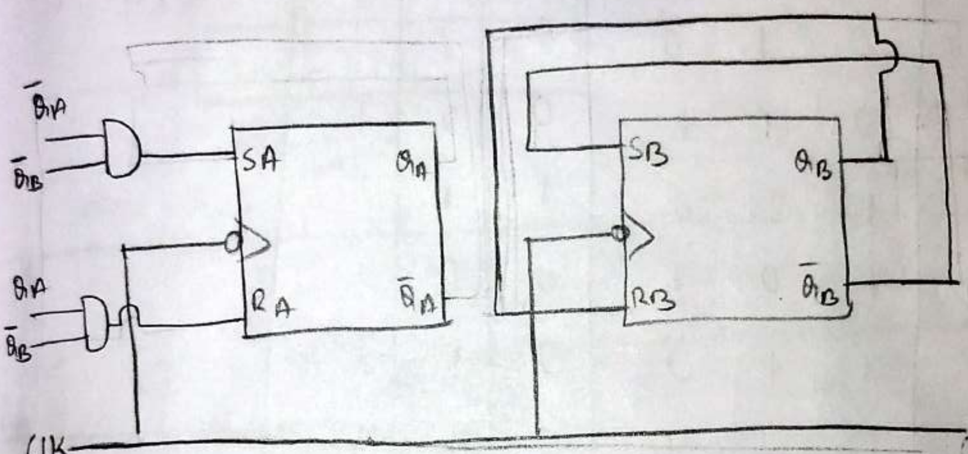
$R_A = Q_A \bar{Q}_B$

$Q_A \backslash Q_B$	0	1
0	1	0
1	1	0

$S_B = \bar{Q}_B$

$Q_A \backslash Q_B$	0	1
0	0	1
1	0	1

$R_B = Q_B$



3-bit up-down counter using T-flip flop :-

No of flip flop :- 3 4

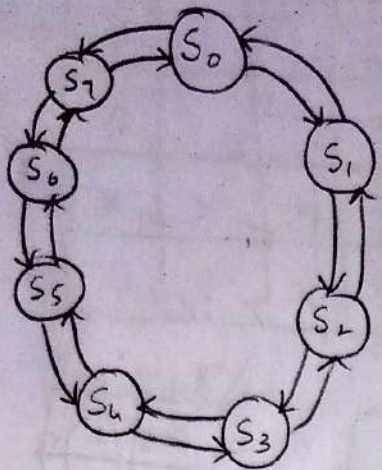
Excitation table :-

m=0 = up

m=1 = down

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

State diagram :-



M	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	0	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

MQ_A \ Q_BQ_C	00	01	11	10
$\bar{M}\bar{Q}_A$ 00	0	0	1	0
$\bar{M}Q_A$ 01	0	0	1	0
MQ_A 11	1	0	0	0
$M\bar{Q}_A$ 10	1	0	0	0

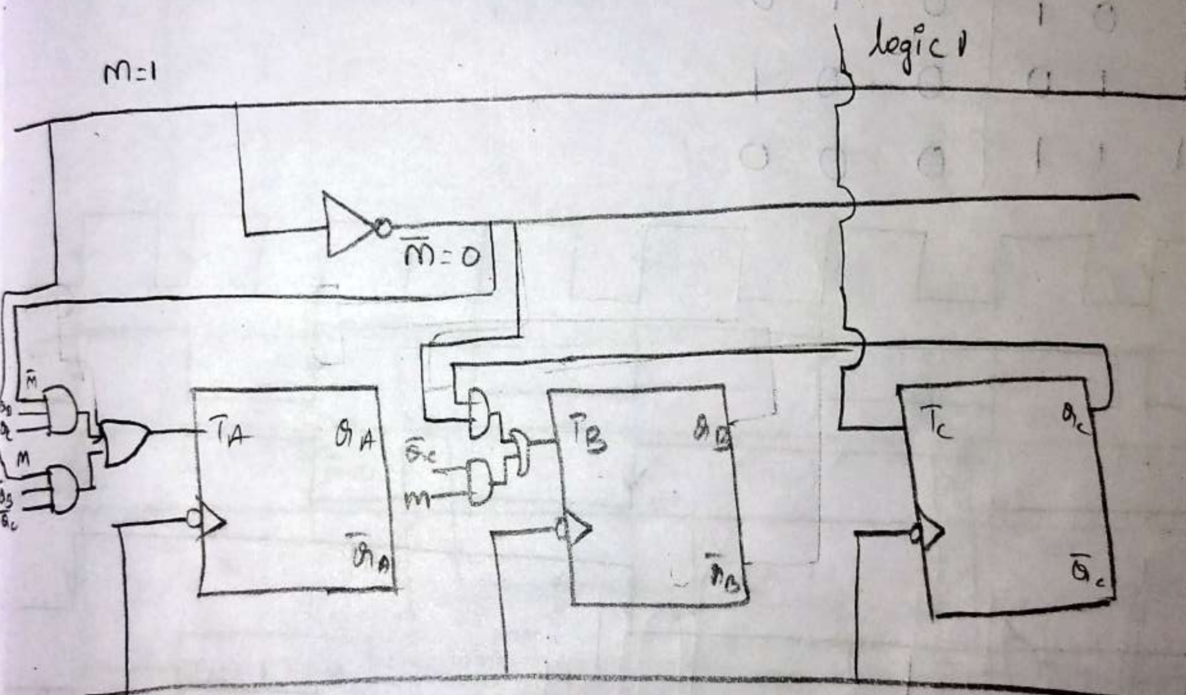
$$T_A = \bar{M}Q_BQ_C + \bar{Q}_B\bar{Q}_CM$$

MQ_A \ Q_BQ_C	$\bar{Q}_B\bar{Q}_C$ 00	$\bar{Q}_BQ_C$ 01	Q_BQ_C 11	$Q_B\bar{Q}_C$ 10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

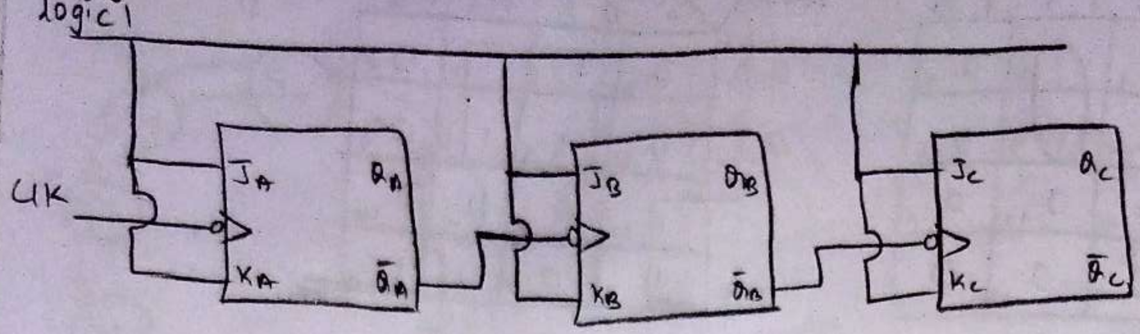
$$T_B = Q_C\bar{M} + \bar{Q}_CM$$

MQ_A \ Q_BQ_C	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

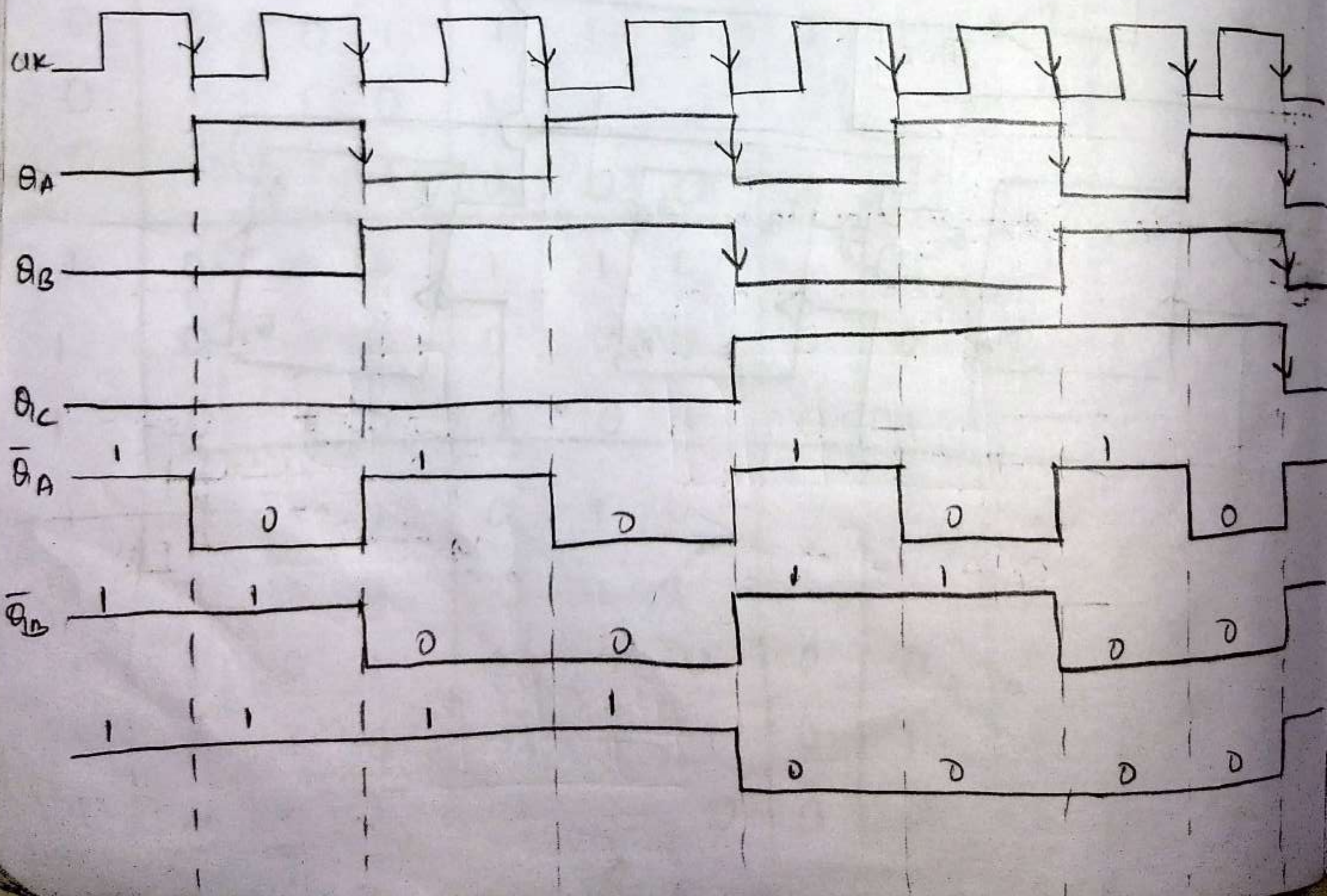
$$T_C = 1$$



3-bit Asynchronous downcounter:-



Q_A	Q_B	Q_C	$\bar{Q}_A$	$\bar{Q}_B$	$\bar{Q}_C$
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0



A 3-bit asynchronous up-down counter:

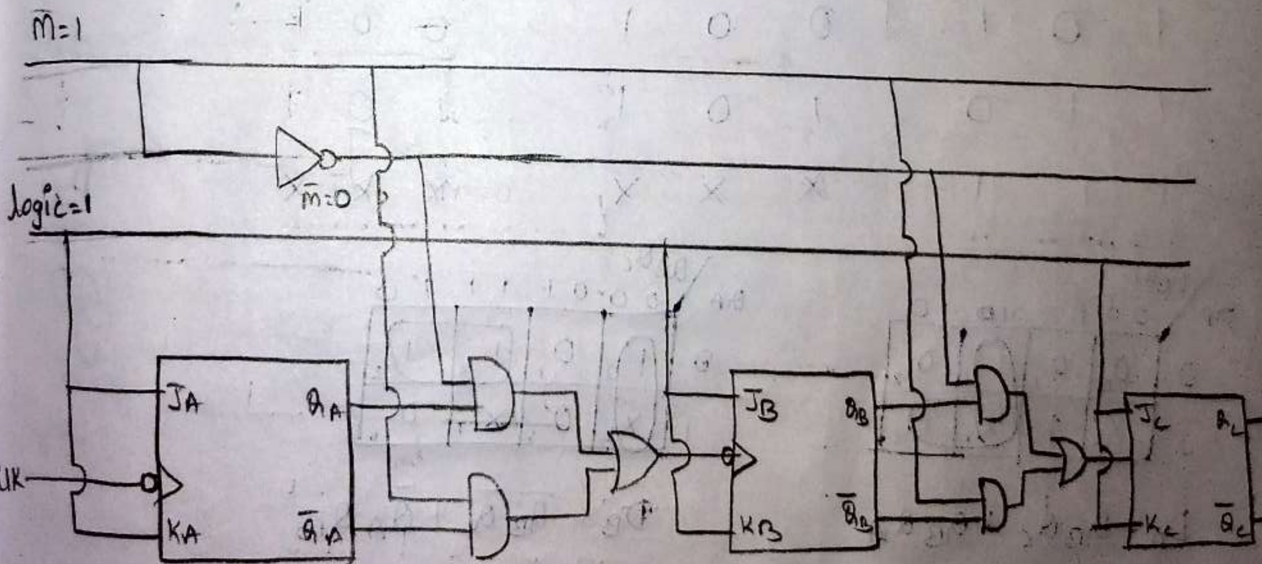
* A mode controller input 'M' is used to select either up (or) down mode.
* A combination circuit is required between each pair of flip flop.

M	Q	$\bar{Q}$	y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

M \ $Q\bar{Q}$	00	01	11	10
0	0_0	0_1	1_3	1_2
1	0_4	1_5	1_7	0_6

$$y = \bar{M} Q_A + M \bar{Q}_A$$

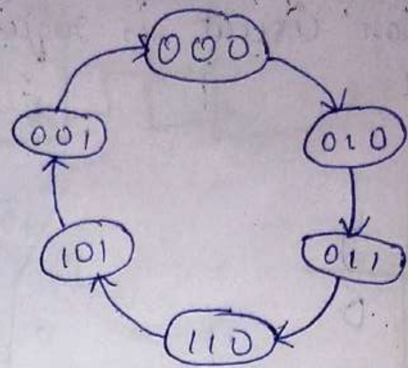
$$y = \bar{M} Q_B + M \bar{Q}_B$$



Design a asynchronous MOD-6 counter using D-flip flop to generate the sequence 0 2 3 6 5 1 0

No of F.F = 3

State diagram



Excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Circuit excitation table:-

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	D_A	D_B	D_C
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	0
0	1	0	0	1	1	0	1	1
0	1	1	1	1	0	1	1	0
1	0	0	X	X	X	X	X	X
1	0	1	0	0	1	0	0	1
1	1	0	1	0	1	1	0	1
1	1	1	X	X	X	X	X	X

Q_A \ Q_BQ_C	00	01	11	10
0	0_0	0_1	1_3	0_2
1	X_4	0_5	X_7	1_6

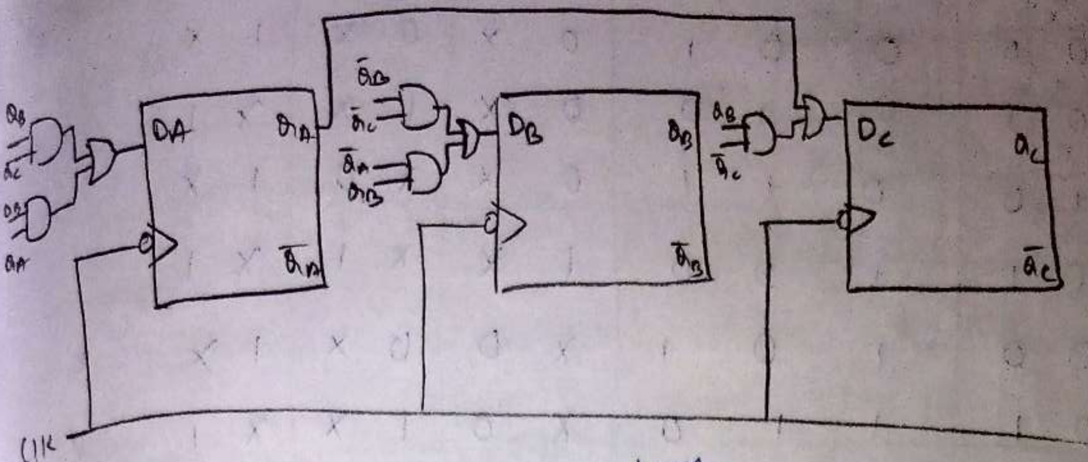
$D_A = Q_BQ_C + Q_BQ_A$

Q_A \ Q_BQ_C	00	01	11	10
0	1_0	0_1	1_3	1_2
1	X_4	0_5	X_7	0_6

$D_B = \bar{Q}_B\bar{Q}_C + \bar{Q}_AQ_B$

Q_A \ Q_BQ_C	00	01	11	10
0	0_0	0_1	0_3	1_2
1	X_4	1_5	X_7	1_6

$D_C = Q_A + Q_B\bar{Q}_C$



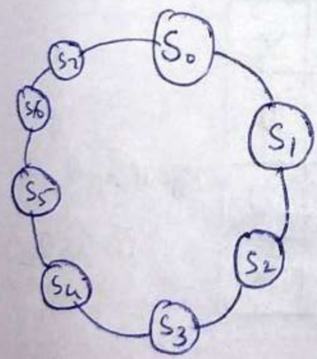
Realize 3 bit synchronous up-down-counter using J-K flipflop with transition table, logic diagram, include pre-set, clear-set.

No. of F.F = 3

Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

State diagram :-



M	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
up counter 0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	1
down counter 1	0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	1	0	0	0	0	X	0	X	X	1
1	0	1	0	0	0	1	0	X	X	1	1	X
1	0	1	1	0	1	0	0	X	X	0	X	1
1	1	0	0	0	1	1	X	1	1	X	1	X
1	1	0	1	1	0	0	X	0	0	X	X	1
1	1	1	0	1	0	1	X	0	X	1	1	X
1	1	1	1	1	1	0	X	0	X	0	X	1

$MQ_A \backslash Q_BQ_C$	00	01	11	10
00	0_0	0_1	1_3	0_2
01	X_4	X_5	X_7	X_6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	1_8	0_9	0_{11}	0_{10}

$J_A = M\bar{Q}_B\bar{Q}_C + \bar{M}Q_BQ_C$

$MQ_A \backslash Q_BQ_C$	00	01	11	10
00	X_0	X_1	X_3	X_2
01	0_4	0_5	1_7	0_6
11	1_{12}	0_{13}	0_{15}	0_{14}
10	X_8	X_9	X_{11}	X_{10}

$K_A = M\bar{Q}_B\bar{Q}_C + \bar{M}Q_BQ_C$

$MQ_A \backslash Q_BQ_C$	00	01	11	10
00	0_0	1_1	X_3	X_2
01	0_4	1_5	X_7	X_6
11	1_{12}	0_{13}	X_{15}	X_{14}
10	1_8	0_9	X_{11}	X_{10}

$J_B = M\bar{Q}_C + \bar{M}Q_C$

$MQ_A \backslash Q_BQ_C$	00	01	11	10
00	X_0	X_1	1_3	0_2
01	X_4	X_5	1_7	0_6
11	X_{12}	X_{13}	0_{15}	1_{14}
10	X_8	X_9	0_{11}	1_{10}

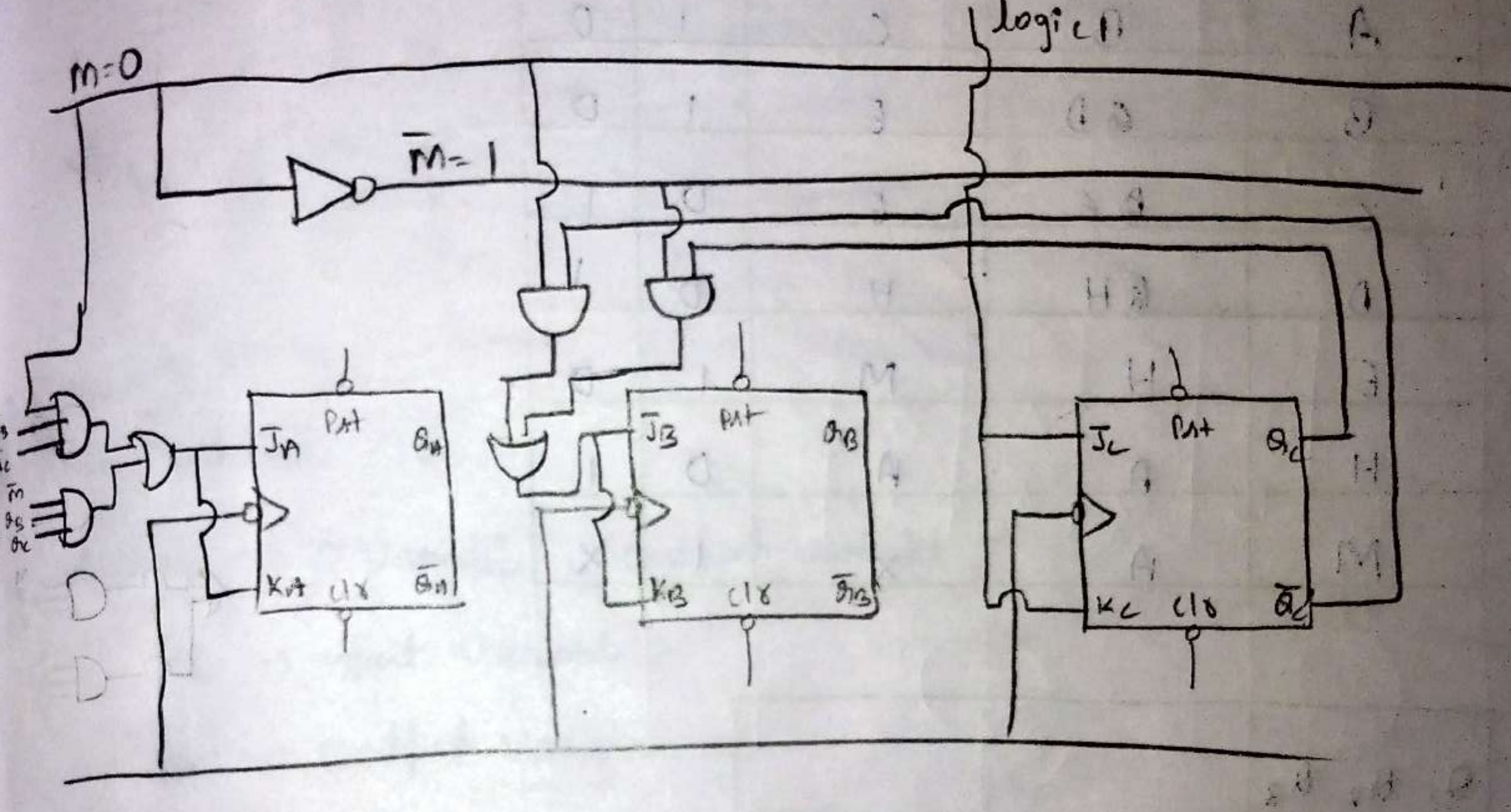
$K_B = M\bar{Q}_C + \bar{M}Q_C$

$MQ_A \backslash Q_BQ_C$	00	01	11	10
00	1_0	X_1	X_3	1_2
01	1_4	X_5	X_7	1_6
11	1_{12}	X_{13}	X_{15}	1_{14}
10	1_8	X_9	X_{11}	1_{10}

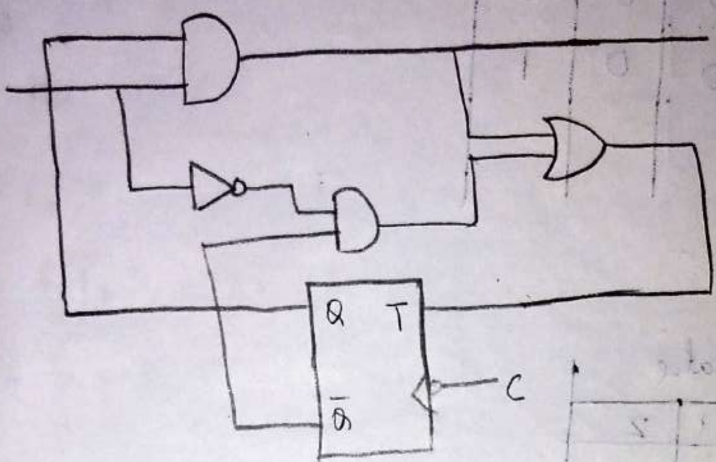
$J_C = 1$

$MQ_A \backslash Q_BQ_C$	00	01	11	10
00	X_0	1_1	1_3	X_2
01	X_4	1_5	1_7	X_6
11	X_{12}	1_{13}	1_{15}	X_{14}
10	X_8	1_9	1_{11}	X_{10}

$K_C = 1$



Consider the transition table, state table, state diagram for the Mealy's sequential circuit.



$Z = \alpha Q$

$T = \alpha Q + \bar{\alpha}\bar{Q}$

$0.1 + 1.0$

$0 + 0$

0

* Identify State Variable = Q

* Identify input variable & output variable

  $\alpha \rightarrow$ input variable

  $Z \rightarrow$ output variable.

* Write the equation

  $T = \alpha Q + \bar{\alpha}\bar{Q}$

  $Z = \alpha Q$

$Q^{+} \Rightarrow T = \alpha Q + \bar{\alpha}\bar{Q}$

$= 0.0 + 1.1$

$= 0 + 1$

$= 1$

* Excitation table

I/P Variable	Present state	Next state	F.F i/p	o/p variable
α	Q	Q^{+}	T	Z
0	0	1 ^{2nd}	1 ^{1st}	0
0	1	1	0	0
1	0	0	0	0
1	1	0	1	1

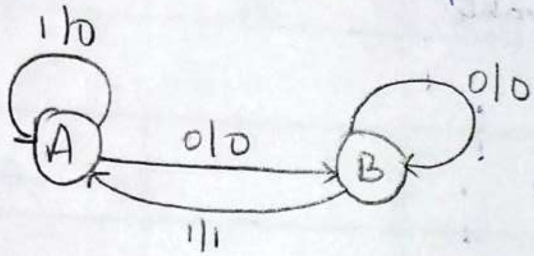
Transition table:-

Present state	Next state			
	$\alpha=0$	Z	$\alpha=1$	Z
Q	Q^+		Q^+	
A → 0	1	0	0	0
B → 1	1	0	0	1

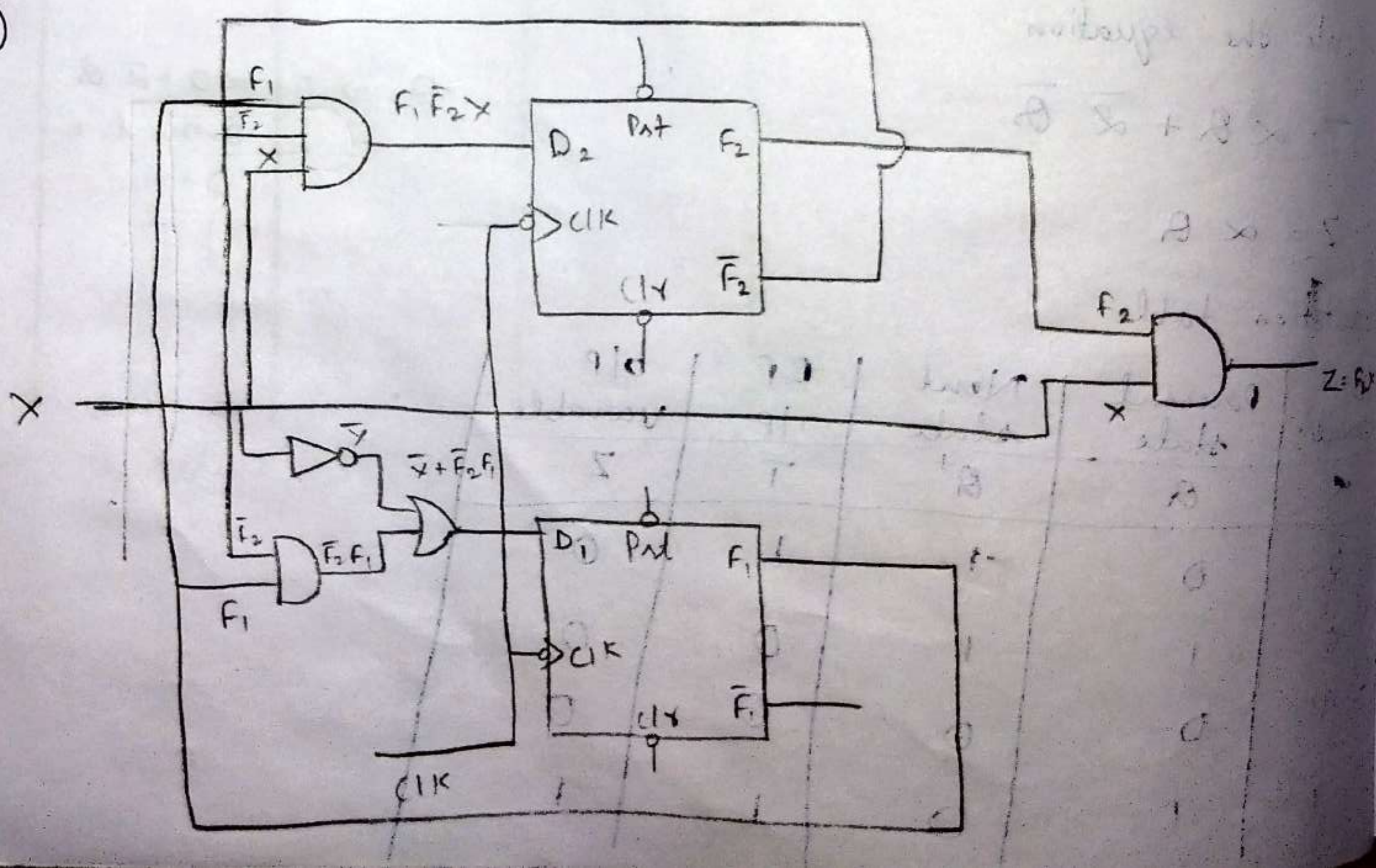
State table:-

P.S	Next state			
	$\alpha=0$	Z	$\alpha=1$	Z
A	B	0	A	0
B	B	0	A	1

State diagram:-



(2)



① State variable :- F_2, F_1

② i/p variable :- X

o/p variable :- Z

③ No of flip flop :- 2

④ write the equation

$$Z = F_2 X$$

$$D_2 = \underset{0}{F_1}\,\underset{1}{\bar{F_2}}\,\underset{0}{X}$$

$$D_1 = \underset{1}{\bar{X}} \underset{+}{+} \underset{1}{\bar{F_2}}\,\underset{0}{F_1}$$

⑤ Excitation table :-

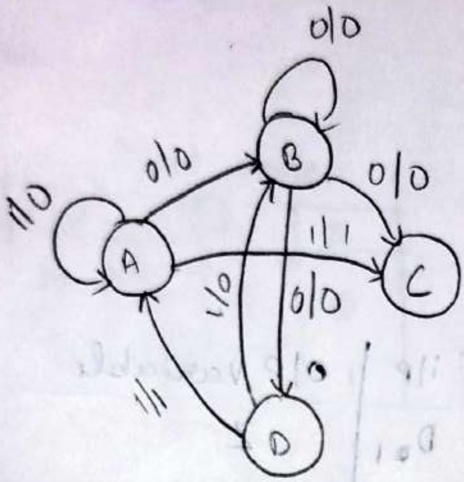
i/p variable	Present state		Next state		f.f i/p		o/p variable
X	F_2	F_1	F_2^+	F_1^+	D_2	D_1	Z
0	0	0	0	1	0	1	0
0	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0
0	1	1	0	1	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	0
1	1	0	0	0	0	0	1
1	1	1	0	0	0	0	1

Transition table :-

	P.S	N.S			
	$F_2\ F_1$	$F_2^+\ F_1^+$ $x=0$	Z	$x=1$	Z
	$F_2\ F_1$	$F_2^+\ F_1^+$		$F_2^+\ F_1^+$	
A	0 0	0 1	0	0 0	0
B	0 1	0 1	0	1 1	0
C	1 0	0 1	0	0 0	1
D	1 1	0 1	0	0 0	1

State table:-

P.S	N.S			
	$x=0$	Z	$x=1$	Z
A	B	0	A	0
B	B	0	D	0
C	B	0	A	1
D	B	0	A	1



MODULE : 05

BEHAVIORAL DESCRIPTION :

- The behavioral description describes the system by showing how the outputs behave according to changes in the inputs.
- In verilog, the major behavioral description statements are always and initial.

Verilog Behavioral description :

```
module half- add (I1, I2, O1, O2);
input I1, I2;
output O1, O2;
reg O1, O2;
/* Since O1 and O2 are outputs and they are
 written inside "always;" they should be
  declared as reg */
always @(I1,I2)
    begin
    #10 O1 = I1 ^ I2; // statement 1.
    #10 O2 = I1 & I2; // statement 2.
   /* The above two statements are procedural
 (inside always) signal- assignment statements with
10 simulation screen units delay */
  /* other behavioral (sequential) statements can be
                added here */

    end
  endmodule
```

In the above example;
All verilog statements inside always are treated as concurrent, the same as in the data-flow description. Any signal that is declared as an output should also be declared as a register (reg) if it appears inside always. O1 and O2 are declared outputs, so they should also be declared as reg.

IF Statement.

Syntax.

```
if (Boolean Expression)
begin
  Statement 1; /* if only One statement,
                  begin and End can be Omitted
                  Omitted */
  Statement 2;
  Statement 3;
  ......
End
Else.
begin
  Statement a; /* if only One statement,
                  begin and End can be
                  Omitted */
  Statement b;
  statement c;
  .....
End
```

Verilog 2x1 Multiplexer Using IF-ELSE

```
Module mux 2x1 (A, B, SEL, Gbar, Y);
input A, B, SEL, Gbar;
output Y;
reg Y;
always @ (SEL, A, B, Gbar)
begin
```

```
if (4bar == 1)
  Y = 1'bZ;
  Else
  begin.
    if (SEL)
    Y = B;
```

/* This is a procedural assignment. Procedural assignments are used to assign values to variables delared as regs (as Y here in this module). Procedural statement have to appear inside always, blocks, intial, tasks, or functions *)

```
    Else
    Y = A;
   End
 End
 Endmodule.
```

If-else:

```
if (Boolean Expression1)
begin
  Statement 1; Statement 2; ...
End
Else if (Boolean Expression2)
begin
  statement i; statementii
End
Else
begin
  statement a; statementb;
End.
```

Verilog 2x1 multiplexer using ELSE-IF

```
MODULE MUXBH (A, B, SEL, Gbar, Y);
input A, B, SEL, Gbar;
output Y;
reg Y; /* Since Y is an output and appears
       inside always, Y has to be declared
       as reg (register) */
always @ (SEL, A, B, Gbar)
begin
    Y=B;
End
Else if (Gbar == 0 & SEL == 0)
Y=A;
Else.
```

```
Y = 1'bz; // Y is assigned to high impedance
End
End module.
```

Case statement:-

→ The case statement is a sequential control statement.

Verilog case Format:

```
case ( control- expression)
test value1 : begin statements1 ; end
test value2 : begin statements2; end
test value3 : begin statements3; end
default : begin default statements end
endcase
```

Verilog Positive Edge-Triggered JK Flip-Flop Using Case:

```
module JK-FF (JK, clk, q, qb);
input [1:0] JK;
input clk;
output q, qb;
reg q, qb;
always @ (posedge clk)
begin
case (JK)
    2'd0 : q = q;
    2'd1 : q = 0;
  2'd2 : q = 1;
    2'd3 : q = ~q;
    endcase
  qb = ~q;
  end
endmodule
```

Behavioural description program for full adder:-

```
module fulladder (A, B, C, sum, carry)
input A, B, C
output sum, carry;
Reg (sum, carry);
always @ (A, B, C)
Begin
sum = A^B^C;
carry = (A&B) C (A^B)
End
Endmodule
```

MODULE - 04

Chapter 1: Introduction to Verilog system

Introduction :-

Hardware Description language [HDL] is a computer Aided Design [CAD] tool for the modern design and synthesis to digital system the recent, steady advances in semiconductor technology continue to increase the power and complexity of digital system Due to their complexity such system cannot be realized using discrete Integrated circuits [ICs]. They are usually realised using high density programmable chips such as Application Specific Integrated circuit (ASICs) and field programmable Gate Arrays [FPGAs] and require sophisticated CAD tools HDL is an Integral part of such tools HDL offers the designer a very Efficient tool for Implementing and synthesizing designs on chips.

Structure of the Verilog module :-

The Verilog module has a declaration and a body. In the declaration name, Input, and outputs of the module are listed The body shows the relationship between the inputs and outputs.

```
Module module_name (i/ps & o/ps);
  [Declaration parts]  -> i/ps and o/ps
  [Body]               -> relation b/w i/ps and o/ps.
Endmodule
```

Example of Verilog module :-

```
module half-adder (I1, I2, O1, O2);
input I1;
input I2;
Output O1;
Output O2;
// Blank lines are allowed
assign O1 = I1^I2;
assign O2 = I1 & I2;
Endmodule
```

The name of the module is the user selected half-adder. In contrast to VHDL Verilog is case sensitive. Half-adder, half-adder, and half_addEr are all different names. The name of the module should Start with an alphabetical letter and can include the special. character underscore (_). The declaration of the module starts with the predefined word module, followed by user selected name The names of the Inputs and outputs (i.e. the input and output ports) follow the same guidelines as the module's name They are written inside parentheses and are separated by commas. the closing ~~parth~~ parentheses is followed by a semicolon In I1, I2, O1, and O2 are the names of inputs and outputs. The order in which the input and output ports are written inside the parenthesis is Irrelevant we could have written the module statement as:

```
module half-adder (O1, I1, I2, O2);
```

Also more than one inputs or output could have been written on the same line by using a comma (,) to separate Each Input : for Example

```
module half-adder (I1, I2, O1, O2);
output O1, O2;
input I1, I2;
```

Statement 1 and 2 are signal assignment statement. in Statement 1, the symbol ^ represents an EXCULSIVE-OR operation; this symbol is called a logical operator so, Statement 1 describes the relationship b/w O1, I1 and I2 as;

O1 = I1 XOR I2.

In Statement 2. the symbol and represents AND logic it is also a logical operator So Statement 2 describes the relationship. b/w O2, I1 and I2 as; O2 = I1 AND I2. Accordingly Simulates a half adder. The double slashes (//) signal a comment command. If the comment takes more than one line, new double slashes can be used or the pair (/*...*/) can be. used to write a comment of any length.

Verilog ports:- Verilog ports can be one of the following three modes

Input :- The port is only an input port in any assignment Statement, the port should appear only on the right hand side of the Statement.

output :- The port is an output port In contrast to VHDL, the Verilog output port can appear on Either side of the assignment Statement.

Input and output (inout) The port can be used as both an Input and output The inout port represents a bidirectional bus

Operators :-
operators perform a wide Variety of functions these functions can be classified as:

logical :- Such as AND, OR, and XOR;

Relational:- to Express the relation b/w objects these operator include Equality, inequality, less than, less than or Equal, greater than and greater than or Equal;

Arithmetic:- Such as addition Subtraction multiplication, and division;

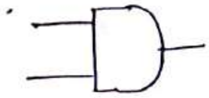
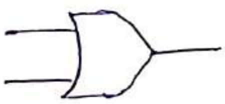
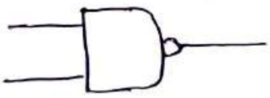
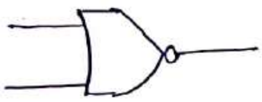
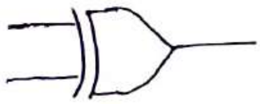
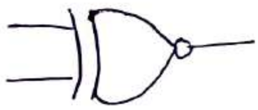
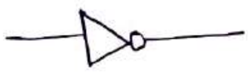
Shift:- To move the bits of an object in a ~~to~~ certain direction. Such as right or left.

1) Logical operators:- These operators perform logical operations such as AND, OR, NAND, NOR, NOT and EXCLUSIVE-OR the operation can be on two operand or on a single operand the operand can be single bit or multiple bits

Verilog logical operator :- Verilog has Extensive logical operators These operators perform logical operations such as AND, OR and EXCLUSIVE-OR Verilog logical operators can be classified into three groups :- Bitwise
Boolean logical
reduction

The bitwise operators are 111le to VHDL logical operators : they operate on the corresponding bits of two operands consider the Statement : z = X&Y ; where the AND operator (&) ANDs' the corresponding bits of X and Y and stores the result in Y For Example if X is the 4-bit signal 1011 and Y is the 4 bit signal 1010, then z = 1010 Shows bitwise logical operation on X and Y we write z = ~(X&Y). operator for Example, If we want to perform an NAND

Verilog Bitwise logical operators:

operator	Equivalent logic	operand type	Result type
&		Bit	Bit
|		Bit	Bit
~(&)		Bit	Bit
~(|)		Bit	Bit
^		Bit	Bit
~(^)		Bit	Bit
~		Bit	Bit

other types of logical operators are the Boolean logical operators these operators operate on two operands ; the result is Boolean, 0 (false) or 1 (true) for Example consider the statement z = X && Y where && is the Boolean logical AND operator if X = 1011 and Y = 0001 then z=1 . If X = 1010 and Y=0101 then Z = 0 if z = !X where ! is the negation operator and X=1111 then z=0 shows the Boolean logical operators

Verilog Boolean operators.

operator	operation	number of operands
&&	AND	two
||	OR.	two.

The third type of logical operator is the reduction operator These operators operate on a single operand the result is Boolean for Example in the statement $Y = \& X$, where & is the reduction AND operator and assuming $X = 1010$ then $Y = (1 \& 0 \& 1 \& 0) = 0$ Shows the reduction logic operators.

operator	operation	nos of operands.
&	Reduction AND.	one
|	Reduction OR	one
~(&)	Reduction NAND	one
~(|)	Reduction OR.	one
^	Reduction XOR.	one
~(^)	Reduction XNOR.	one
!	NEGATION	one

Relational operators :-

Relation operator are Implemented to Compare the Values of two objects the result returned by these Operators is Boolean that is false (0) or true (1).

Verilog Relation operator :-

Verilog has a set of relational operators ||le to VHDL As in VHDL the relational operators return Boolean Values false (0) or true (1)

For the Equality operator (==) and inequality operator (!=) the result can be of type unknown (X) if any of the operands include don't care or unknown (X); or

The following is an Example of a Verilog relational operator if (A==B)

Verilog relational operators.

operator	Description	Result type
==	Equality	0, 1, x
!=	In Equality	0, 1, x
===	Equality inclusive	0, 1
!==	In Equality inclusive	0, 1
<	less than	0, 1, X
<=	less than or Equal	0, 1, X.
>	Greater than	0, 1, X.
>=	Greater than or Equal.	0, 1, X.

If the value of A or B contain one or more 'don't care' or Z bits the value of the Expression is unknow otherwise if A Equal to. B. the value of the Expression is true (1) If A is not Equal to B, the value of the Expression is false (0).

if (A == B).

A or B can include X or Z;

This is a bit-by-bit comparison if all bits of A match that of B the result is true (1) otherwise the false (0)

3) Arithmetic operator:-

Arithmetic operator can perform a wide variety of operations such as addition, Subtraction multiplication and devision

Verilog Arithmetic operator:-

Verilog In contrast to VHDL is not an Extensive type oriented Languages Accordingly for most operation only one type of operation is Expected for Each operator to Illustrate the function of these operators consider the arithmetic operation Y := A (arithmetic operator) B. An Example of an arithmetic operator is the multiplication operator (*); the Statement Y := (A * B) calculates the values of Y as the the products of A time B

Verilog Arithmetic operator :-

operator	Description	A or B type.	Y type
+	Addition A+B	A numeric B numeric	numeric
−	Subtraction A − B	A numeric B numeric	numeric
*	multiplication A * B	A numeric B numeric	numeric
/	Division A / B	A numeric B numeric	numeric
%	modulus A % B	A numeric not real B numeric not real	numeric not real
**	Exponent. A**B	A numeric B numeric	numeric
{ , }	Concatenation	A numeric or array B numeric or array	Same as A.

Shift and Rotate operators :-

Shift and rotate operators are Implemented in many application such as in multiplication and division A shift left represents multiplication by two and a shift right represents division by two.

Verilog shift operator

Verilog Shift operators.

operation	description	operand A Before Shift	Operand A After Shift.
A <<1 ~~A<<2.~~	Shift A one position left logic	1110	110X.
A<<2	Shift A two position left logic	1110	10XX.
A>>1	Shift A one position right logical	1110	X111
A>>2	Shift A two position right logical	1110	XX11

Data type:-

Since HDL is Implemented to describe the hardware of a system the data or operands used in the language must have several types to match the need for describing the hardware for Example if we are describing a signal we need to specify its types (ie the values that the signal can take) such as type bit which means that the signal can assume only 0 or 1;

Verilog Data type:-

Verilog In contrast to VHDL does not Extensive data ty type. Verilog supports several data type Including

* nets
* registers
* Vectors
* Integer
* real
* parameters
* arrays

Nets :- Nets are declared by the predefined word wire nets have values that change continuously by circuit that the driving them Verilog supports four values for nets as

Verilog net Values

Value	Definition
0	logic 0 (false)
1.	Logic 1 (true)
X	unknown.
Z	high Impedance

Example:-

wire Sum ;

wire S1 = 1'b0;

The first statement declares a net by the name sum the Second Statement declars a net by the name S1; Its Initial value is 1'b0; which represents 1 bit with value 0.

~~more details on nets can be found~~ ?

Registors:-

Register in contrast to nets store values until they are updated Registers as their name suggests represent data storage Element. Register is declared by the predefined word reg. Verilog supports four values for register

Value	Definition
0	logic 0 (false)
1	logic 1 (true)
x	unknown.
z	Impedance.

An Example of a register is:

reg sum_total;

The above statement declares a register by the name sum_total.

Vectors:- Vectors are multiple bit A register or a net can be declared as a vector are declared by brackets [ ].

Example:

wire [3:0] a = 4'b1010;

reg [7:0] total = 8'd12;

The first statement declared a net a. It has 4 bits and Its Initial value is 1010 (b stands for bit) The second statement declares a register total Its size is 8 bits and its value is decimal 12 (d stands for decimal)

Integers

Integers are declared by the predefined word integer An Example of Integer declaration is :

integer no_bits;

The above Statement declares no_bits as an integers.

Real:- Real (floating point) numbers are declared with the Predefined word real Examples of real values 2.4, 56.3. and 5e12. the Value 5e12 is Equal to 5×10^{12} the following. Statement declares the register weight as real.

real weight ;

Parameters:-

Parameters represent global constant they are declared by predefined word parameter

Example:-

```
module compr_genr (x, y, xgty, x1ty, xegy);
Parameter N=3;
input [N:0] x, y;
output xgty, x1ty, xegy;
wire [N:0] sum, yb;
```

To changes the size of the inputs x and y and the size of the nets sum and yb to 8bits we just change the value of N as: parameter N=7;

Arrays :-

Verilog In contrast to VHDL does not have a predefined word for array Registers. and Integers can be written as arrays.

Example:- parameter N=3;

parameter m=2;

reg signed [m:0] carry [0:N];

reg [m:0] b [0:N];

integer sum [0:N];

The above statement declare an array by name sum. The array has five Elements and Each Element is an Integer type the array carry has five Element and Each Element Is 4 bits the 4 bits are in 2's complement form for Example if the value 9 a certain Element 1001 thus it is Equivalent to decimal -7. the array b has five Element of Each Element Is 4 bits the value of Each bit can be 0; 1, x, or z. Verilog does not support multi dimensional arrays.

Styles (Types) of Descriptions :-

classified as behavioral, structural, switch level, data flow, mixed type, mixed language.

1. Behavioral Descriptions :-

A behavioral description models the system as to how the o/p's behave with the i/p's. The definition of behavioral description is one where the module includes the predefined word always or initial.

Example of Behavioral Description [Verilog]

Half Adder :-

```
module HA (A, B, S, C)
input A, B;
output S, C;
reg S, C;  — (o/p's)
always @ (A, B)      → (always declare i/p's)
begin
Delay → { #10  S = A ^ B;
          #10  C = A & B;
End
Endmodule
```

2) Structural Descriptions:-

Structural descriptions model the System as Components or gates. This description is identified by the presence of the keyword Component in the module (Verilog) Such as (gates and, or, not.

Example of structural Description:- [Verilog]

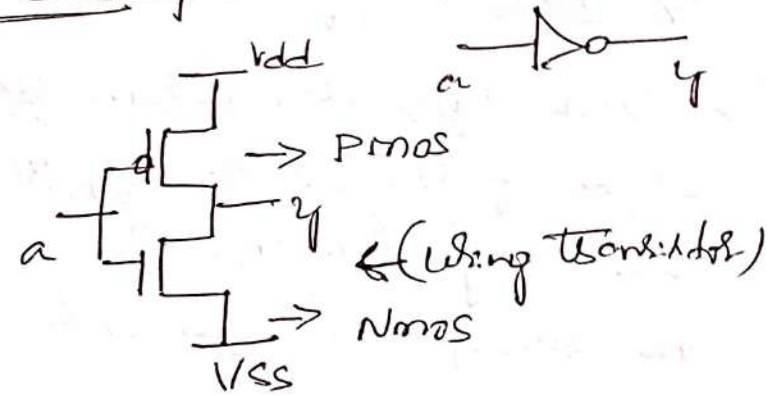
```
module HA (a, b, s, c)
input a, b;
output s, c;
  xor x1 (s, a, b);
// The above statement is Exclusive-OR gate
  and a1 (c, a, b);
// The above statement is AND gate
Endmodule
```

3) Switch-level Descriptions :-

The switch-level description is the lowest level of description. The System is described using switches or transistors. The Verilog Keywords nmos, pmos, cmos describe the System.

Example of Switch level Description :-

inverter :-




```
module invel (a, y)
input a;
output y;
Supply1 vdd;
Supply 0 gnd;
Pmos P1 (y, Vdd, a);
nmos n1 (y, gnd, a);
Endmodule
```

4) Data flow Descriptions :-

> Data flow describes how the System's signals flow from the inputs to the outputs. usually, the description is done by writing the Boolean function of the O/PS.

> The data-flow statements are Concurrent, their Execution is Controlled by Events.

Example of Data-flow Description :-

```
module HA (a, b, S, C)
input a, b;
output S, C;
assign S = a ^ b;
assign C = a & b;
Endmodule
```

5) Mixed - type Descriptions :-

→ Mixed- type descriptions use more than one type or style of the previously mentioned descriptions.

→ We may describe some parts of the system using one description type and other parts using another type.

Example of mixed-type Description [Verilog]

```
module ALU_mixed (a, b, Cin, opc, Z)
. . . . . . . . . . . . . . . . . . .
wire [2:0] g, P;
wire C0, C1;
// The following is data-flow description
  assign g[0] = a[0] & b[0];
  assign g[1] = a[1] & b[1];
  assign g[2] = a[2] & b[2];
  assign P[0] = a[0] | b[0];
  assign P[1] = a[1] | b[1];
. . . . . . . . . . . . . . . .
// The following is behavioral description
always @ (a, b, Cin, opc, temp1)
begin
   Case (OPC)
   . . . . . . . . . . . . .
   Endmodule
```

6] Mixed - language Descriptions :-

→ The mixed - language description is a newly added tool for HDL descriptions. The user now can write a module in one language (VHDL or Verilog) and invoke or import a construct (entity or module) written in the other language.

Example of mixed - language descriptions [Verilog]

```
module Full_Adder1 (X, Y, Cin, Sum, Carry)
 input X, Y, Cin;
 output Sum, Carry;
 wire C0, C1, S0;

HA H1 (Y, Cin, S0, C0);
// Description of HA is written in VHDL in the Entity HA
. . . . . . . . . . . . . . . . . . . . . .

Endmodule
library IEEE;
use ieee.std_logic_1164.all;
entity HA is
...for correct binding between this VHDL code & the
 above verilog code, the entity has to be named HA

 port (a, b: in std_logic; s, c: out std_logic);
 end HA;
 architecture HA_Dtflw of HA is
 begin
       s <= a xor b;
       c <= a and b;
   end HA_Dtflw;
```

Chapter 2:- Data flow Descriptions:-

Structure of the Data-flow Descriptions:-

module file name (i/p's & o/p's)

Declaration → i/p & o/p

Body → Relationship b/w i/p & o/p.

Endmodule

→ Data-flow descriptions simulate the system by showing how the signal flows from system inputs to outputs.

→ The above structure include 2 part one for input & o/p declaration and the other part is Body → Relationship between i/p & o/p.

Example of Data-flow Descriptions:-

Half Adder:-

```
module ~~HA~~ AND (a, b, y)
input a, b;
output y;
assign y = a & b;
Endmodule.
```

→ In this above Example State that the Code is describe by using module (System).

→ There are two inputs and Single o/p.

→ Statement are used to assign a value to the o/p y.

→ In Verilog [Data flow] using predefined word assign [assign a value].

Signal Declaration and Assignment statements :-

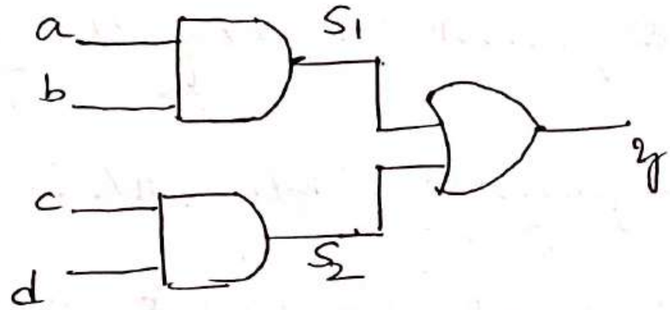


fig: AND-OR Ckt

→ The above figure shows that AND-OR ckt. Signals a, b, c and d are the inputs, signal y is the o/p, and signals S_1 and S_2 are intermediates.

→ Input & output Signals are declared in the module as ports. In HDL, a signal has to be declared before it can be used. Accordingly, signals S_1 and S_2 have to be declared.

→ In verilog, S_1 and S_2 are declared as signals by using the predefined word wire.

wire S_1, S_2;

→ By default, all ports in Verilog are assumed to be wires. The value of the wire is continuously changing with changes in the device that is driving it.
for Example, S_1 is the output of the AND gate in the above figure, and S_1 may change as a & b changes.

→ A signal-assignment statement is used to assign a value to a signal. The left-hand side of the statement should be declared as a signal. The right hand side can be a signal, a variable, or a constant. The operator for signal assignment in verilog is assign

Concurrent Signal-Assignment Statements:-

In HDL data-flow descriptions, concurrent signal-assignment statements constitute the major part of the body of verilog modules.

Example:- $S = a \wedge b$; statement 1
$c = a \& b$; statement 2

→ Concurrent Statement

Constant Declarations and Assignment Statements:-

→ A constant in HDL is treated as in C language; its value is constant within the segment of the program where it is visible.

→ A constant in verilog can be declared using the predefined word such as time or integer.

time period ;

→ To assign a value to a Constant, we use the assignment operator = in Verilog. For Example, to assign a value of 100 nanoseconds to the Constant period described above

period = 100 ; .

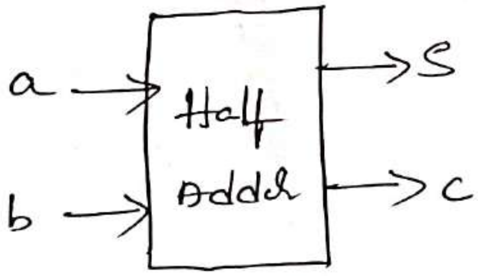
Assigning a Delay time to the Signal-Assignment Statement :-

→ To assign a delay time to a signal-assignment statement, we use the predefined word # in Verilog.

→ For Example, the following statement assign a 10-nanosecond delay time to signal S1.

assign #10 S1 = Sel & b // Verilog .

Verilog Code for Half Adder [Data flow Description]



Logic Symbol

I/p's		O/p's	
a	b	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table

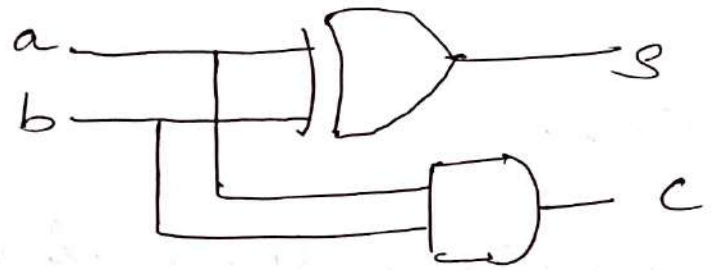
Boolean Expression: -

$S = a \oplus b$

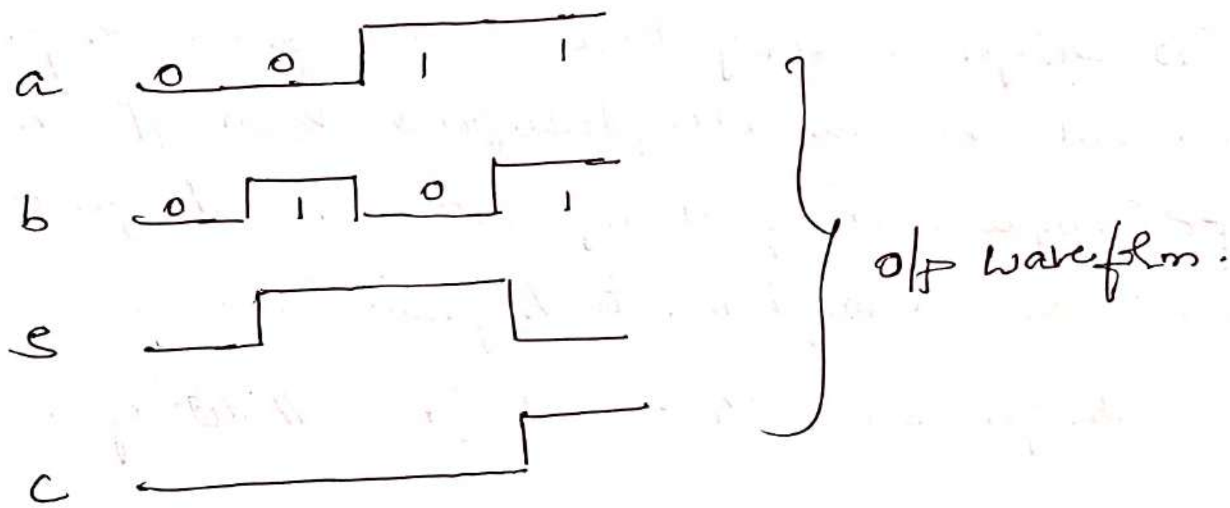
$C = a \cdot b$

In verilog: - $S = a \wedge b$

$C = a \& b$.



Logic diagram.



Verilog Code: -

```
module Half_Adder (a, b, s, c)
input a, b;
output s, c;
assign S = a ^ b;
assign c = a & b;
Endmodule
```

Verilog Code for 2X1 multiplexer with Active low Enable

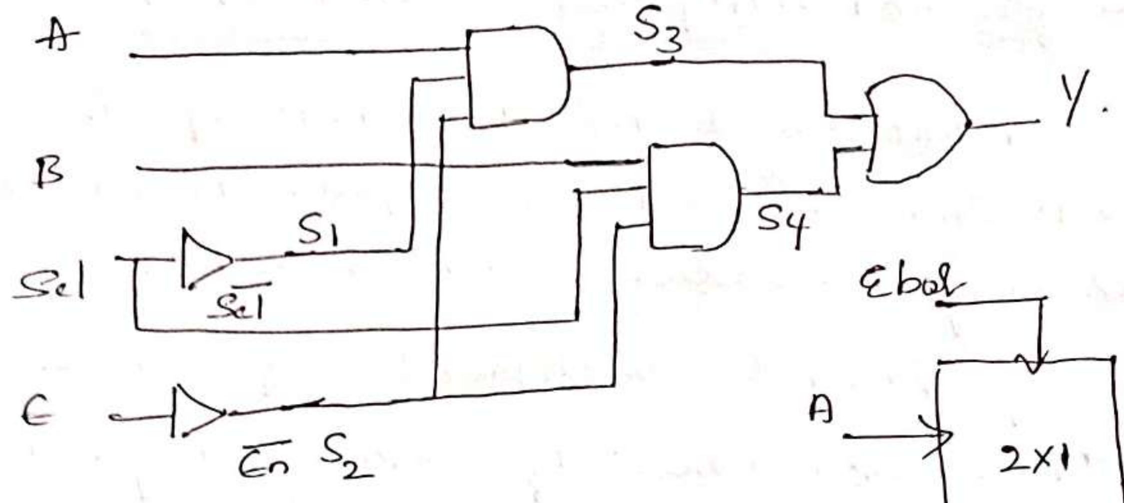
→ A basic 2X1 multiplexer has two 1-bit inputs, a 1-bit select line, and a 1-bit output. Additional control signals may be added, such as enable.

→ The output of the basic multiplexer depends on the level of the select line. If select is high (1), the o/p is equal to one of the two inputs, if select is low (0), the o/p is equal to the other i/p. A truth table for 2X1 mux with active low enable is shown in below truth table

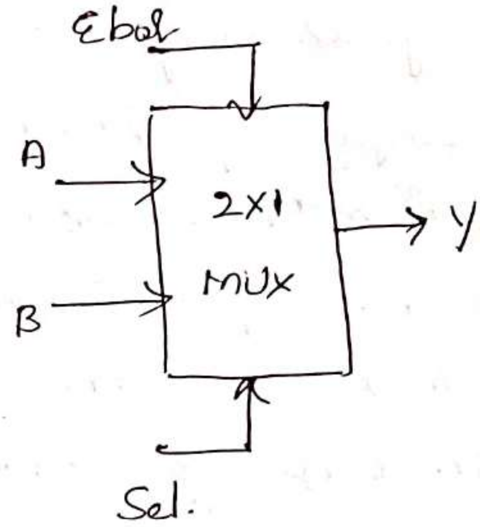
i/p		o/p
Sel	Ebar	y
X	H(1)	0
0	0	A
1	0	B

→ If enable (Ebar) is high (1), then the o/p is low(0), regardless of the i/p. When Ebar is low(0), the o/p is A if Sel is low(0), & the o/p is B if Sel is high(1).

$$Y = Ebar\,\overline{Sel}\,A + Ebar\,Sel\,B$$

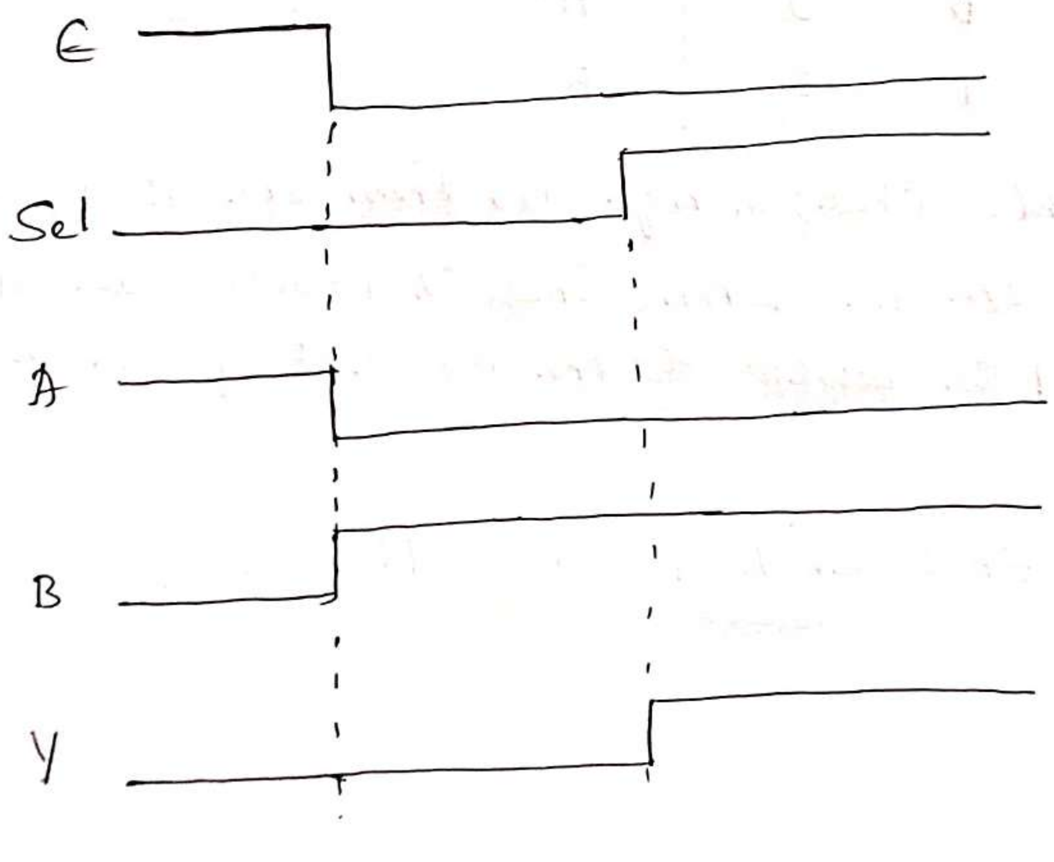


Logic diagram



Logic Symbol

output waveform:-



Verilog Code:-

```
module mux2x1 (A, B, SEL, Ebar, Y);
input A, B, SEL, Ebar;
output y;
wire S1, S2, S3, S4, S5;

assign #7 y = S3 | S4;
assign #7 S3 = A & S1 & S2;
assign #7 S4 = B & Sel & S2;
assign #7 S1 = ~Sel;
assign #7 S2 = ~En;
endmodule
```

Data type - Vectors :-

A vector is a data type that declares an array of similar elements, such as to declare an object that has a width of more than 1 bit.

```
wire a0, a1, a2, a3 ;    // Verilog
```

the vector declaration can be written as

```
wire [3:0] a;    // Verilog
```

[ ] in Verilog is a predefined operator that describes the width of the vector.

a[3] = 1, a[2] = 1, a[1] = 1, a[0] = 0.

The following declaration can be used

```
wire [0:3];    // Verilog.
```

Write a Verilog Code 2x2 unsigned Combinational Array multiplier

→ Consider the multiplication of a×b, where a and b are 2-bit numbers. The multiplication is done as follows.

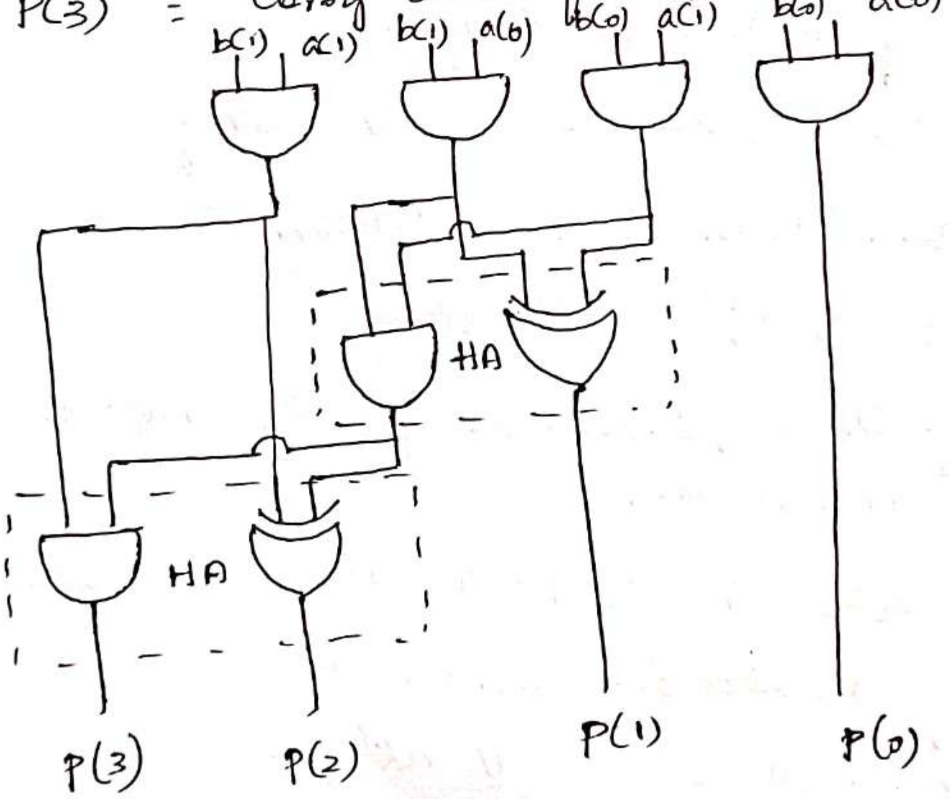
		a(1)	a(0)
		b(1)	b(0)
		b(0)×a(1)	b(0) × a(0)
	b(1)×a(1)	b(1) × a(0)	
P(3)	P(2)	P(1)	P(0)

P(0) = b(0) a(0)

P(1) = b(0) a(1) plus b(1) a(0)

P(2) = b(1) a(1) plus Carry out of P(1)

P(3) = Carry out of P(2)



Verilog 2x2 unsigned Combinational Array multiplier

```
module mul_array (a, b, P)
input [1:0] a, b;
output [3:0] P;
assign P[0] = a[0] & b[0];
assign P[1] = (a[0] & b[1]) ^ (a[1] & b[0]);
assign P[2] = (a[1] & b[1]) ^ ((a[0] & b[1]) & (a[1] & b[0]));
assign P[3] = (a[1] & b[1]) & ((a[0] & b[1]) & (a[1] & b[0]));
endmodule
```

Module 4

Feedback and Oscillator Circuits

4.1 Feedback Concepts

A typical feedback connection is shown in Fig. 4.1. The input signal V_s is applied to a mixer network, where it is combined with a feedback signal V_f . The difference of these signals V_{in} is then the input voltage to the amplifier. A portion of the amplifier output V_{out} is connected to the feedback network (β), which provides a reduced portion of the output as feedback signal to the input mixer network. If the feedback signal is of opposite polarity to the input signal, as shown in Fig. 4.1, negative feedback results. While negative feedback results in reduced overall voltage gain, but a number of improvements obtained are

1. Higher input impedance.

2. Better stabilized voltage gain.

3. Improved frequency response.

4. Lower output impedance.

5. Reduced noise.

6. More linear operation.

.

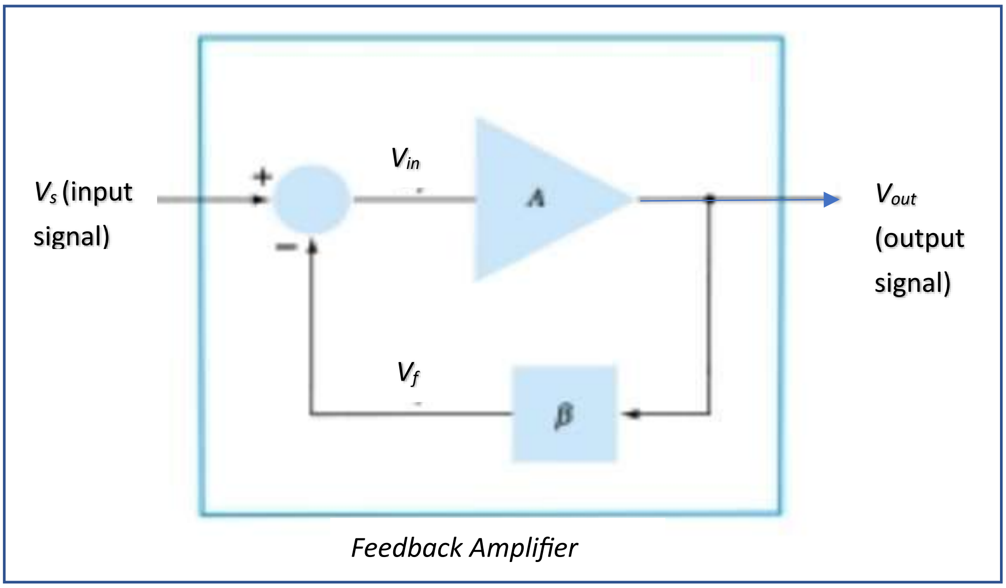
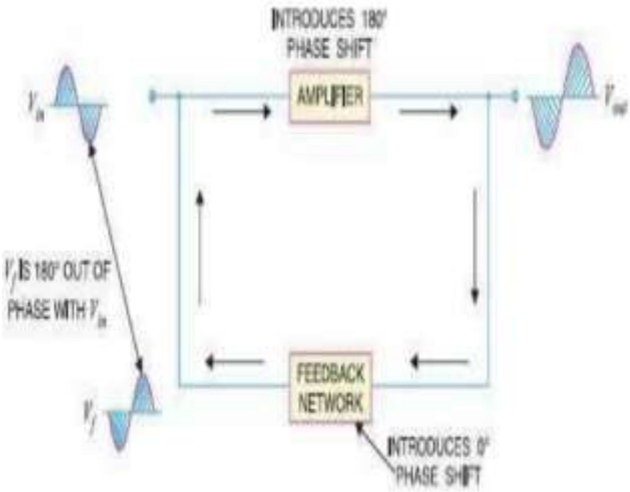


Fig 4.1: Simple Block Diagram of Feedback Amplifier



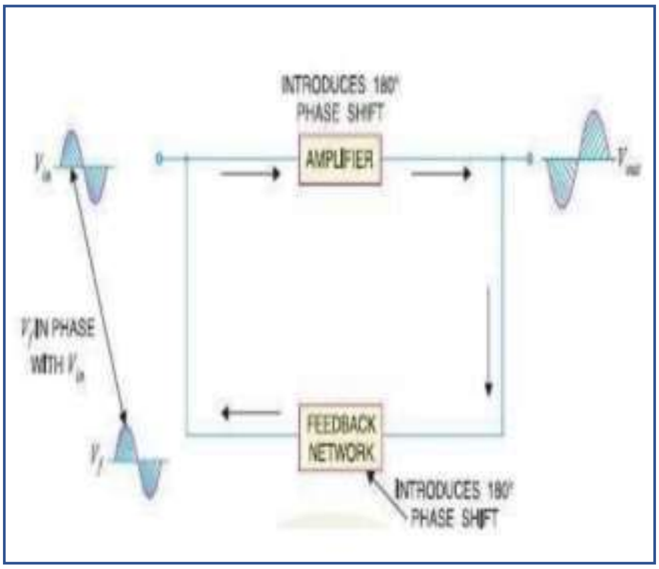


Fig 4.2(a): Negative Feedback **Fig 4.2(b): Positive Feedback**

The above figure 4.2(a) and 4.2(b) shows positive and negative feedback circuits.

If the feedback energy (voltage or currents), is **out of phase** with the input signal then it is **Negative feedback**. Negative feedback reduces gain of the amplifier. It also reduces distortion, noise and instability. This feedback increases bandwidth and improves input and output impedances. Due to these advantages, the negative feedback is frequently used in **amplifiers.**

If the feedback energy (voltage or currents), is **in phase** with the input signal then it is **positive feedback**. Positive feedback increases gain of the amplifier also increases distortion, noise and instability. Because of these disadvantages, positive feedback is not often used in amplifiers. But the positive feedback is used in **oscillators.**

4.2 Feedback Connection Types

There are four basic ways of connecting the feedback signal. Both voltage and current

can be fed back to the input either in series or parallel. Specifically, there are four types of feedback:

1. Voltage-series feedback.

2. Voltage-shunt feedback.

3. Current-series feedback.

4. Current-shunt feedback.

In the above mentioned four types

- ***voltage*** refers to connecting the output voltage as input to the feedback network;
- ***current*** refers to tapping off some output current through the feedback network.
- ***Series*** refers to connecting the feedback signal in series with the input signal voltage;
- ***shunt*** refers to connecting the feedback signal in shunt (parallel) with an input current source.

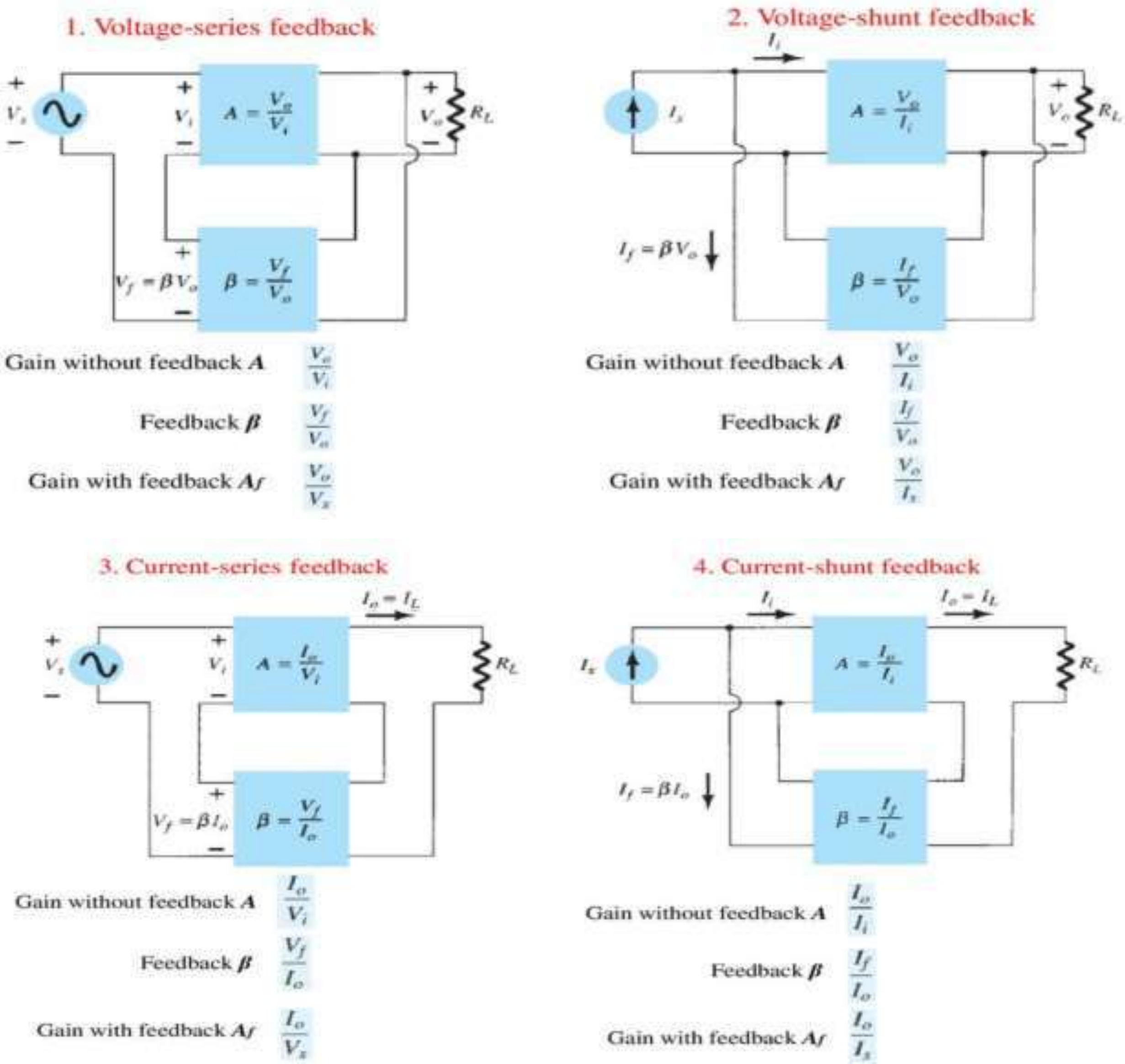


Fig 4.3: Feedback Connections

All four types of feedback connections are as shown in above figure 4.3.

Series feedback connections tend to ***increase*** the input resistance, while ***shunt*** feedback connections tend to ***decrease*** the input resistance. Voltage feedback tends to decrease the output impedance, while current feedback tends to increase the output impedance.

4.2.1 Gain with Feedback

The gain of each of the feedback circuit connections are examined in this section.

4.2.1.1 Voltage-Series Feedback

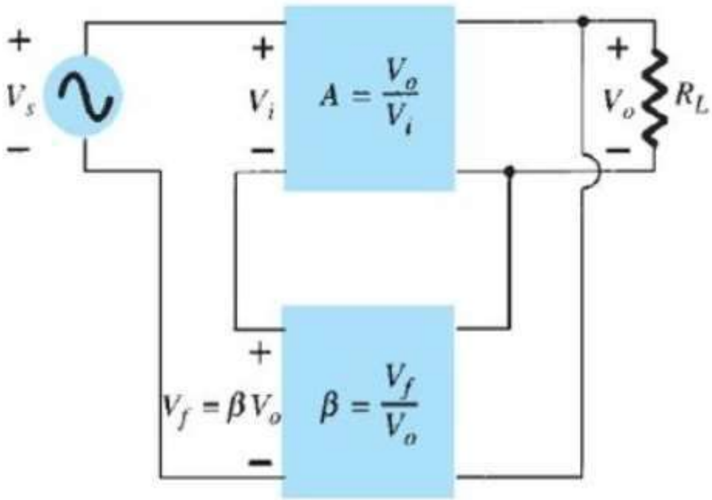


Fig 4.4: Voltage Series Feedback

Figure 4.4 shows the voltage-series feedback connection with a part of the output voltage(V_o) fed back in series with the input signal(V_s), resulting in an overall gain reduction. If there is no feedback (V_f), the voltage gain (A) of the amplifier stage is given by

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i} \qquad \text{.............. (4.1)}$$

If a feedback signal, V_f, is connected in series with the input, then

$$V_i = V_s - V_f$$

Since $\quad V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$

then $\quad (1 + \beta A)V_o = AV_s$

so that the overall voltage gain *with* feedback is

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}} \qquad \text{.............. (4.2)}$$

Equation (4.2) shows that the gain with feedback is the amplifier gain reduced by the factor (1+βA). This factor will be seen also to affect input and output impedance among other circuit features.

4.2.1.2 Voltage-Shunt Feedback

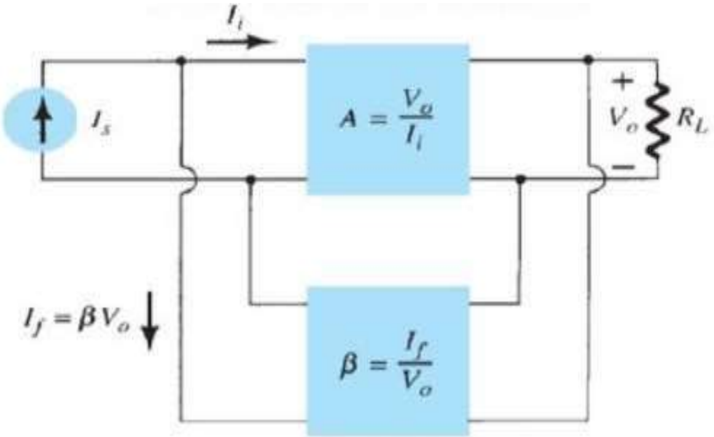


Fig 4.5: Voltage Shunt Feedback

Figure 4.5 shows the voltage-shunt feedback connection with a part of the output voltage (V_o) fed back in series with the input signal(I_s), if there is no feedback (I_f), the gain (A) of the amplifier stage is given by

$$A = \frac{V_o}{I_s} = \frac{V_o}{I_i} \quad \text{------} \cdot (4.3)$$

If the feedback signal I_f is connected as shown ~~parallel (shunt)~~ in Figure 4.5, then the gain of the feedback network is

$$A_f = \frac{V_o}{I_s} \quad \text{. - - . . - -} \cdot (4.4)$$

where $I_s = I_i + I_f$ {By applying KCL to node}

$$A_f = \frac{V_o}{I_i + I_f}$$

where $I_f = \beta V_o$

$$A_f = \frac{V_o}{I_i + \beta V_o}$$

where $V_o = A I_i$

$$A_f = \frac{V_o}{I_i + \beta A I_i} = \frac{V_o}{I_i(1+\beta A)} = \frac{A \cancel{I_i}}{\cancel{I_i}(1+\beta A)}$$

$$\boxed{A_f = \frac{A}{1+\beta A}} \quad \text{- - . . .} (4.5)$$

Equation (4.5) shows that the gain with feedback is the amplifier gain reduced by the factor (1+βA). This factor will be seen also to affect input and output impedance among other circuit features.

4.2.1.3 Current-Series Feedback

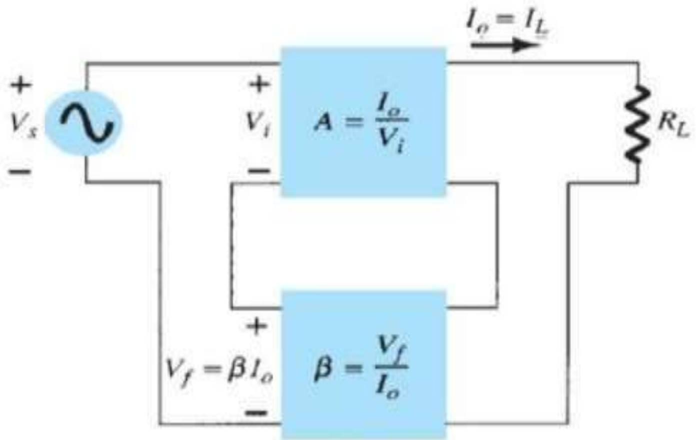


Fig 4.6: Current Series Feedback

Figure 4.5 shows the voltage-shunt feedback connection with a part of the output current (I_o) fed back in series with the input signal (V_s), if there is no feedback (V_f), the gain (A) of the amplifier stage is given by

$$A = \frac{I_o}{V_s} \,.\, \frac{I_o}{V_i} \quad \ldots\ldots (4.6)$$

If the feedback signal V_f is connected as shown in figure 4.6 then the gain of the feedback network is

$$A_f = \frac{I_o}{V_s} \quad \ldots\ldots (4.7)$$

where $V_s = V_i + V_f$ { from figure 4.6 }

$$A_f = \frac{I_o}{V_i + V_f}$$

where $V_f = \beta I_o$ from figure 4.6

$$A_f = \frac{I_o}{V_i + \beta I_o}$$

where $I_o = AV_i$ from equation 4.7

$$A_f = \frac{I_o}{V_i + \beta A V_i} = \frac{AV_i}{V_i + \beta A V_i}$$

$$= \frac{A\cancel{V_i}}{\cancel{V_i}(1+\beta A)}$$

$$\boxed{A_f = \frac{A}{(1+\beta A)}} \quad \ldots\ldots (4.8)$$

Equation (4.8) shows that the gain with feedback is the amplifier gain reduced by the factor (1+βA). This factor will be seen also to affect input and output impedance among other circuit features.

4.2.1.4 Current-Series Feedback

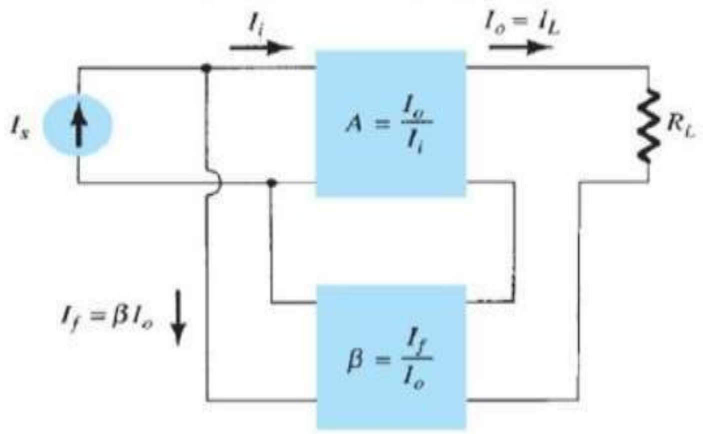


Fig 4.7: Current Shunt Feedback

Figure 4.5 shows the voltage-shunt feedback connection with a part of the output current (I_o) fed back in series with the input signal (I_s), if there is no feedback (I_f), the gain (A) of the amplifier stage is given by

$$A = \frac{I_o}{I_s} = \frac{I_o}{I_i} \quad \text{.....(4.9)}$$

If the feedback signal I_f is connected as shown in figure 4.7 then the gain of the feedback network is

$$A_f = \frac{I_o}{I_s} \quad \text{.....(4.10)}$$

where

$$I_s = I_i + I_f \quad \{\text{By applying KCL at node}\}$$

$$A_f = \frac{I_o}{I_i + I_f}$$

where $I_f = \beta I_o$ from figure 4.7

$$A_f = \frac{I_o}{I_i + \beta I_o}$$

where $I_o = A I_i$ from Equation 4.9

$$A_f = \frac{A I_i}{I_i + \beta A I_i} = \frac{A \cancel{I_i}}{\cancel{I_i}(1+\beta A)}$$

$$\boxed{A_f = \frac{A}{(1+\beta A)}} \quad \text{.....(4.11)}$$

Equation (4.11) shows that the gain with feedback is the amplifier gain reduced by the factor (1+βA). This factor will be seen also to affect input and output impedance among other circuit features.

4.2.2 Input Impedance and Output Impedance

The input and output impedance of each of the feedback circuit connections are examined in this section.

4.2.2.1 Voltage-Series Feedback

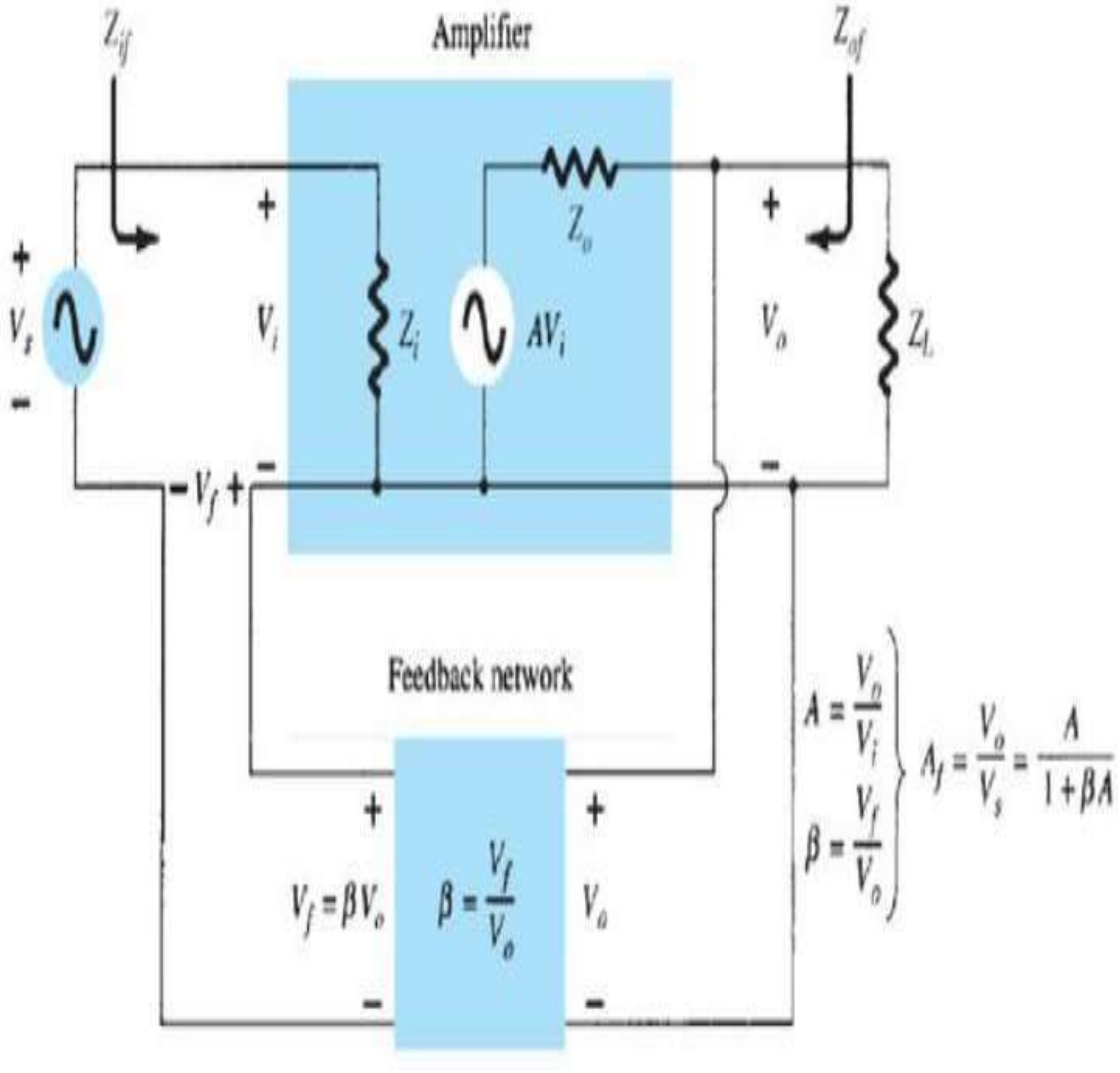


Fig 4.8: Voltage Series Feedback Connection

From the equation 4.16 the input impedance with voltage series feedback is seen to be the value of the input impedance without feedback multiplied by the factor ($1+\beta A$).

Consider the Voltage-series feedback connection shown in figure 4.8,

(i) The Input impedance can be determined as follows:

W.K.T The input current I_i is given by,

$$I_i = \frac{V_i}{Z_i} \quad \ldots (4.12)$$

where $V_i = V_s - V_f$

$$V_f = \beta V_o$$

Therefore $V_i = V_s - \beta V_o \quad \ldots (4.13)$

Substitute equation 4.13 in 4.12 to get input impedance Z_{if}.

$$Z_i = \frac{V_i}{I_i} = \frac{V_s - \beta V_o}{I_i}$$

$$Z_i I_i = V_s - \beta V_o \quad \ldots (4.14)$$

where $V_o = A V_i = A Z_i I_i \quad \ldots (4.15)$

Substitute ean 4.15 in (4.14) we get

$$Z_i I_i = V_s - \beta A Z_i I_i$$

$$Z_i I_i + \beta A Z_i I_i = V_s$$

$$Z_i I_i (1 + \beta A) = V_s$$

$$\frac{V_s}{I_i} = Z_i (1 + \beta A)$$

$$\boxed{Z_{if} = Z_i (1 + \beta A)} \quad \ldots 4.16$$

Z_{if} is the input impedance with feedback.

(ii) The output impedance for voltage series feedback can be determined as follows:

Applying KVL at o/p side in figure 4.8 we get,

$$V_o = AV_i + IZ_o \quad \cdots (4.17)$$

where

$$V_i = -V_f = -\beta V_o$$ ← {To find o/p impedance V_s is set to zero}

$$V_o = IZ_o + A(-\beta V_o)$$

$$V_o = IZ_o - A\beta V_o$$

$$IZ_o = (V_o + A\beta V_o)$$

$$IZ_o = V_o(1 + A\beta)$$

$$\frac{V_o}{I} = \frac{Z_o}{(1+A\beta)}$$

$$\boxed{Z_{of} = \frac{Z_o}{1+A\beta}} \quad \cdots (4.18)$$

where

Z_i → Input Impedance without feedback

Z_{if} → Input Impedance with feedback

Z_o → output Impedance without feedback

Z_{of} → output Impedance with feedback

The output impedance gets reduced by the factor of $(1+\beta A)$ in voltage series feedback connection.

4.2.2.1 Voltage-Shunt Feedback

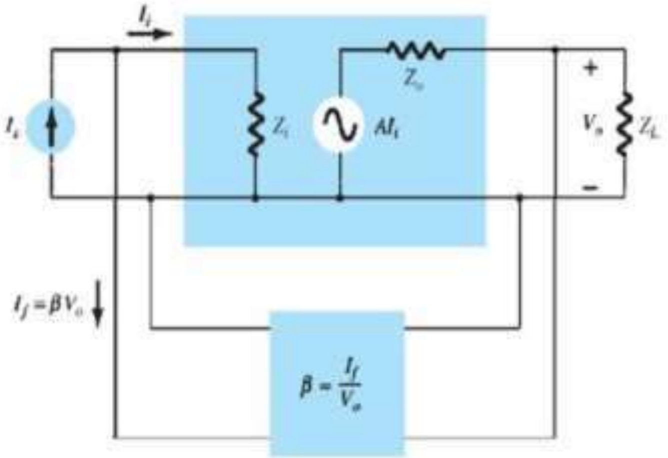


Fig 4.9: Voltage Shunt Feedback Connection

Consider the Voltage-Shunt feedback connection shown in figure 4.9.

(i) The input impedance can be determined as follows:

The input impedance with feedback is given by,

$$Z_{if} = \frac{V_i}{I_s} \quad \dots\dots (4.17)$$

where $I_s = I_i + I_f$

$$Z_{if} = \frac{V_i}{I_i + \beta V_o} \quad \dots\dots (4.18)$$

Dividing numerator & denominator by I_i

$$Z_{if} = \frac{\frac{V_i}{I_i}}{\frac{I_i}{I_i} + \frac{\beta V_o}{I_i}} = \frac{Z_i}{1 + \beta \frac{V_o}{I_i}}$$

From figure $\frac{V_o}{I_i} = A$

$$\boxed{Z_{if} = \frac{Z_i}{(1+\beta A)}} \quad \dots\dots (4.19)$$

The input impedance gets reduced by the factor of $(1+\beta A)$ in the voltage shunt feedback connection.

(ii) The output impedance for voltage shunt feedback can be determined as follows:

Apply KVL at O/p side in figure 4.9,

$$V_o = IZ_o + AI_i \quad \cdots\cdots (4.19)$$

set $V_s = 0$, & $I_s = 0$ so that

$$I_s = I_i + I_f$$

$$I_i = -I_f = -\beta V_o \quad \cdots\cdots (4.20)$$

Substitute (4.20) in Eqn (4.19) we get

$$V_o = IZ_o - A\beta V_o$$

$$IZ_o = (V_o + A\beta V_o)$$

$$IZ_o = V_o(1+A\beta)$$

$$\frac{V_o}{I} = \frac{Z_o}{(1+A\beta)}$$

$$\boxed{Z_{of} = \frac{Z_o}{1+A\beta}} \quad \cdots\cdots (4.21)$$

The output impedance gets reduced by the factor of $(1+\beta A)$ in voltage shunt feedback connection.

4.2.2.3 Current Series Feedback

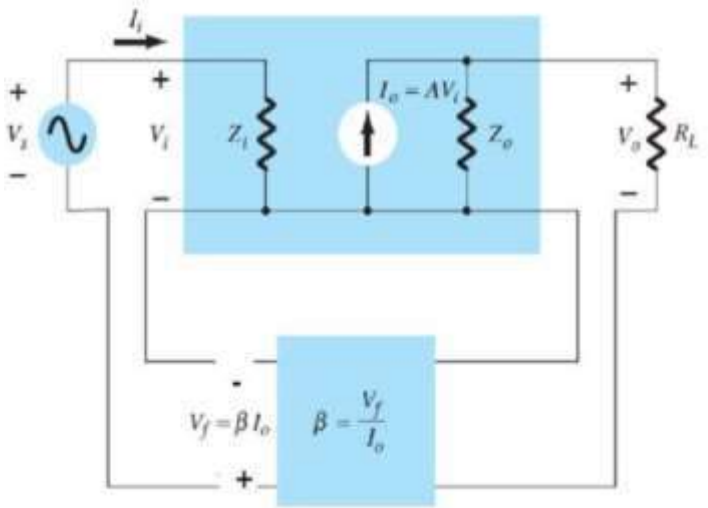


Fig 4.10: Current Series Feedback Connection

Consider the current series feedback connection shown in Figure 4.10,

(i) The input impedance can be determined as follows:

W.K.T The input impedance Z_i is given by,

$$Z_i = \frac{V_i}{I_i} \quad \text{.....(4.22)}$$

From Figure,

$$\beta = \frac{V_f}{I_o} \quad \text{--(a)}$$

$$V_f = \beta I_o \quad \text{-(b)}$$

where $V_i = V_s - V_f$

$$V_i = V_s - \beta I_o \quad \text{--(4.23)}$$

$$Z_i = \frac{V_s - \beta I_o}{I_i}$$

$$Z_i I_i = V_s - \beta I_o$$

where $I_o = AV_i$

and $V_i = Z_i I_i$

$$Z_i I_i = V_s - \beta A V_i = V_s - \beta A Z_i I_i$$

$$V_s = Z_i I_i + \beta A Z_i I_i$$

$$V_s = Z_i I_i (1 + \beta A)$$

$$\frac{V_s}{I_i} = Z_i (1 + \beta A)$$

$$\boxed{Z_{if} = Z_i (1 + \beta A)} \quad \text{.....(4.24)}$$

The input impedance increase by the factor of $(1+\beta A)$ in current series feedback connection.

(ii) The output impedance for current series feedback can be determined as follows:

→ Set $V_s = 0$ so that $V_s = V_i - V_f$ becomes

$$\boxed{V_i = V_f} \quad \ldots\ldots (i)$$

Apply KCL at the output node shown in figure 4.10

$$I_o = \frac{V}{Z_o} - AV_i \quad \cdot (4.25)$$

$$I_o = \frac{V}{Z_o} - AV_f$$

where $V_f = \beta I$

$$I = \frac{V}{Z_o} - A\beta I$$

$$\frac{V}{Z_o} = I + A\beta I$$

$$\frac{V}{Z_o} = I(1 + A\beta)$$

$$\frac{V}{I} = Z_o(1 + A\beta)$$

$$\boxed{Z_{of} = Z_o(1 + A\beta)} \quad \ldots (4.26)$$

The output impedance gets increased by the factor of $(1 + \beta A)$ in current-series feedback connection.

4.2.2.4 Current Shunt Feedback

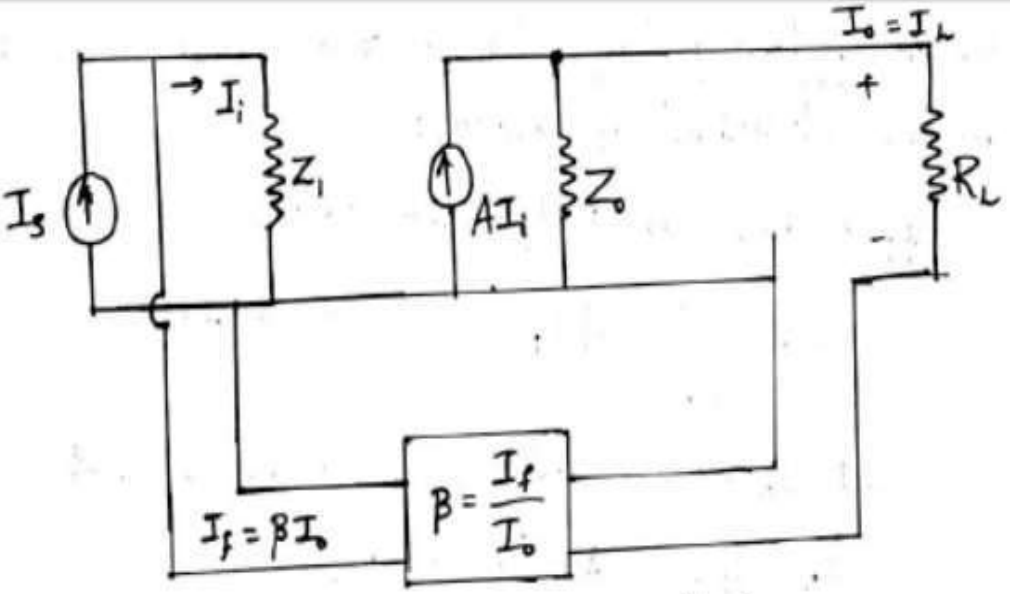


Fig 4.17: Current Shunt Feedback

Consider the ~~voltage-series~~ current shunt Feedback connection shown in Figure 4.17.

(i) The input impedance can be determined as follows,

$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} \qquad \text{where } I_f = \beta I_o$$

Dividing numerator & denominator by I_i

$$Z_{if} = \frac{V_i / I_i}{\frac{I_i}{I_i} + \frac{I_f}{I_i}} = \frac{Z_i}{\left(1 + \beta \frac{I_o}{I_i}\right)}$$

$$\boxed{Z_{if} = \frac{Z_i}{(1+\beta A)}} \quad \ldots\ldots (4.27)$$

The input impedance gets reduced by the factor of $(1+\beta A)$ in current shunt feedback connection.

(ii) The output impedance For current Shunt feedback can be determined as follows:

Apply KCL at output side node,

$$I_o = \frac{V}{Z_o} - AI_i \quad \dots\dots (4.28)$$

Set $I_s = 0$ to find o/p impedance. So that,

$I_i = I_s + I_f$ will become,

$$I_i = I_f$$

$$I_o = \frac{V}{Z_o} - AI_f$$

where $I_f = \beta I_o$

$$I_o = \frac{V}{Z_o} - A\beta I_o$$

$$\frac{V}{Z_o} = I_o + A\beta I_o$$

$$V = Z_o I_o (1 + A\beta)$$

$$\frac{V}{I_o} = Z_o (1 + A\beta)$$

$$\boxed{Z_{of} = Z_o(1 + A\beta)} \quad \dots\dots (4.29)$$

The output impedance gets increased by the factor of $(1 + \beta A)$ in current-shunt feedback connection.

Summary of Feedback Concepts:

Summary of Feedback, Gain with and without feedback

		Voltage-Series	*Voltage-Shunt*	*Current-Series*	*Current-Shunt*
Gain without feedback	A	$\frac{V_o}{V_i}$	$\frac{V_o}{I_i}$	$\frac{I_o}{V_i}$	$\frac{I_o}{I_i}$
Feedback	β	$\frac{V_f}{V_o}$	$\frac{I_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$
Gain with feedback	A_f	$\frac{V_o}{V_s}$	$\frac{V_o}{I_s}$	$\frac{I_o}{V_s}$	$\frac{I_o}{I_s}$

Effects of Feedback Connection on Input Impedance and Output Impedance

	Voltage-Series	*Current-Series*	*Voltage-Shunt*	*Current-Shunt*
Z_{if}	$Z_i(1+\beta A)$ (increased)	$Z_i(1+\beta A)$ (increased)	$\frac{Z_i}{1+\beta A}$ (decreased)	$\frac{Z_i}{1+\beta A}$ (decreased)
Z_{of}	$\frac{Z_o}{1+\beta A}$ (decreased)	$Z_o(1+\beta A)$ (increased)	$\frac{Z_o}{1+\beta A}$ (decreased)	$Z_o(1+\beta A)$ (increased)

Problems on Feedback Connections:

1. Determine the voltage gain, input, and output impedance with feedback for voltage series feedback having $A = -100$, $R_i = 10\text{ k}\Omega$, $R_o = 20\text{ k}\Omega$ for feedback of (a) $\beta = -0.1$ and (b) $\beta = -0.5$.

Solution

Using Eqs. (18.2), (18.4), and (18.6), we obtain

(a) $$A_f = \frac{A}{1+\beta A} = \frac{-100}{1+(-0.1)(-100)} = \frac{-100}{11} = \mathbf{-9.09}$$

$$Z_{if} = Z_i(1+\beta A) = 10\text{ k}\Omega\,(11) = \mathbf{110\text{ k}\Omega}$$

$$Z_{of} = \frac{Z_o}{1+\beta A} = \frac{20\times 10^3}{11} = \mathbf{1.82\text{ k}\Omega}$$

(b) $$A_f = \frac{A}{1+\beta A} = \frac{-100}{1+(0.5)(100)} = \frac{-100}{51} = \mathbf{-1.96}$$

$$Z_{if} = Z_i(1+\beta A) = 10\text{ k}\Omega\,(51) = \mathbf{510\text{ k}\Omega}$$

$$Z_{of} = \frac{Z_o}{1+\beta A} = \frac{20\times 10^3}{51} = \mathbf{392.16\ \Omega}$$

4.3 Oscillator Operation

An ***oscillator*** is a circuit that produces a periodic waveform on its output with only the dc supply voltage as an input. The output voltage can be either sinusoidal or non-sinusoidal, depending on the type of oscillator.

The use of positive feedback that results in a feedback amplifier having closed-loop gain $|A_f|$ greater than 1 and satisfies the phase conditions will result in operation as an oscillator circuit. An oscillator circuit then provides a varying output signal. If the output signal varies sinusoidally, the circuit is referred to as a ***sinusoidal oscillator***. If the output voltage rises quickly to one voltage level and later drops quickly to another voltage level, the circuit is generally referred to as a pulse or ***square-wave oscillator***.

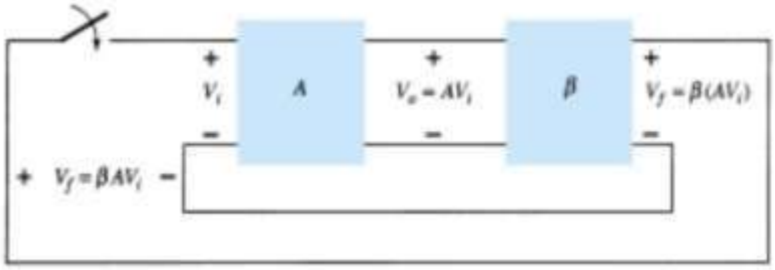


Fig 4.14: Feedback circuit used as an oscillator

To understand how a feedback circuit performs as an oscillator, consider the feedback circuit of Fig. 4.14. When the switch at the amplifier input is open, no oscillation occurs. Consider that we have some voltage at the amplifier input (V_i). This results in an output voltage $V_o = AV_i$ after the amplifier stage and in a voltage $V_f = \beta AV_i$ after the feedback stage.

Thus, we have a feedback voltage $V_f = \beta AV_i$, where A is referred to as the loop gain. If the circuits of the base amplifier and feedback network provide βA of a correct magnitude and phase, V_f can be made equal to V_i. Then, when the switch is closed and voltage V_i is removed, the circuit will continue operating since the feedback voltage is sufficient to drive the amplifier and feedback circuits resulting in a proper input voltage to sustain the loop operation. The output waveform will still exist after the switch is closed if the condition $\beta A=1$ This is known as the **Barkhausen criterion** for oscillation.

The condition βA =1 is known as ***Barkhausen criteria.*** It implies

(1) Magnitude of the loop gain βA = 1

(2) Phase shift over the loop = 0 0r 360 degrees.

If βA is made greater than 1 and the system is started oscillating by amplifying noise voltage, which is always present. Saturation factors in the practical circuit provide an "average" value of βA of 1. The resulting waveforms are never exactly sinusoidal. However, the closer the value βA is to exactly 1, the more nearly sinusoidal is the waveform. Figure 4.15 shows how the noise signal results in a buildup of **a steady-state oscillation condition**.

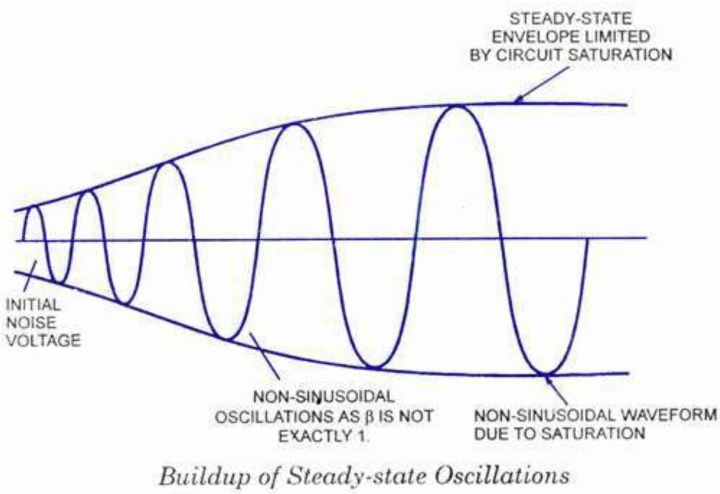


Fig 4.15: Buildup of steady-state oscillations.

4.4 FET Phase Shift Oscillator

A practical version of a FET phase-shift oscillator circuit is shown in 14.16. The circuit is drawn to show clearly the amplifier and feedback network. The amplifier stage is self-biased with a capacitor bypassed source resistor R_s and a drain bias resistor R_D. The FET device parameters of interest are gm and r_d. From FET amplifier theory, the amplifier gain magnitude is calculated from

$$|A| = g_m R_L$$

Where R_L in this case is the parallel resistance of R_D and r_d, i.e

$$R_L = \frac{R_D r_d}{R_D + r_d}$$

The RC Oscillator which is also called a ***Phase Shift Oscillator***, produces a sine wave output signal using regenerative feedback from the resistor-capacitor combination. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tank circuit). This resistor-capacitor feedback network can be connected as shown in figure 14.16 to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360^0. By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done using a 3-ganged variable capacitor.

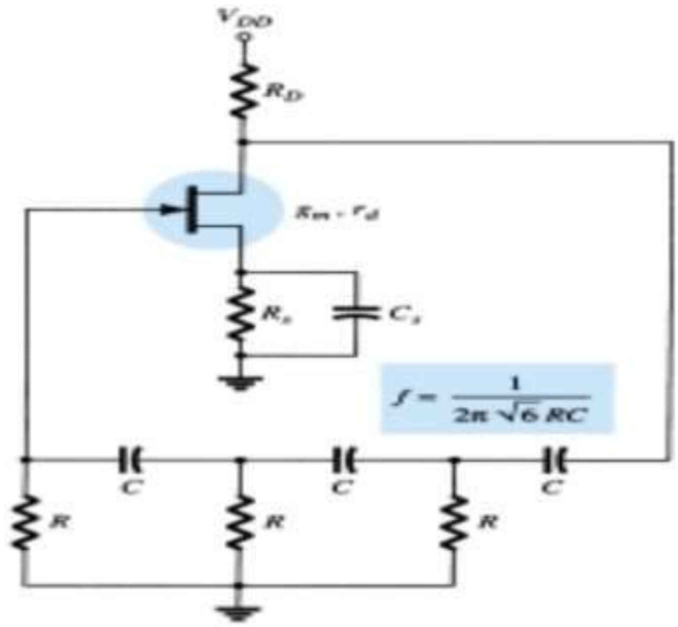


Fig 4.16: Practical FET phase-shift oscillator circuits

If all the resistors, R and the capacitors, C in the phase shift network are equal in value, then the frequency of oscillations produced by the RC oscillator is given as:

$$\boxed{f = \frac{1}{2\pi\sqrt{6}RC}}$$

Where: f is the Output Frequency in Hertz R is the Resistance in Ohms C is the Capacitance in Farads N is the number of RC stages. (in our example N = 3).

We shall assume as a very good approximation that the ***input impedance*** of the FET amplifier stage is infinite. This assumption is valid as long as the oscillator operating frequency is low enough so that FET capacitive impedances can be neglected. The ***output impedance*** of the amplifier stage given by $\mathbf{R_L}$ should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs. In practice, these considerations are not always negligible, and the amplifier stage gain is then selected somewhat larger than the needed factor of 29 to assure oscillator action.

BJT Phase Shift Oscillator:

If a transistor is used as the active element of the amplifier stage, the output of the feedback network is loaded appreciably by the relatively low input resistance (h_{ie}) of the transistor. Of course, an emitter-follower input stage followed by a common-emitter amplifier stage could be used. If a single transistor stage is desired, however, the use of voltage-shunt feedback (as

shown in Figure 4.17) is more suitable. In this connection, the feedback signal is coupled through the feedback resistor ***R`*** in series with the amplifier stage input resistance (R_i). Analysis of the ac circuit provides the following equation for the resulting oscillator frequency:
Figure 4.17 shows Practical BJT phase-shift oscillator circuits.

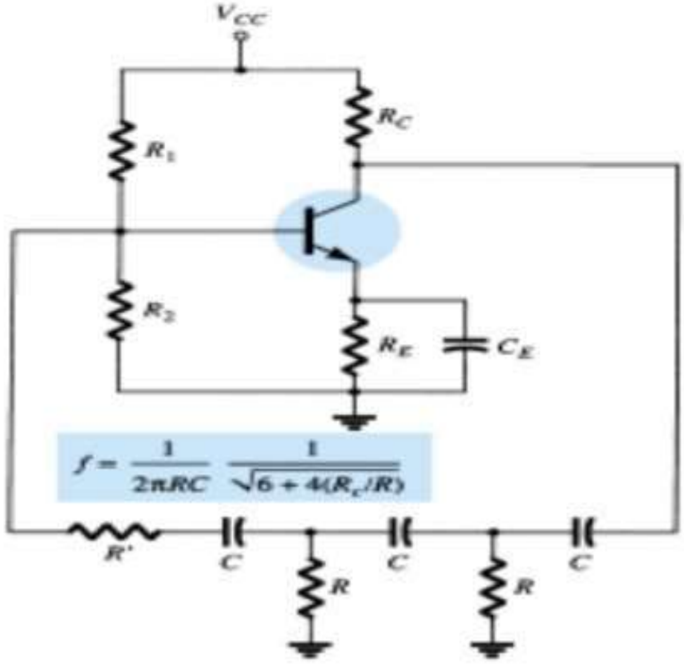


Fig 4.17: Practical BJT phase-shift oscillator circuits

4.5 Wein Bridge Oscillator

A Wien-Bridge Oscillator is a type of phase-shift oscillator which is based upon a Wien-Bridge network comprising of four arms connected in a bridge fashion. Here two arms are purely resistive while the other two arms are a combination of resistors and capacitors. In particular, one arm has resistor and capacitor connected in series (R_1 and C_1) while the other has them in parallel (R_2 and C_2). This indicates that these two arms of the network behave identical to that of ***high pass filter*** or ***low pass filter***.

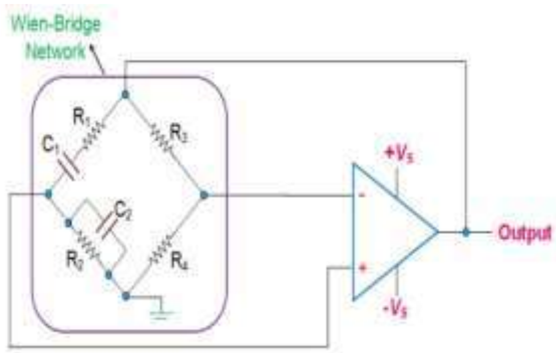


Fig 4.18: Wein Bridge Oscillator using op-amp amplifier

Wien-bridge oscillators can even be designed using Op-Amps as a part of their amplifier section, as shown by Figure 4.18. However, it is to be noted that, here, the Op-Amp is required to act as a non-inverting amplifier as the Wien-Bridge network offers zero phase-shift. Further, from the circuit, it is evident that the output voltage is fed back to both inverting and noninverting input terminals. At resonant frequency, the voltages applied to the inverting and noninverting terminals will be equal and in-phase with each other. However, even here, the voltage gain of the amplifier needs to be greater than 3 to start oscillations and equal to 3 to sustain them. In general, these kinds of Op-Amp-based Wien Bridge Oscillators cannot operate above 1 MHz due to the limitations imposed on them by their open-loop gain.

The resonant frequency for a Wein Bridge Oscillator is calculated using the following formula,

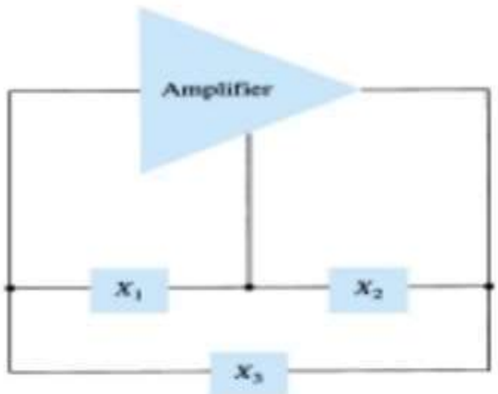
$$f_r = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

$$if\ R_1 = R_2 = R\ and\ C_1 = C_2 = C$$

$$then\ f_r = \frac{1}{2\pi RC}$$

4.6 Tuned Oscillator Circuit

A variety of circuits can be built using that shown in Fig. 4.19 by providing tuning in both the input and output sections of the circuit. Analysis of the circuit of Fig. 4.19 reveals that the following types of oscillators are obtained when the reactance elements are as designated:



	Reactance Element		
Oscillator Type	X_1	X_2	X_3
Colpitts oscillator	C	C	L
Hartley oscillator	L	L	C
Tuned input, tuned output	LC	LC	—

Fig 4.19: Basic configuration of resonant circuit oscillator

4.6.1 Hartley Oscillator

Hartley Oscillator is a type of harmonic oscillator which was invented by Ralph Hartley in 1915. These are the Tuned Circuit Oscillators which are used to produce the waves in the range of radio frequency and hence are also referred to as RF Oscillators. Its frequency of oscillation is decided by its tank circuit which has a capacitor connected in parallel with the two serially connected inductors, as shown by Figure 4.20.

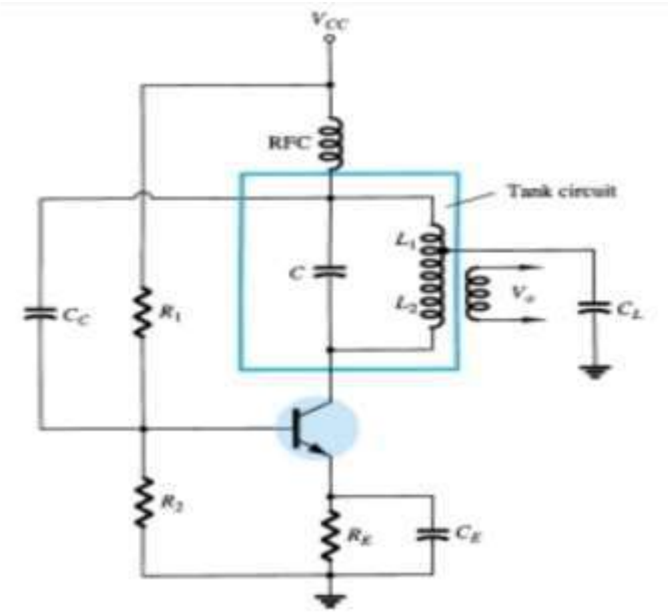


Fig 4.20: Transistor Hartley Oscillator circuit

Here the RFC is the radio frequency choke which allows only DC component, while the emitter resistor R_E forms the stabilizing network. Further the resistors R_1 and R_2 form the voltage divider bias network for the transistor in common-emitter CE configuration. Next, the capacitors C_c and C_L are the input and output decoupling capacitors while the emitter capacitor C_E is the bypass capacitor used to bypass the amplified AC signals. All these components are identical to those present in the case of a common-emitter amplifier which is biased using a voltage divider network. However, Figure 4.20 also shows one more set of components viz., the inductors L_1 and L_2 and the capacitor C which form the tank circuit.

On switching ON the power supply, the transistor starts to conduct, leading to an increase in the collector current, I_c which charges the capacitor C. On acquiring the maximum charge feasible, C starts to discharge via the inductors L_1 and L_2. This charging and discharging cycles result in the damped oscillations in the tank circuit. The oscillation current in the tank circuit produces an AC voltage across the inductors L_1 and L_2which are out of phase by 180^0 as their point of contact is grounded. Further from the figure, it is evident that the output of the amplifier is applied across the inductor L_1 while the feedback voltage drawn across L_2 is applied to the base of the transistor. Thus, one can conclude that the output of the amplifier is in phase with the tank circuit's voltage and supplies back the energy lost by it while the energy fed back to amplifier circuit will be out-of-phase by 180^0. The feedback voltage which is already 180o out-of-phase with the transistor is provided by an additional 180^0 phase-shift due to the transistor action. Hence the signal which appears at the transistor's output will be amplified and will have a net phase-shift of 360^0.

The inductors L_1 and L_2have a mutual coupling, M, which must be taken into account in determining the equivalent inductance for the resonant tank circuit. The circuit frequency of oscillation is then given approximately by

$$\boxed{f_o = \frac{1}{2\pi\sqrt{L_{eq}C}}}$$

$$L_{eq} = L_1 + L_2 + 2M$$

FET Hartley Oscillator Circuit:

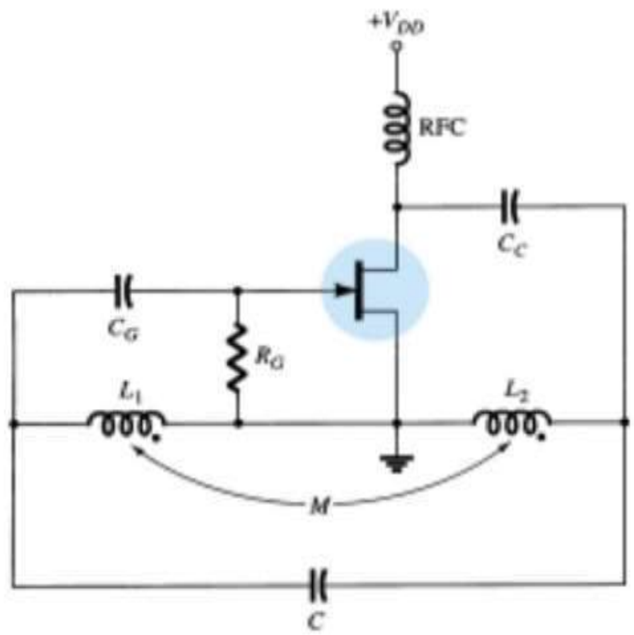


Fig 4.21: FET Hartley Oscillator circuit

The FET Hartley Oscillator circuit is as shown in the figure 4.21, the working is similar to transistor Hartley Oscillator circuit.

4.6.2 Colpitts Oscillator

Colpitts Oscillator is a type of LC oscillator which falls under the category of Harmonic Oscillator and was invented by Edwin Colpitts in 1918. Figure 4.22 shows a typical Colpitts oscillator with a tank circuit in which an inductor L is connected in parallel to the serial combination of capacitors C_1 and C_2. Other components in the circuit are the same as that found in the case of common-emitter C_E which is biased using a voltage divider network i.e. RFC is the radio frequency choke which allows DC components, R_E is the emitter resistor which is used to stabilize the circuit and the resistors R1 and R2 form the voltage divider bias network. Further, the capacitors C_c are the input coupling capacitor while the emitter capacitor C_E is the bypass capacitor used to bypass the amplified AC signals

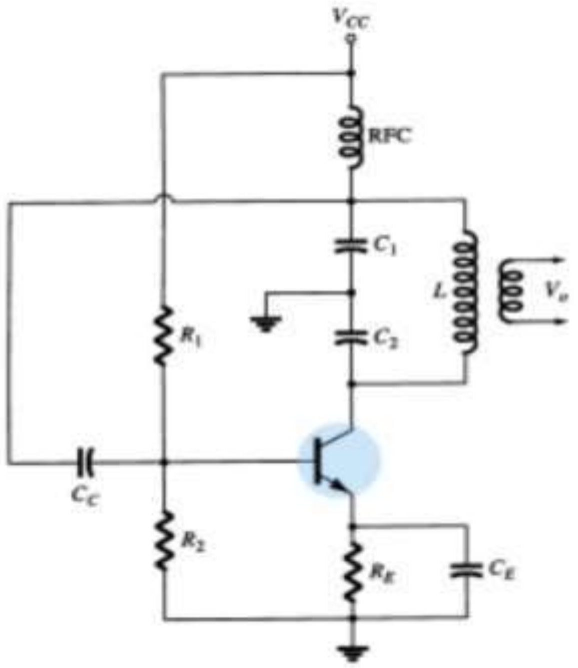


Fig 4.22: Transistor Colpitts Oscillator circuit

As the power supply is switched ON, the transistor starts to conduct, increasing the collector current I_C due to which the capacitors C_1 and C_2 get charged. On acquiring the maximum charge feasible, they start to discharge via the inductor L. During this process, the electrostatic energy stored in the capacitor gets converted into magnetic flux which in turn is stored within the inductor in the form of electromagnetic energy. Next, the inductor starts to discharge which charges the capacitors once again. Likewise, the cycle continues which gives rise to the oscillations in the tank circuit.

Further the figure shows that the output of the amplifier appears across C1 and thus is in-phase with the tank circuit's voltage and makes-up for the energy lost by re-supplying it. On the other hand, the voltage feedback to the transistor is the one obtained across the capacitor C_2, which means the feedback signal is out-of-phase with the voltage at the transistor by 180^0. This is due to the fact that the voltages developed across the capacitors C_1 and C_2 are opposite in polarity as the point where they join is grounded. Further, this signal is provided with an additional phase-shift of 180^0 by the transistor which results in a net phase-shift of 360^0 around the loop, satisfying the phaseshift criterion of Barkhausen principle.

At this state, the circuit can effectively act as an oscillator producing sustained oscillations by carefully monitoring the feedback ratio given by (C_1/C_2). The frequency of such a Colpitts Oscillator depends on the components in its tank circuit and is given by

$$\boxed{f_o = \frac{1}{2\pi\sqrt{LC_{eq}}}}$$

$$C_{eq} = \frac{C_1C_2}{C_1 + C_2}$$

Where, the C_{eq} is the effective capacitance of the capacitors expressed as shown in above equation.

FET Colpitts Oscillator circuit:

FET Colpitts Oscillator circuit is as shown in below figure 4.23.

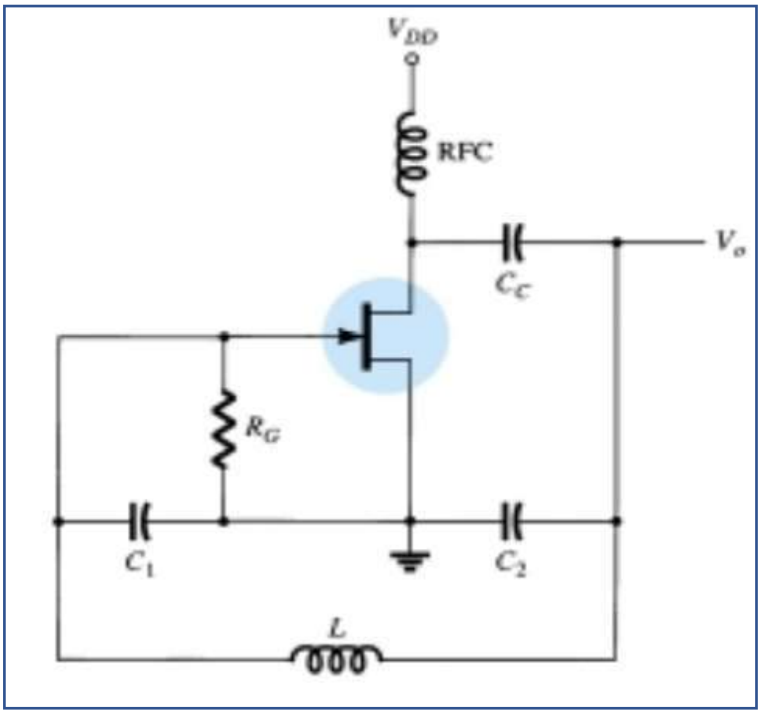


Fig 4.22: Transistor Colpitts Oscillator circuit

4.7 Crystal Oscillator

A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as a resonant tank circuit. The crystal (usually quartz) has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used whenever great stability is required, such as in communication transmitters and receivers.

Characteristics of a Quartz Crystal

A quartz crystal (one of a number of crystal types) exhibits the property that when mechanical stress is applied across the faces of the crystal, a difference of potential develops across opposite faces of the crystal. This property of a crystal is called the ***piezoelectric effect***.

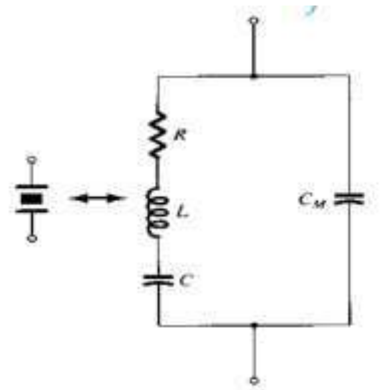
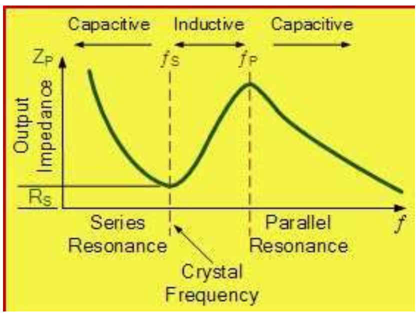


Fig 4.23: Electrical equivalent circuit of a crystal

When alternating voltage is applied to a crystal, mechanical vibrations are set up—these vibrations having a natural resonant frequency dependent on the crystal. Although the crystal has electromechanical resonance, we can represent the crystal action by an equivalent electrical resonant circuit as shown in Fig. 14.23.

The inductor **L** and capacitor **C** represent electrical equivalents of crystal mass and compliance, while resistance **R** is an electrical equivalent of the crystal structure's internal friction. The shunt capacitance **C_M** represents the capacitance due to mechanical mounting of the crystal.



When the frequency of ac source signal is equal to the frequency f_s the current through the crystal becomes maximum (I_{max}), this condition is called series resonance and f_s is called the ***series resonant frequency***.

When the frequency of ac source signal is equal to the frequency f_p the current through the crystal becomes minimum (I_{min}), this condition is called parallel resonance and f_p is called the ***parallel resonant frequency***.

Series-Resonant Circuit:

To excite a crystal for operation in the series-resonant mode, it may be connected as a series element in a feedback path. At the series-resonant frequency of the crystal, its impedance is smallest and the amount of (positive) feedback is largest. A typical transistor circuit is shown in Fig. 4.24(a). Resistors R_1, R_2, and R_E provide a voltage divider stabilized dc bias circuit. Capacitor C_E provides ac bypass of the emitter resistor, and the RFC coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal. The voltage feedback from collector to base is a maximum when the crystal impedance is minimum (in series-resonant mode).

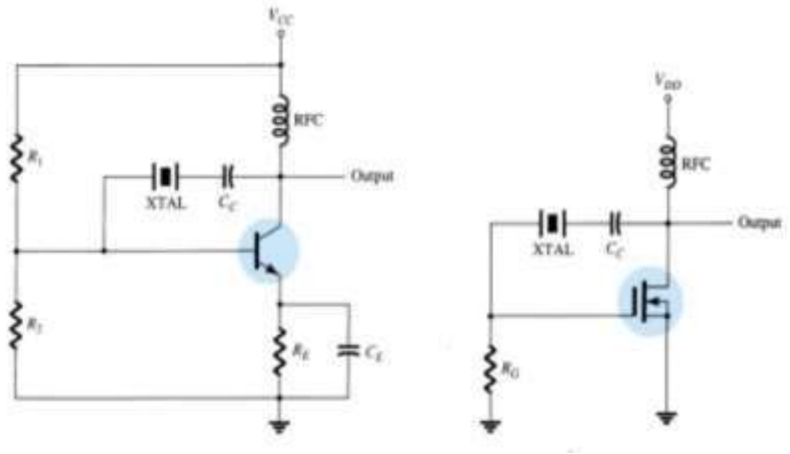


Fig 4.24: Crystal-controlled oscillator using crystal in series-feedback (a) BJT (b) FET

The coupling capacitor C_c has negligible impedance at the circuit operating frequency but blocks any dc between collector and base. The resulting circuit frequency of oscillation is set, then, by the series-resonant frequency of the crystal. Changes in supply voltage, transistor device parameters, and so on have no effect on the circuit operating frequency, which is held stabilized by the crystal. The circuit frequency stability is set by the crystal frequency stability, which is good. The frequency of circuit operating in series-resonant mode is given by

$$f = \frac{1}{2\pi\sqrt{L.C}}$$

Parallel-Resonant Circuit:

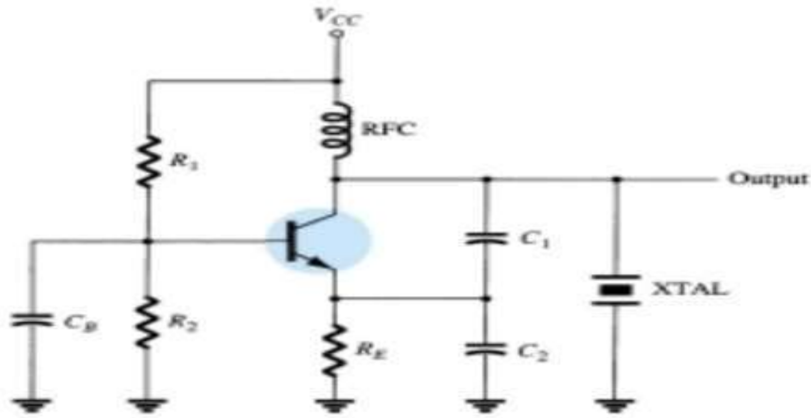


Fig 4.25: Crystal-controlled oscillator operating in parallel-resonant mode.

Since the parallel-resonant impedance of a crystal is a maximum value, it is connected in shunt. At the parallel-resonant operating frequency, a crystal appears as an inductive reactance of largest value. Figure 4.25 shows a crystal connected as the inductor element in a modified Colpitts circuit. tor element in a modified Colpitts circuit. The basic dc bias circuit should be evident. Maximum voltage is developed across the crystal at its parallel-resonant frequency. The voltage is coupled to the emitter by a capacitor voltage divider—capacitors C_1 and C_2. The frequency of circuit operating in parallel-resonant mode is given by

$$f_p = \frac{1}{2\pi\sqrt{L.C_T}}$$

where,

$$C_T = \frac{CC_m}{(C + C_m)}$$

The value of $C_a$is usually very large as compared to C. Therefore, the value of C_T is approximately equal to C and hence the series resonant frequency is approximately equal to the parallel resonant frequency (i.e., $f_s = f_p$).

* Hybrid π model:

→ The hybrid π model is as shown in the below figure, which includes parameters that do not appear in the other two models (r_e, hybrid) primarily to provide a more accurate model for high frequency effects.

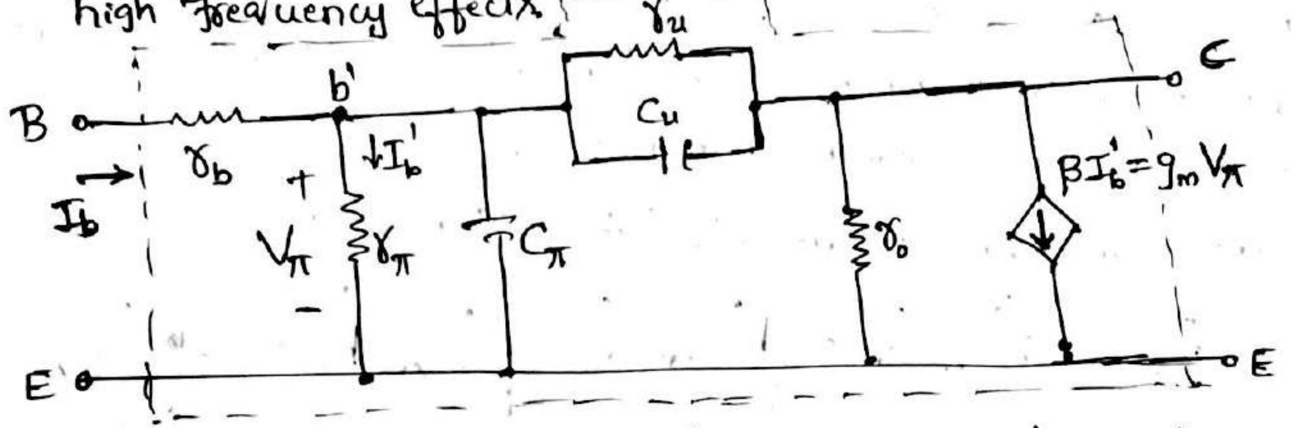


Fig: Giacoletto (or hybrid π) high frequency transistor small-signal ac equivalent circuit.

→ All the capacitors that appears in the above figure are stray parasitic capacitors between the various junction of the device.

→ At high frequency all capacitive effects will come into play, at low frequency all capacitance acts as open circuit.

→ C_π represents the diffusion capacitance of forward bias of Base-Emitter junction.

→ C_u represents transition capacitance due to reverse bias of collector & base junction.

→ The resistance r_b includes the base contact, base bulk and base spreading resistance level.

→ The resistance r_π is βr_e similar to common-emitter r_e model.

→ The resistance r_u (the subscript u refers to the union it provides between collector & base terminals) is a very large resistance and provides a feedback path from output to input circuits in the equivalent model.

→

- The resistance r_o represents the output resistance across the load.
- For low to mid frequency analysis the effect of the stray capacitive effects can be ignored due to very high reactance levels associated with each.

→ r_b is very small can be replaced by short circuit, r_u is large it can be ignored for many applications.

Typical data sheet values for hybrid π model is,

$$r_\pi = \beta r_e, \quad g_m = \frac{1}{r_e}, \quad r_o = \frac{1}{h_{oe}}, \quad h_{re} = \frac{r_\pi}{r_\pi + r_u}$$

$$h_{re} = \frac{r_\pi}{r_\pi + r_u} = \frac{r_\pi}{r_u}$$

$$r_\pi = \frac{\beta}{g_m}$$

Module-2

Chapter-1 FET FREQUENCY RESPONSE

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* Logarithms:

Consider the following mathematical equations:

$$a = b^x, \quad x = \log_b a \quad \cdots \quad (1)$$

The variables a, b and x are the same in both expressions. If the variable 'a' is determined by taking the base b to the power, the same x will result if the log of a is taken to the base b.

John Napier invented logarithms, but many other scientists and mathematicians helped to develop Napier's logarithm system that we use today.

For example, if $b = 10$ and $x = 2$ then

$$a = b^x = (10)^2 = 100 \text{ and}$$

$$x = \log_b a = \log_{10}(100) = 2.$$

→ For the electrical / electronics industry & majority of scientific researchers use the base in the logarithm equation is chosen as either 10 or the number $e = 2.71828\ldots$

→ (i) Logarithms taken to the base 10 are referred as Common Logarithms.

$$x = \log_{10} a.$$

(ii) Logarithms taken to the base e are referred as Natural Logarithm.

$$y = \log_e a$$

→ Common logarithms and natural logarithms are related by :

$$\log_e a = 2.3 \log_{10} a$$

→ on scientific calculator, the common logarithm is typically denoted by the key $\boxed{\log}$, and natural logarithm is typically denoted by the key $\boxed{\ln}$.

Examples 1:

(1) $\log_{10} 10^6 = 6$ (2) $\log_e e^3 = 3$ (3) $\log_{10} 10^{-2} = -2$ (4) $\log_e e^{-1} = -1$:

Properties

(1) $\log_{10} 1 = 0$ (2) $\log_{10} \frac{a}{b} = \log_{10} a - \log_{10} b$.

(3) $\log_{10}\left(\frac{1}{b}\right) = -\log_{10} b$ (4) $\log_{10} ab = \log_{10} a + \log_{10} b$.

Examples 2:

(1) $\log_{10} 64 = 1.806$ (2) $\log_e 64 = 4.159$ (3) $\log_{10} 1600 = 3.204$

(4) $\log_{10} 10^{-5} = -5$.

Examples 3:

(1) $1.6 = \log_{10} a$ Find a? → solution: $a = 10^{1.6} = 39.81$

(2) $0.04 = \log_e a$ Find a? → Solution: $e^{0.04} = 1.0408$

(3) $\log_{10}\left(\frac{1}{2}\right) = -0.3$

(4) $\log_{10}\left(\frac{4000}{250}\right) = 1.204$

(5) $\log_{10}(0.6 \times 30) = 1.255$

* Decibels:

The term decibel has its origin in the fact that power and audio levels are related on a logarithm basis. That is, increase in power level from 4W to 16W does not result in audio level increase by a factor of 4, but factor of 2.

Similarly if power level increased from 4W to 64W does not result in an audio level increase by a factor of 16, instead it will increase by the factor 3.

i.e $4 \to 16 \to 4^2 \to 2$ i.e $\log_4(16) = 2$

$4 \to 64 \to 4^3 \to 3$ $\log_4(64) = 3.$

The term bel is derived from the surname of Alexander Graham Bell

For standardization, the bel (B) is defined by the following equation relating two power levels, P_1 and P_2.

$$G = \log_{10} \frac{P_2}{P_1} \text{ bel}$$

For particular purpose, G_{dB} will be,

$$G_{dB} = 10 \log_{10}\left(\frac{P_2}{P_1}\right) \text{ dB} \quad \cdots (1)$$

→ The terminal rating of electronic components is commonly in decibels.

$P_2 \to$ output power level

$P_1 \to$ Reference power level.

→ The second equation for decibels that is applied frequently exist and can be derived as,

W.K.T for some value V_1,

$$P_1 = \frac{V_1^2}{R_i} \quad \text{--- (2)}$$

and for some other value V_2,

$$P_2 = \frac{V_2^2}{R_i} \quad \text{--- (3)}$$

substitute equation (2) & (3) in (1) then

$$G_{dB} = 10\log_{10}\left(\frac{\left(\frac{V_2^2}{\cancel{R_i}}\right)}{\left(\frac{V_1^2}{\cancel{R_i}}\right)}\right) = 10\log_{10}\left(\frac{V_2^2}{V_1^2}\right)$$

$$\boxed{G_{dB} = 20\log_{10}\left(\frac{V_2}{V_1}\right)}$$

* Cascaded Stages: The advantage of logarithmic relationship is that it can be applied to cascaded stages.

For example, the magnitude of overall voltage gain of a cascaded system is given by

$$|A_{v_T}| = |A_{v_1}| \cdot |A_{v_2}| |A_{v_3}| \cdots |A_{v_n}|$$

$$G_{dB} = 20\log_{10}(A_{v_T}) = 20\log_{10}A_{v_1} + 20\log_{10}A_{v_2} + \cdots + 20\log_{10}A_{v_n}$$

Examples on Decibels:

(1) Find the magnitude gain corresponding to a voltage gain of 100dB.

Solution: W.K.T $G_{dB} = 100dB$

$$20\log_{10}\left(\frac{V_2}{V_1}\right) = 100$$

$$\log_{10}\left(\frac{V_2}{V_1}\right) = \frac{\cancel{100}\ 5}{\cancel{20}}$$

$$\boxed{\frac{V_2}{V_1} = 10^5}$$

(2) The input power to a device is 10,000W at a voltage of 1000V. The o/p power is 500W and the output impedance is 20Ω. Find (i) the power gain in decibels.

(ii) Voltage gain in decibels.

Solutions (i) $G_{dB} = 10\log_{10}\left(\frac{P_o}{P_i}\right) = 10\log_{10}\left(\frac{500}{10,000}\right) = -13.01dB$

(ii) $G_{dB} = 20\log_{10}\left(\frac{V_o}{V_i}\right) = 20\log_{10}\left(\frac{\sqrt{PR}}{V_i}\right) = 20\log_{10}\left(\frac{1}{10}\right) = -20dB$

$P = \frac{V_o^2}{R}$ & $V_o = \sqrt{PR}$

(3) An amplifier rated at 40W output is connected to a 10Ω speaker.

(a) calculate the input power required for full power output if the power gain is 25dB.

(b) Calculate the input voltage for rated output if the amplifier voltage gain is 40dB.

Solution:

(a) $P_i = ?$

$P_o = 40W$

$G_{dB} = 25dB$

W.K.T

$$G_{dB} = 10\log_{10}\left(\frac{P_o}{P_i}\right)$$

$$25 = 10\log_{10}\left(\frac{40}{P_i}\right)$$

$$\log_{10}\left(\frac{40}{P_i}\right) = \frac{25}{10}$$

$$\frac{40}{P_i} = 10^{2.5}$$

$$P_i = \frac{40}{316} = \underline{\underline{12.6.5mW}}$$

(b) $V_i = ?$ $V_o = ?$ $G_{dB} = 40$

W.K.T

$$G_{dB} = 20\log_{10}\left(\frac{V_o}{V_i}\right) \Rightarrow 40 = 20\log_{10}\left(\frac{V_o}{V_i}\right)$$

$$\log_{10}\left(\frac{V_o}{V_i}\right) = 2 \Rightarrow \frac{V_o}{V_i} = 10^2 = \underline{\underline{100}}$$

W.K.T $V_o = \sqrt{PR} = \sqrt{40 \times 10} = \underline{\underline{20V}}$

$$\frac{V_o}{V_i} = 100 \quad \xi_1 \Rightarrow V_i = \frac{V_o}{100} = \frac{20}{100} = \underline{\underline{200mV}}$$

* Frequency Response:

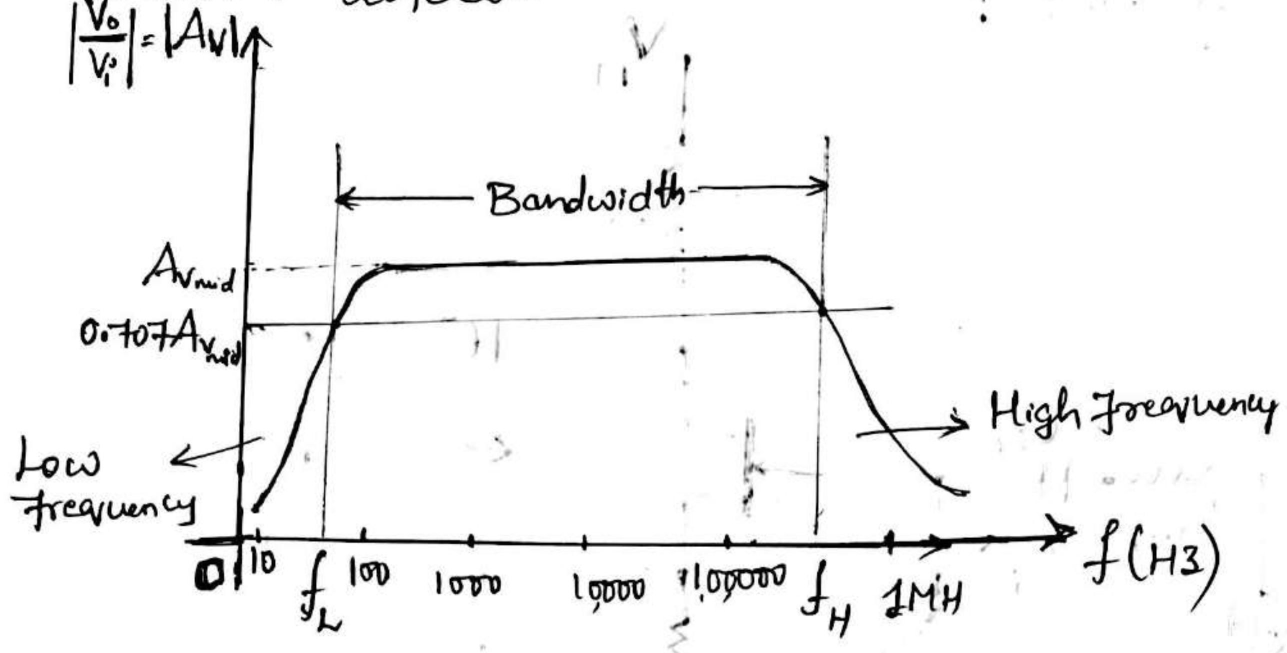

Fig: Gain vs Frequency plot

→ The frequency response can be divided into three regions,

(a) Low Frequency Region: In this region the amplifier can be modeled as a High pass Filter. The frequency at which the gain rises to $\frac{1}{\sqrt{2}}$ times the midband gain ($A_{V_{mid}}$) is called the lower cut-off frequency or break frequency or corner frequency represented by f_L or f_1. Hz,

(b) High Frequency Region: In this region the amplifier can be modeled as Low pass Filter. The frequency at which the gain falls to $\frac{1}{\sqrt{2}}$ times mid band gain ($A_{V_{mid}}$) is called upper cut-off frequency represented by f_H or f_2 Hz.

(c) Mid Band Region:

In this region the gain is independent of frequency & it is constant at $A_{V_{mid}}$.

This is the best region of operation of the amplifier.

* Low-Frequency Response - FET (Field Effect Transistor) Amplifier:

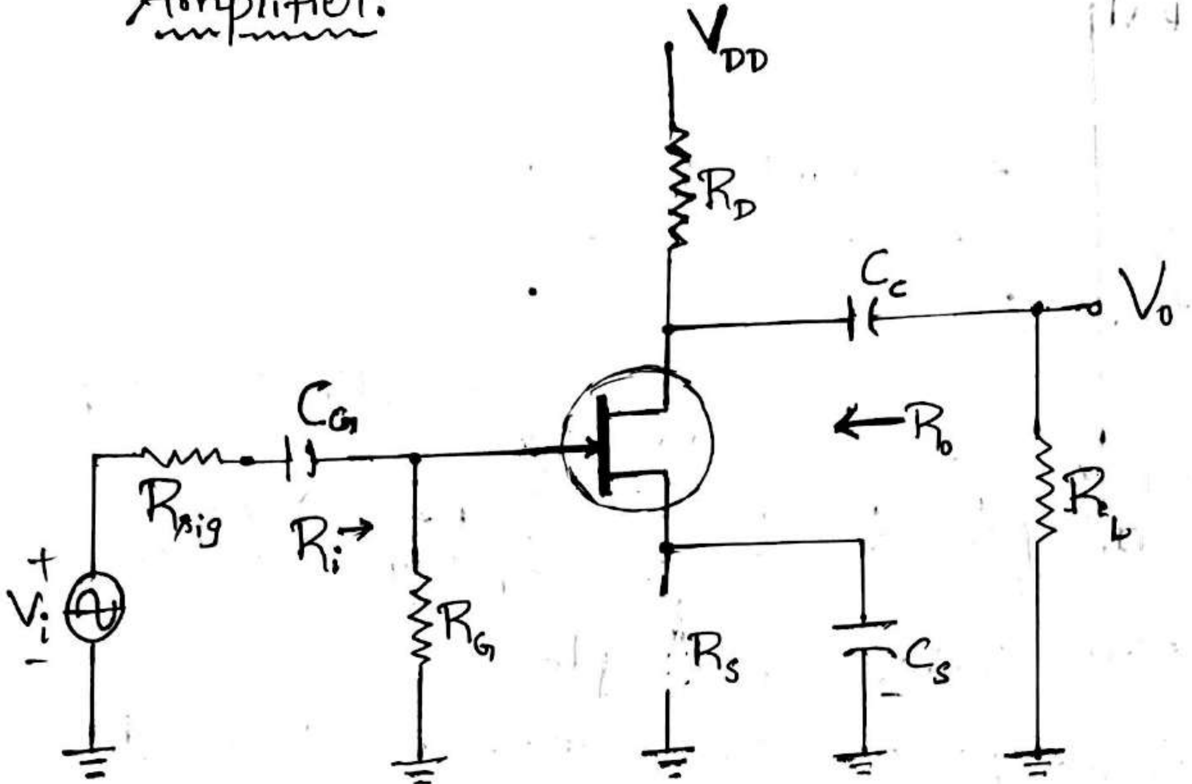

Fig 1: Capacitive Element that affect the Low-Frequency response of a JFET amplifier.

→ There are three capacitors of primary concern as shown in above Figure: C_G, C_c, C_s.

(i) C_G → For the coupling capacitor between the source and the active device, the ac equivalent network is as shown below.

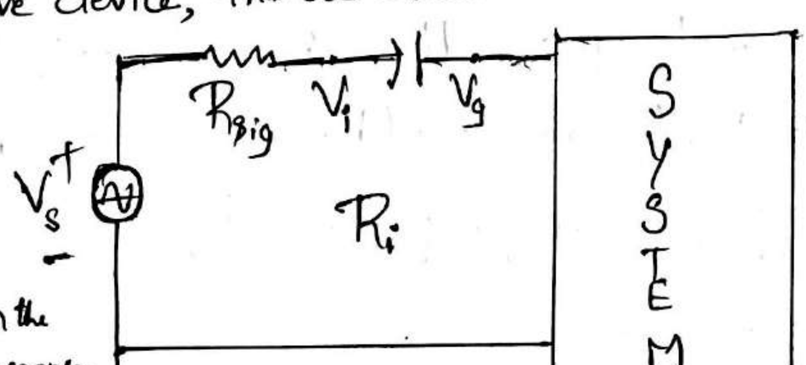

Fig 2: Determining the effect of C_G on the Low-Frequency Response

where

$$R_i = R_G$$

The cut-off Frequency determined by C_G is

$$f_{LG} = \frac{1}{2\pi(R_{sig}+R_i)C_G} \quad \cdots (1)$$

(ii) $C_c \rightarrow$ For the coupling capacitor between the active device and the load the network is as shown below figure.

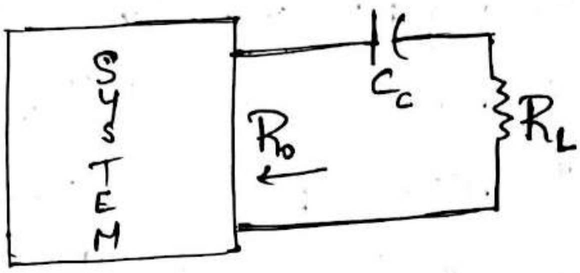

Fig 3: Determining the effect of C_c on the low-frequency Response

The resulting cut off frequency is,

$$\boxed{f_{LC} = \frac{1}{2\pi (R_o + R_L) C_c}} \quad \cdots (2)$$

For the network shown in figure 1 $R_o = R_D \| r_d$

(iii) $C_s \rightarrow$ For the source capacitor C_s, the resistance level of importance is defined by figure 4.

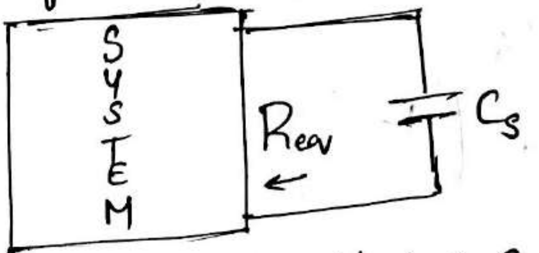

Fig 4: Determining the effect of C_s on the low-frequency response

The cutoff frequency is defined by

$$\boxed{f_{LS} = \frac{1}{2\pi R_{eq} C_s}}$$

The R_{eq} is given by

$$\boxed{R_{eq} = \frac{R_s}{1 + R_s(1 + g_m r_d)/(r_d + R_D \| R_L)}}$$

which for $r_d \cong \infty \Omega$

$$\boxed{R_{eq} = R_s \| \frac{1}{g_m}}$$

Problems

(1) Determine the lower cutoff frequency for the low frequency response of JFET amplifier using the following parameters.
$C_G = 0.01\mu F$, $C_c = 0.5\mu F$, $C_S = 2\mu F$, $R_{sig} = 10K\Omega$, $R_G = 1M\Omega$, $R_D = 4.7k\Omega$, $R_S = 1K\Omega$, $R_L = 2.2K\Omega$, $I_{DSS} = 8mA$, $V_p = -4V$, $r_d = \infty\Omega$, $V_{DD} = 20V$, $V_{GS} = -2V$. Also find mid band Gain.

Solution:

Lower cutoff frequencies $f_{LG} = ?$ $f_{LC} = ?$ $f_{LS} = ?$,

(i) $$f_{LG} = \frac{1}{2\pi(R_{sig}+R_i)C_G} = \frac{1}{2\pi(10K\Omega + 1M\Omega)(0.01\mu F)} = \underline{\underline{15.8Hz}}$$

W.K.T $R_i = R_G$

(ii) $$f_{LC} = \frac{1}{2\pi(R_o+R_L)C_c} = \frac{1}{2\pi(4.7k\Omega+2.2k\Omega)(0.5\mu F)} = \underline{\underline{46.13Hz}}$$

(iii) $$f_{LS} = \frac{1}{2\pi R_{eq} C_S} \quad \text{where } R_{eq} = R_S \| \frac{1}{g_m} \quad \{\text{Since } r_d = \infty\Omega\}$$

where $$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$$

& to find g_{mo} we have $$g_{mo} = \frac{2 I_{DSS}}{V_P} = \frac{2(8m)}{(4)} = \underline{\underline{4mS}}$$

Therefore $$g_m = g_{mo}\left(1 - \frac{(-2)}{(-4)}\right) = \underline{\underline{2mS}}$$

$$R_{eq} = R_S \| \frac{1}{g_m} = \left(1K\Omega \| \frac{1}{2m}\right) = 333.33\,\Omega$$

$$f_{LS} = \frac{1}{2\pi R_{eq} C_S} = \frac{1}{2\pi(333.33)(2\mu F)} = \underline{\underline{238.73Hz}}$$

(iv) $$A_{Vmid} = \frac{V_o}{V_i} = -g_m(R_D\|R_L) = -(2mS)(1.499k\Omega) = \underline{\underline{-3}}$$

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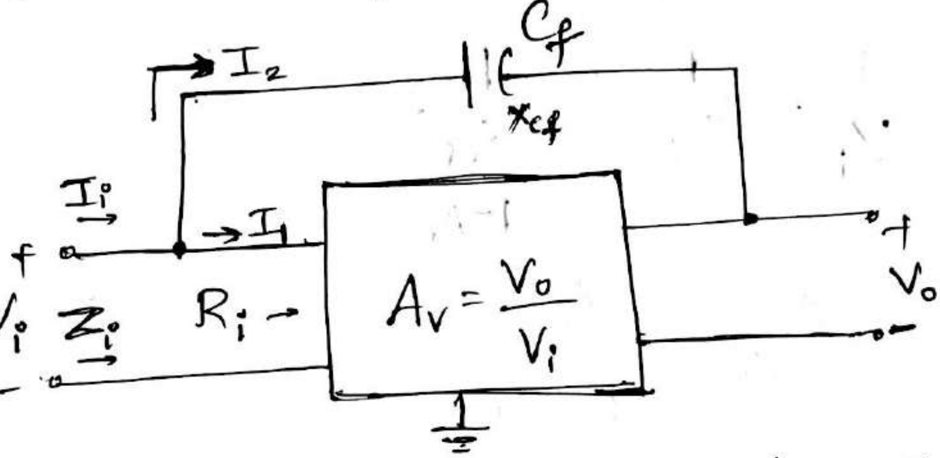
* Miller Effect Capacitance:

In the high-frequency region, the capacitive elements of importance are interelectrode capacitances internal to the active device and wiring capacitance between leads of the network.

"The junction capacitance C_{bc} is connected between input (Base) and the output (collector) for high frequency transistor and it is necessary to split the capacitance between input (Base) and the output (collector). This can be achieved by using Miller's Theorem."



Fig(a): Network Employed in the derivation of the equation for the Miller Input capacitance

(i) Miller Input Capacitance:

Applying KCL in Figure (a) gives,

$$I_i = I_1 + I_2 \quad \cdots (1)$$

using ohm's law

$$I_i = \frac{V_i}{Z_i}, \quad I_1 = \frac{V_i}{R_i}, \quad I_2 = \frac{V_i - V_o}{X_{cf}}$$

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{V_i - V_o}{X_{cf}} \quad \cdots (2)$$

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W.K.T Voltage Gain is given by,

$$\left\{ A_v = \frac{V_o}{V_i} \Rightarrow V_o = A_v V_i \right\} \quad \cdots (3)$$

∴ Equation (2) can be written as

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{V_i\left(1 - \frac{V_o}{V_i}\right)}{X_{c_f}} \quad \cdots (4)$$

Substitute Equation (3) in (4)

$$\frac{\cancel{V_i}}{Z_i} = \cancel{V_i}\left[\frac{1}{R_i} + \frac{(1 - A_v)}{X_{c_f}}\right]$$

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{\left(\frac{X_{c_f}}{1-A_v}\right)}$$

where $X_{C_{Mi}} = \dfrac{X_{c_f}}{1-A_v}$

$$\frac{1}{\cancel{2\pi f} C_{Mi}} = \frac{1}{\cancel{2\pi f} C_f (1-A_v)}$$

$$\boxed{C_{Mi} = C_f (1-A_v)}$$

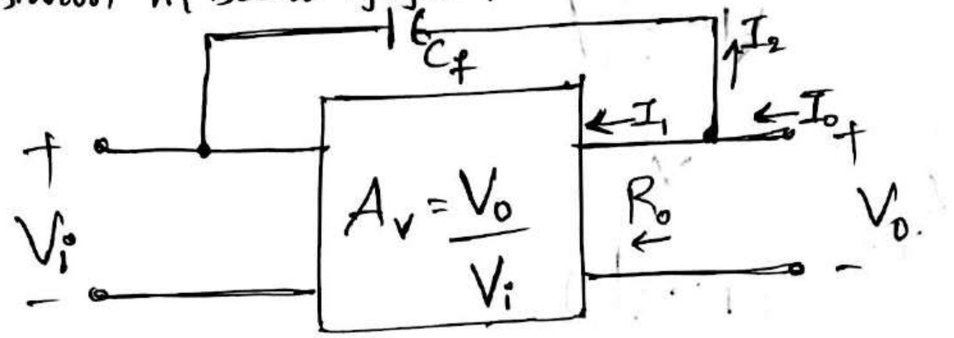
C_{Mi} → Miller input capacitance

C_f → Feedback Capacitance. $\{C_{bc}\}$

"For any inverting amplifier, the miller input capacitance is increased by a capacitance level sensitive to the gain of the amplifier and interelectrode capacitance between the input & output terminal of the active device".

(ii) Miller Output Capacitance:

Network employed to derive miller output capacitance is as shown in below figure.



Figure(b): Network to Derive Miller output Capacitance

Applying Kirchoff's current law for n/w in Fig (b),

$$I_o = I_1 + I_2 \quad \text{---(1)}$$

Using ohm's law,

$$I_1 = \frac{V_o}{R_o}, \quad I_2 = \frac{V_o - V_i}{X_{Cf}}$$

The value of R_o is usually very large so I_1 can be ignored.

Equation (1) becomes

$$I_o = \frac{V_o - V_i}{X_{Cf}} = \frac{V_o\left(1 - \frac{V_i}{V_o}\right)}{X_{Cf}}$$

where $A_v = \frac{V_o}{V_i}$ and $\frac{1}{A_v} = \frac{V_i}{V_o}$

Therefore $\frac{I_o}{V_o} = \frac{\left(1 - \frac{1}{A_v}\right)}{X_{Cf}}$

$$\frac{I_o}{V_o} = \frac{1}{\left(\frac{X_{cf}}{1-\frac{1}{A_v}}\right)}$$

where

$$X_{CMo} = \frac{X_{cf}}{\left(1-\frac{1}{A_v}\right)}$$

$$\frac{1}{\cancel{2\pi f} C_{Mo}} = \frac{1}{\cancel{2\pi f} C_f\left(1-\frac{1}{A_v}\right)}$$

$$\boxed{C_{Mo} = C_f\left(1-\frac{1}{A_v}\right)}$$

$C_{Mo} \rightarrow$ Miller output capacitance.

After applying miller theorem, the network in Figure(a) can be redrawn as,

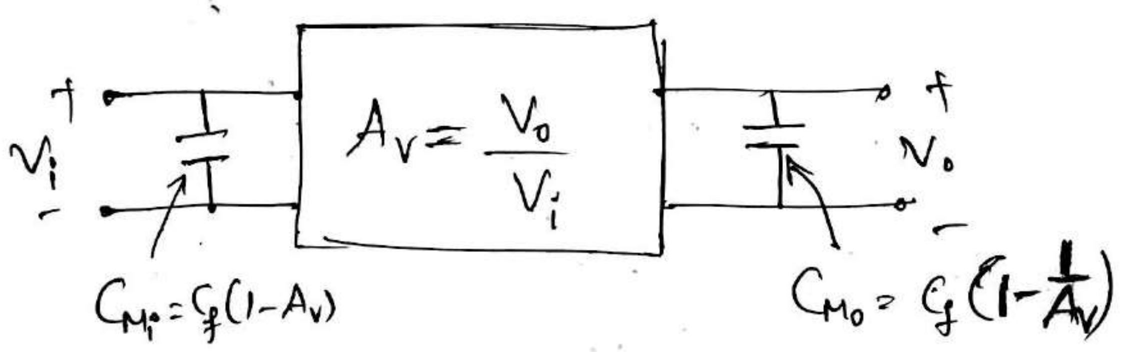


Fig: Network after Miller Theorem

* High Frequency Response - FET Amplifier:

In the high frequency response of the FET amplifier there are interelectrode & wiring capacitances that will determine the high frequency characteristics of the amplifier.

The network is an inverting amplifier, a miller effect capacitance will appear on the high frequency AC equivalent network. At high frequencies C_i will approach a short circuit equivalent & V_{GS} will drop in value and reduce the overall gain. At frequencies where C_o is short circuited V_o will reduce in magnitude.

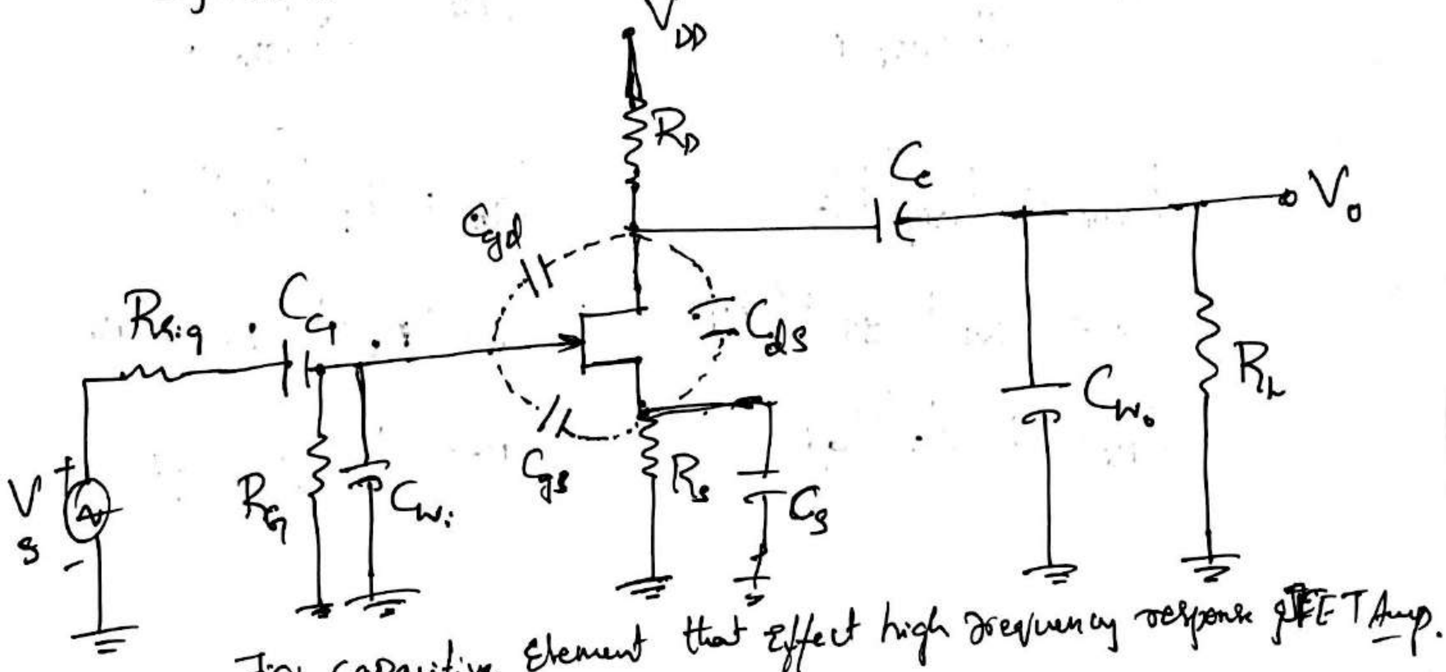


Fig: capacitive Element that Effect high frequency response of FET Amp.

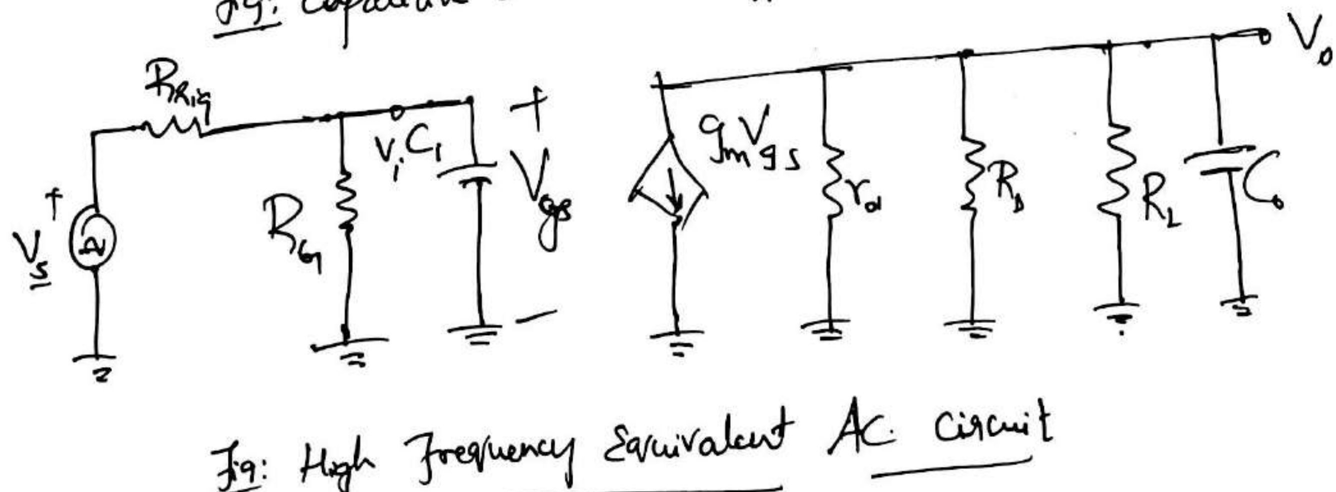


Fig: High Frequency Equivalent AC Circuit

The cutoff frequencies defined by the i/p & o/p circuits can be obtained by first finding the Thevenin equivalent ckt for each section.

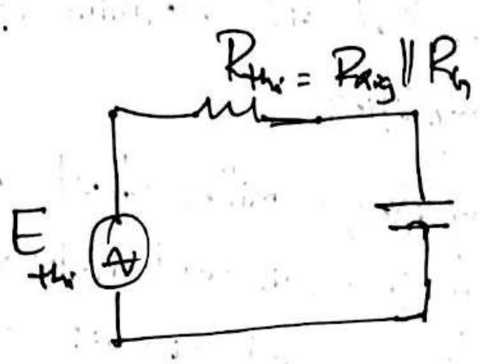


Fig: Thevenin equivalent I/p circuit

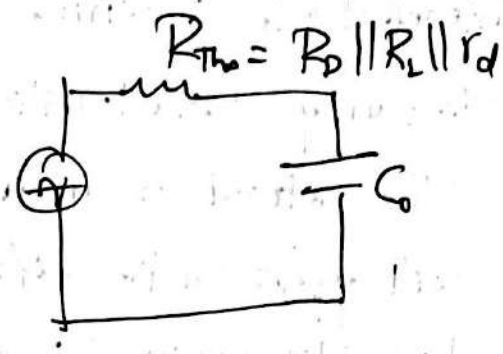


Fig: Thevenin equivalent o/p circuit

$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i} \quad \ldots (1) \qquad f_{Ho} = \frac{1}{2\pi R_{Tho} C_o} \quad \ldots (2)$$

$$R_{Thi} = R_{sig} \| R_G \qquad R_{Tho} = R_D \| R_L \| r_d$$

$$C_i = C_{wi} + C_{gs} + C_{Mi} \qquad C_o = C_{wo} + C_{ds} + C_{Mo}$$

$$C_{Mi} = (1 - A_v) C_{gd} \qquad C_{Mo} = \left(1 - \frac{1}{A_v}\right) C_{gd}$$

where

C_{Mi} → Miller input capacitance

C_{Mo} → Miller output capacitance

High frequency of FET amplifier is given by equation ① & ②

* Problem

(1) Determine the high-cutoff frequencies for the high-frequency response FET Amplifier using the following parameters.

$C_G = 0.01\mu F$, $C_c = 0.5\mu F$, $C_s = 2\mu F$, $R_{sig} = 10K\Omega$,

$R_G = 1M\Omega$, $R_D = 4.7K\Omega$, $R_S = 1K\Omega$, $R_L = 2.2K\Omega$,

$I_{DSS} = 8mA$, $V_p = -4V$, $r_d = \infty\Omega$, $V_{DD} = 20V$,

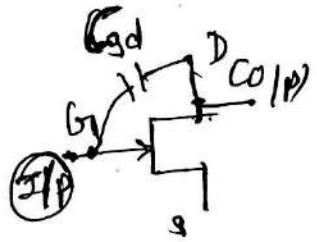
$V_{GS} = -2V$, $C_{gd} = 2pF$, $C_{gs} = 4pF$, $C_{ds} = 0.5pF$,

$C_{W_i} = 5pF$, $C_{W_o} = 6pF$.

Solution:

(1) $$f_{H_i} = \frac{1}{2\pi R_{Th_i} C_i}$$

$R_{Th_i} = R_{sig} \| R_G = 10K\Omega \| 1M\Omega$



$$\boxed{R_{Th_i} = 9.9K\Omega}$$

$C_i = C_{Wi} + C_{gs} + C_{M_i}$

{ $C_{gd} = C_f$ = feedback capacitor. }

where $C_{M_i} = (1 - A_v) C_{gd}$

where $A_v = -g_m (R_D \| R_L)$

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = 4m\left(1 - \frac{(-2)}{(-4)}\right) = 2mS$$

$$g_{mo} = \frac{2 I_{DSS}}{V_P} = 4mS$$

{ $R_D \| R_L = 4.7k \| 2.2k$ }

$A_v = -2m(1.499k) = -3$ ← ($R_D \| R_L = 1.499K\Omega$)

Multistage Frequency Effects:

(19)

→ The effect of increasing the number of identical stages can be clearly demonstrated by Figure (a). In each case, the upper and lower cut-off frequencies of each cascaded stages are identical.

→ For single stage frequencies are f_1 and f_2 indicated in Figure (a).

→ For two identical stages in cascade −3dB point has shifted to f_1' and f_2' with a resulting drop in the bandwidth.

→ The low frequency region and high frequency region can be determined by using equation (2) & (3).

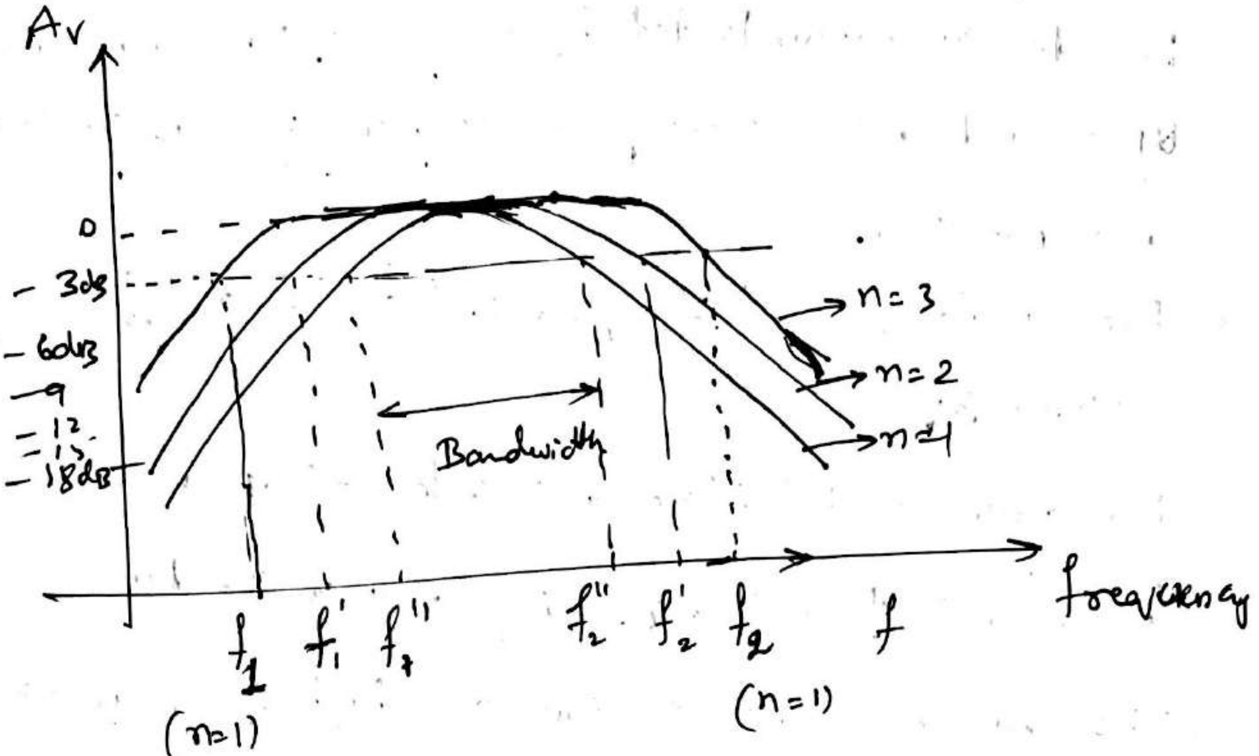
In equation (2) & (3) 'n' indicates number of stages that are identical.

→ As the 'n' value increases lower cutoff frequency increases & higher cutoff frequency decreases which indicates the reduction in bandwidth.

→ A decrease in bandwidth is not always associated with an increase in the number of stages if the midband gain can remain fixed & independent of the number of stages.

Continued from previous page →

* Multistage Frequency Effects:



Fig(a): Effect of an increased number of stages on the cutoff frequencies & the Bandwidth

For the low frequency region,

$$A_{v_{low}} = A_{v_{1low}} A_{v_{2low}} \cdots A_{v_{n(low)}} \quad \cdots (1)$$

$$A_{v_{low(small)}} \equiv \left(A_{v_{1low}}\right)^n \quad \Big\} \text{ Since all stages are identical.}$$

For the low frequency region

$$\boxed{f_1' = \frac{f_1}{\sqrt{2^{1/n} - 1}}} \text{ Hz} \cdots (2)$$

For the High frequency region

$$\boxed{f_2' = \left(\sqrt{2^{1/n} - 1}\right) f_2} \text{ Hz} \cdots (3)$$

Table: n vs $\sqrt{2^{1/n}-1}$

n	$\sqrt{2^{1/n}-1}$
2	0.64
3	0.51
4	0.43
5	0.39
6	
.	

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Module-3

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Chapter-1 MOSFETs: Biasing in MOS Amplifier Circuits

①

MOSFET (Metal oxide Semiconductor Field Effect Transistor)

Circuit Symbol:

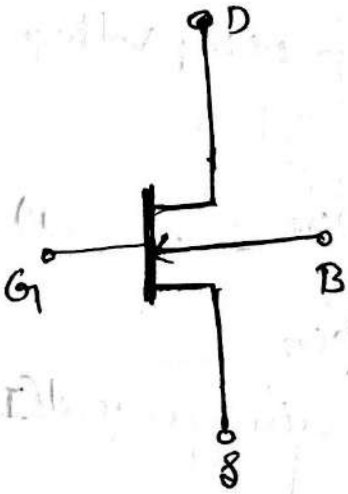


Fig (a): Circuit Symbol for n-Channel MOSFET

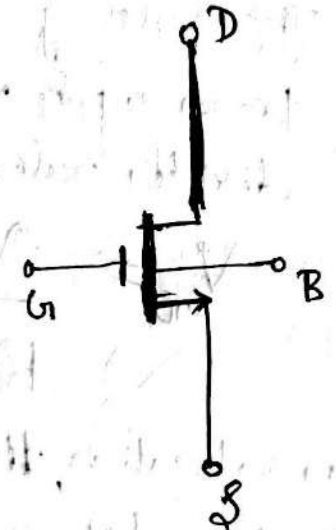
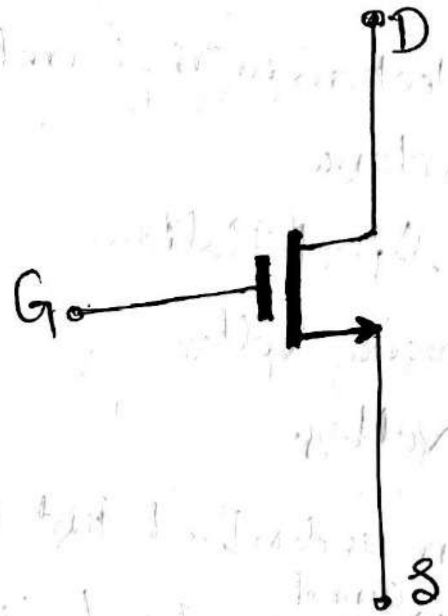


Fig (b): Modified circuit Symbol with an arrowhead on the Source.

MOSFET with Four terminals
(1) Gate
(2) Drain
(3) Body
(4) Source

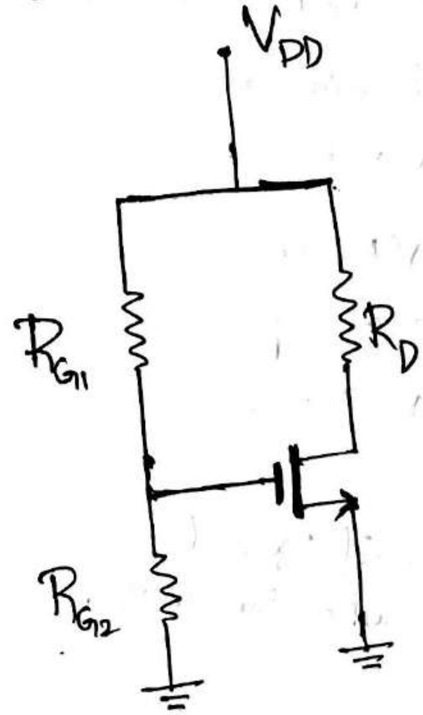


MOSFET with three terminals
(1) Drain
(2) Source
(3) Gate

Fig (c): Simplified circuit Symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

* Biasing by Fixing V_{GS}:

→ The most straight forward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required to provide desired I_D. This voltage can be derived from the power supply V_{DD} through the use of an appropriate voltage divider.



→ The value of V_{GG} is derived from power supply voltage using voltage divider rule, i.e.

$$V_{GG} = \frac{V_{DD} R_{G2}}{R_{G1} + R_{G2}} \quad \text{---} (1)$$

In saturation, the drain current (I_D) is given by,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \quad \text{---} (2)$$

where, μ_n → Mobility of electrons in 'n' channel $\left[\mu = \frac{V_d}{E}\right]$

C_{ox} → Oxide Capacitance

$\frac{W}{L}$ → Transistor Aspect Ratio

V_{GS} → Gate to Source Voltage

V_t → Threshold Voltage

→ From equation (2) we can understand that if we fix V_{GS} the I_D (drain current) cannot be fixed, since I_D also depends on $\mu_n, C_{ox}, \frac{W}{L}, V_t$. And μ_n, V_t are temperature dependent.

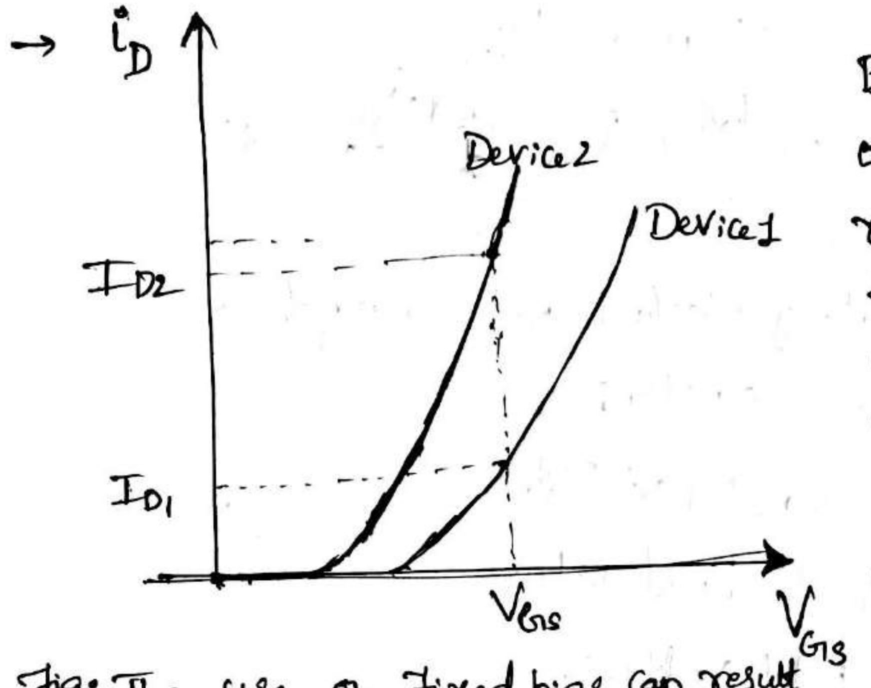


Fig: The use of fixed bias can result in a large variability in the value of I_D

Both V_t and μ_n depend on temperature, with the result that if we fix the value of V_{GS}, the drain current I_D becomes very much temperature dependent.

The figure shows V_{GS} – id curve for two MOSFET of same type (Batch)

Conclusion: Biasing by fixing V_{GS} is not good approach.

* Biasing by fixing V_G and connecting a feedback resistance to the source:

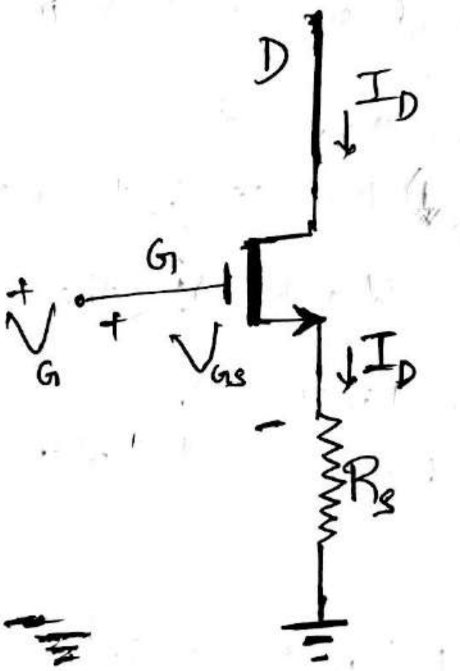


Fig: Biasing using a fixed voltage at gate, V_G & a resistance in the source lead R_S

An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G and connecting a resistance in the source lead as shown in figure.

Apply KVL to gate to source,

$$+V_G - V_{GS} - I_D R_S = 0$$

$$\boxed{V_G = V_{GS} + I_D R_S} \quad \ldots (1)$$

and

$$\boxed{V_{GS} = V_G - I_D R_S} \quad \ldots (2)$$

where R_S provides negative feedback.

The drain current is given by,

$$\boxed{I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2} \quad \cdots (3)$$

where $\mu_n \rightarrow$ Mobility of electrons in 'n' channel

$C_{ox} \rightarrow$ Oxide capacitance

$\frac{W}{L} \rightarrow$ Transistor Aspect Ratio

$V_{GS} \rightarrow$ Gate to Source Voltage

$V_t \rightarrow$ Threshold Voltage.

→ Consider equation (3) when drain current increases ($I_D\uparrow$) because of increase in $\mu_n C_{ox}\frac{W}{L}(\uparrow)$ or decrease in $V_t(\downarrow)$, the gate source voltage (V_{GS}) in equation (2) decreases. This in turn results in decrease in drain current (I_D) in equation (3).

→ Similarly when drain current in equation (3) decreases ($I_D\downarrow$) because of decrease in $\mu_n C_{ox}\frac{W}{L}(\downarrow)$ or increase in V_t (threshold voltage)$\uparrow$, the gate source voltage (V_{GS}) in equation (2) increases. This in turn results in increase in drain current (I_D) in equation (3).

→ Thus the action of R_S works to keep I_D as constant as possible. This negative feedback action of R_S gives it the name degeneration resistance,

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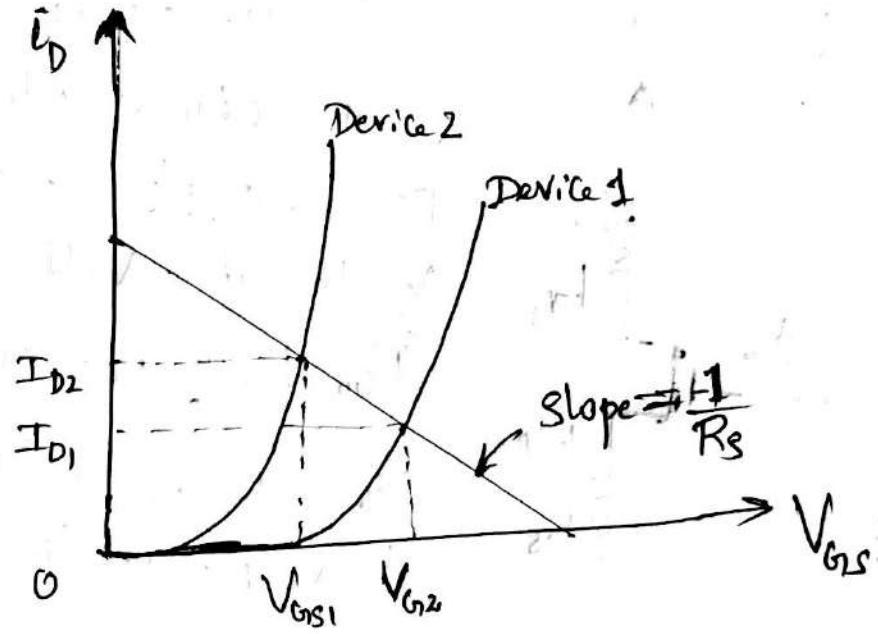


Fig: $i_d - V_{GS}$ plot demonstrating reduced variability in I_D

→ By fixing V_{GS} and connecting feedback resistance R_S the drain current (I_D) can be kept constant as much as possible.

i.e $\Delta I_D = I_{D2} - I_{D1}$ which is very small.

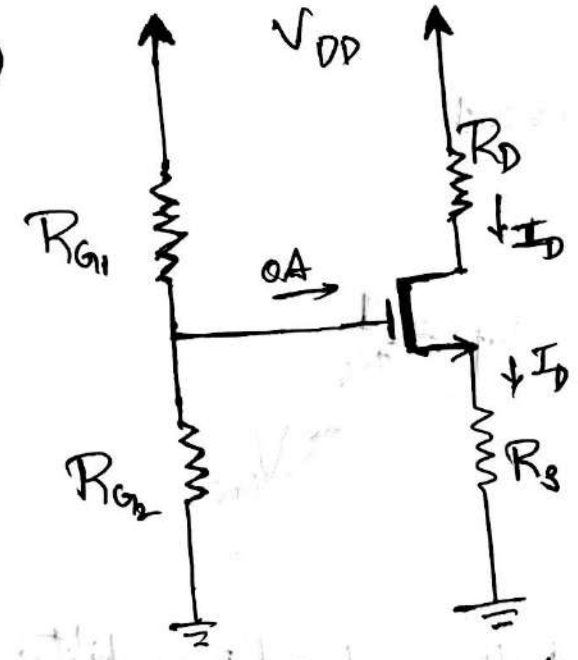
→ In general R_S increase the bias stability. i.e

$$i_d = \left(-\frac{1}{R_S}\right) V_{GS} + \frac{V_G}{R_S}$$

where $-1/R_S$ is the slope.

→ Examples of Bias with Source Degeneration:

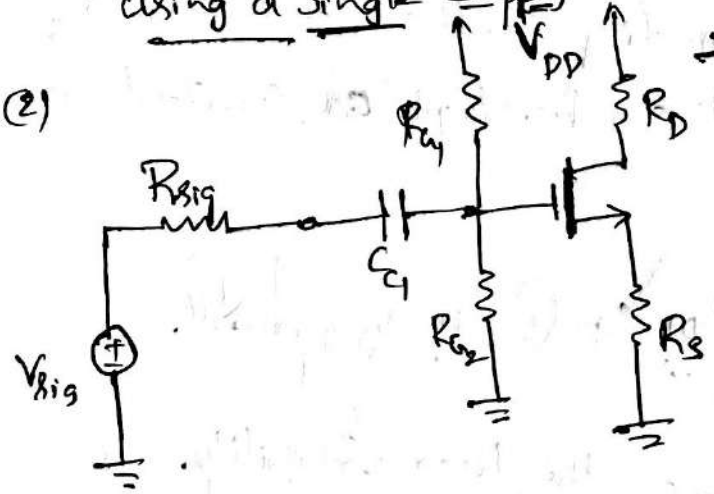
(1)



→ The circuit utilizes one power-supply V_{DD} and derives V_G through a voltage divider (R_{G1}, R_{G2}). Since $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (in the MΩ range).

Fig(a) Practical Implementation using a Single Supply

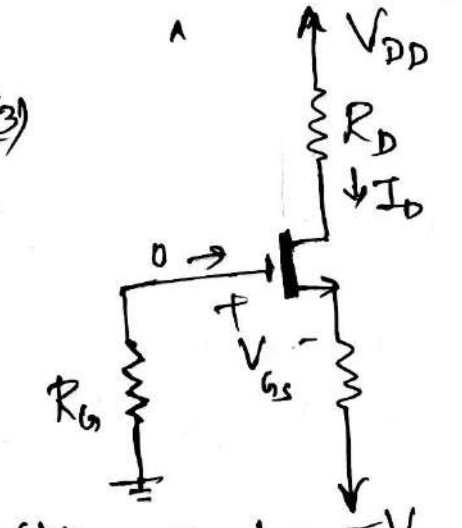
(2)



→ R_{G1}, R_{G2} allows the MOSFET to present a large input resistance to a signal source that may be connected to the gate through a coupling capacitor. C_{C1} blocks dc & thus allows us to couple the signal V_{sig} to the amplifier input without disturbing the MOSFET dc bias point.

Fig(b) Coupling of a signal Source to the gate using a capacitor C_1.

(3)



→ when two power supplies are available, the bias arrangement is as shown in Fig (c).

Apply KVL @ i/p side with $I_G = 0$ A

$$-V_{GS} - I_D R_S + V_{SS} = 0$$

$$\boxed{V_{GS} = V_{SS} - I_D R_S}$$

Fig(c) Two Supplies

* Biasing Using a Drain to Gate Feedback Resistor:

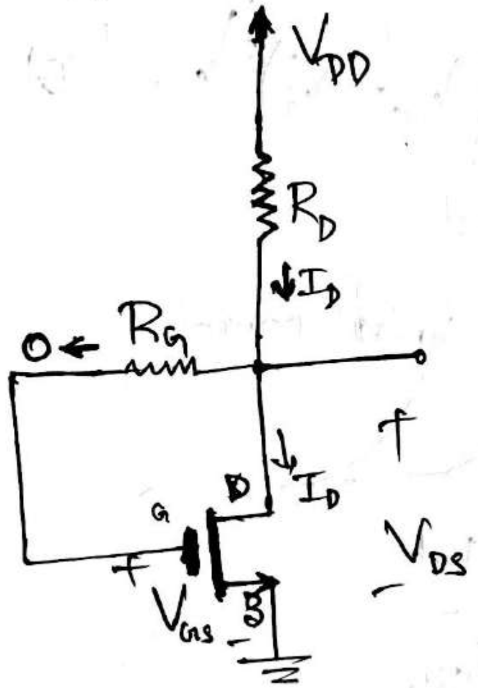


Fig: Biasing the MOSFET using a large drain-to-gate feedback resistance R_G.

→ A simple and effective discrete circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is as shown in the figure.

Apply KVL to Drain-Source loop,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\boxed{V_{DD} = I_D R_D + V_{DS}} \quad \cdots (1)$$

In this biasing the large feedback resistance R_G (in $M\Omega$) forces the dc voltage at the gate to be equal to that at the drain. i.e

$$\boxed{V_G = V_D} \quad \cdots (2)$$

W.K.T $\quad V_{GS} = V_G - V_S = V_D - V_S = V_{DS} \quad \cdots$

$$\boxed{V_{GS} = V_{DS}} \quad \cdots (3)$$

Substitute equation (3) in equation (1) then

$$V_{DD} = I_D R_D + V_{GS}$$

$$\boxed{V_{GS} = V_{DD} - I_D R_D} \quad \cdots (4)$$

→ In saturation the drain current is given by

$$\boxed{I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2} \quad \ldots (5)$$

where,

μ_n → Mobility of electrons in n channel

C_{ox} → Oxide Capacitance

$\frac{W}{L}$ → Transistor Aspect Ratio

V_{GS} → Gate to Source Voltage

V_t → Threshold Voltage

→ If drain current (I_D) in equation (5) changes for some reason, i.e increases (↑) because of increase in $\mu_n C_{ox}\frac{W}{L}$ or V_t (↓) the gate source voltage (V_{GS}) in equation (4) has to decrease, this in turn results in decrease of drain current in Eqn (5).

→ Similarly when I_D decreases because of decrease in $\mu_n C_{ox}\frac{W}{L}$ or increase in V_t, the gate source voltage V_{GS} in equation (4) has to increase, this in turn results in increase of drain current in equation (5).

→ The negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.

* Small Signal Operation and Models:

The linear amplification can be obtained by two methods,

(a) Biasing the MOSFET to operate in saturation region.

(b) By keeping the input signal small.

→ We already studied about biasing the MOSFET to obtain linear amplification.

→ To understand small signal operation let us consider Common-Source amplifier circuit shown in below figure. In the below circuit MOS transistor is biased by applying a dc voltage V_{GS}, and the input signal to be amplified, v_{gs} is shown superimposed on the dc bias voltage V_{GS}. The output voltage is taken at the drain.

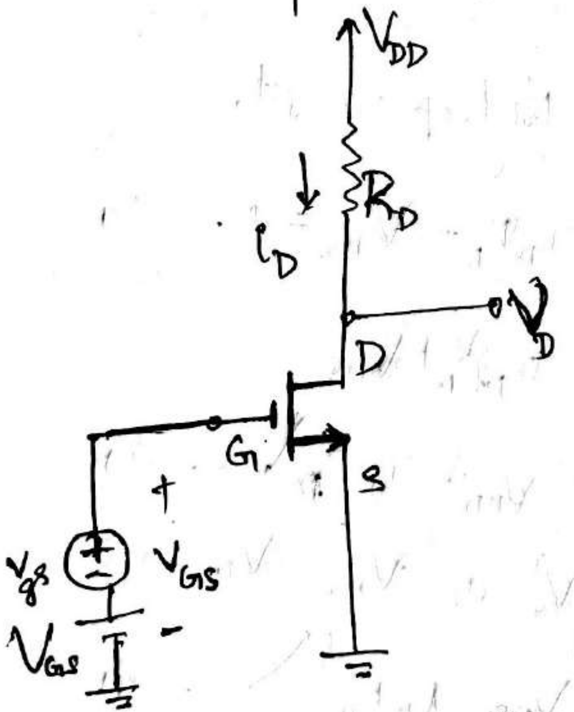


Fig 1: Conceptual circuit to study the operation of the MOSFET as small signal Amplifier

It is necessary to analyze or determine the following parameter for small signal amplifier.

(i) The DC Bias point

(ii) The signal current in the drain terminal

(iii) The voltage gain

(iv) Small-Signal Equivalent circuit models

(v) The transconductance g_m.

(i) The DC Bias point:

The dc bias current I_D can be found by setting the signal v_{gs} to zero in Figure 1. (previous page), i.e

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2 \quad \cdots (1)$$

Let $k_n' = \mu_n C_{ox}$ then equation (1) becomes

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2 \quad \cdots (2)$$

where,
$\mu_n \rightarrow$ Mobility of electrons in n channel
$C_{ox} \rightarrow$ Oxide Capacitance
$\frac{W}{L} \rightarrow$ Transistor Aspect Ratio
$V_{GS} \rightarrow$ Gate to Source voltage
$V_t \rightarrow$ Threshold Voltage.

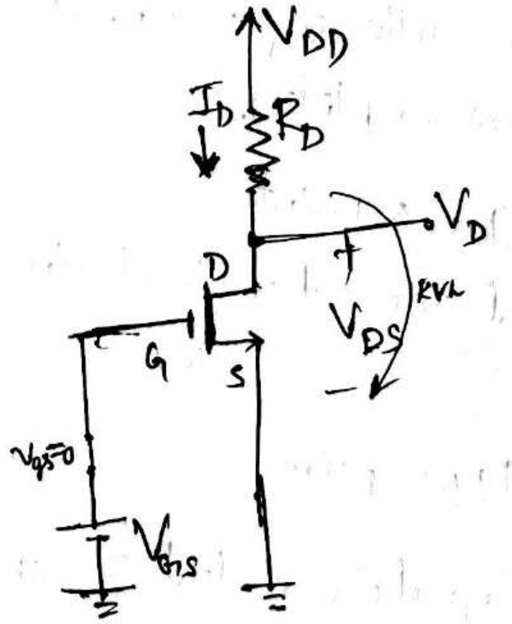


Fig 2: Setting input signal $v_{gs}=0$ to find dc bias current.

→ Apply KVL to loop we get,

$$V_{DD} - I_D R_D - V_{DS} = 0 \quad \cdots (3)$$

$$V_{DD} = I_D R_D + V_{DS}$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \quad \cdots (4)$$

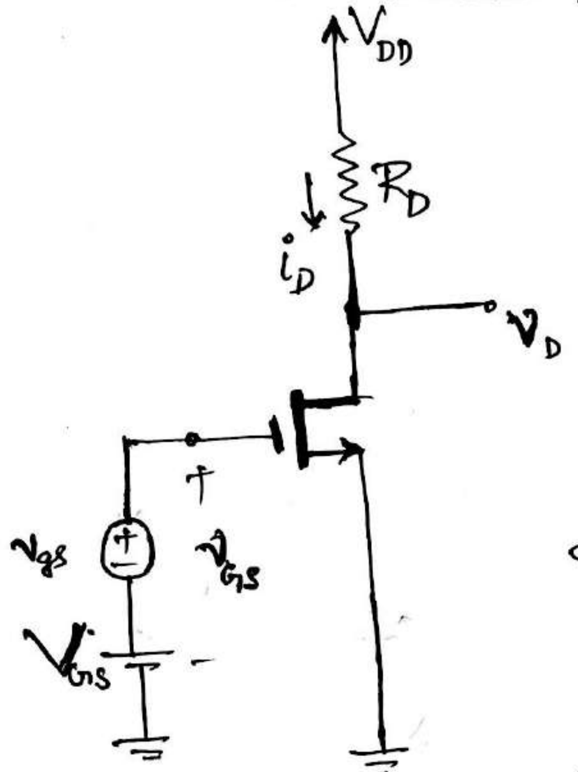
Since $V_S = 0$, $V_{DS} = V_D$

$$\boxed{V_D = V_{DD} - I_D R_D} \quad \cdots (5)$$

To ensure saturation operation, we must have

$$\boxed{V_D > V_{GS} - V_t} \quad \cdots (6)$$

(ii) The Signal current in the Drain Terminal:



Fig(3): MOSFET as a small signal amplifier

The input signal applied is v_{gs} and total instantaneous gate-to source voltage is given by v_{GS},

$$v_{GS} = v_{gs} + V_{GS} \quad \cdots (1)$$

which results in a total instantaneous drain current i_D which given by

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (v_{GS} - V_t)^2 \quad \cdots\cdots (2)$$

Substituting equation (2) in (1) we get,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (v_{gs} + V_{GS} - V_t)^2$$

Rewriting above equation as

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (\underbrace{V_{GS} - V_t}_{a} + \underbrace{v_{gs}}_{b})^2$$

W.K.T $(a+b)^2 = a^2 + 2ab + b^2$ & applying it to above equation we get,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} \left((V_{GS} - V_t)^2 + 2(V_{GS} - V_t) v_{gs} + v_{gs}^2 \right)$$

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + \frac{1}{\cancel{2}} K_n' \frac{W}{L} \cancel{2}(V_{GS} - V_t) v_{gs} + \frac{1}{2} K_n' \frac{W}{L} v_{gs}^2$$

$$i_D = \underbrace{\frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2}_{I} + \underbrace{K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}}_{II} + \underbrace{\frac{1}{2} K_n' \frac{W}{L} v_{gs}^2}_{III} \quad \cdots\cdots (3)$$

There are 3 terms in the R.H.S of equation (3), the first term recognized as the dc bias current I_D i.e

$$I_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 \quad \ldots (a) \quad \{1^{st} \text{ term in Equation } 3\}$$

the second term represents a current component that is proportional to the input signal v_{gs} i.e

$$i_d = K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} \quad \ldots (b) \quad \{2^{nd} \text{ term in Equation } 3\}$$

The third current component that is proportional to the square of the input signal. The last (3^{rd}) component in equation (3) represents non linear distortion & it can be reduced be keeping the input signal small (v_{gs}). i.e.

$$\frac{1}{2} \cancel{K_n'} \frac{W}{L} v_{gs}^{\cancel{2}} << K_n' \frac{W}{L} (V_{GS} - V_t) \cancel{v_{gs}}$$

$$v_{gs} << 2(V_{GS} - V_t)$$

i.e $$\boxed{v_{gs} << 2V_{ov}} \quad \ldots (4)$$

$V_{ov} \rightarrow$ overdrive voltage

If the input signal is small (i.e $v_{gs} << 2V_{ov}$) then the third term in equation (3) can be neglected, & rewritten as

$$\boxed{i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}} \quad (5)$$

from (a) & (b) equation (5) can be written as

$$\boxed{i_D = I_D + i_d} \quad \ldots (6)$$

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The parameter that relates i_d and v_{gs} is the MOSFET transconductance g_m i.e

$$g_m = \frac{i_d}{v_{gs}} \quad \text{---- (7)}$$

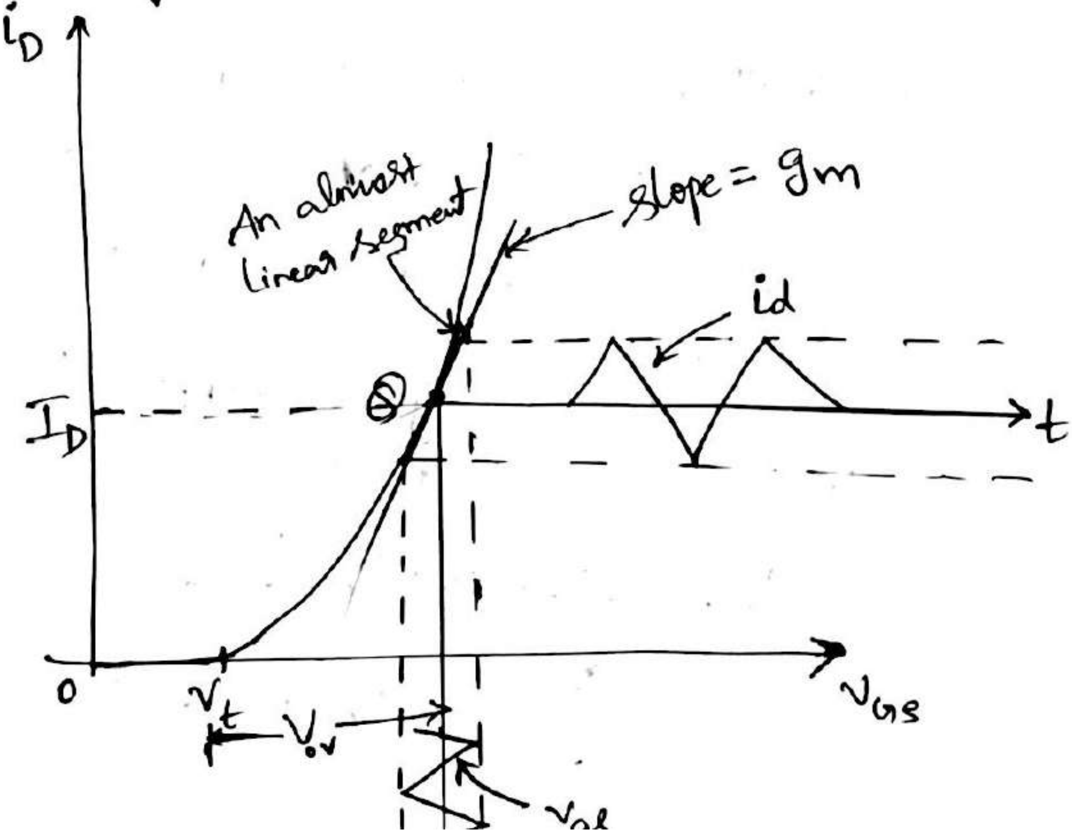
from equation (6)

$$i_d = K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$ & substitute in Eqn (7)

$$g_m = K_n' \frac{W}{L} (V_{GS} - V_t) \frac{\cancel{v_{gs}}}{\cancel{v_{gs}}}$$

$$\boxed{g_m = K_n' \frac{W}{L} (V_{GS} - V_t)} \quad \text{- (8)}$$

→ Below figure presents graphical interpretation of the small signal operation of the MOSFET amplifier



(iii) The voltage Gain:

From the DC bias point W.K.T

$$V_D = V_{DD} - I_D R_D \quad \cdots (1)$$

voltage Gain A_v is given by

$$A_v = \frac{v_d}{v_{gs}} \quad \cdots\cdots (2)$$

under the small-signal condition the small drain voltage v_D is given by

$$v_D = V_{DD} - i_D R_D \quad \cdots (3)$$

W.K.T $i_D = I_D + i_d$

$$v_D = V_{DD} - (I_D + i_d) R_D$$

$$v_D = V_{DD} - I_D R_D - i_d R_D \quad \cdots (4)$$

And small drain voltage v_D can also be written as,

$$v_D = V_D + v_d \quad \cdots (5)$$

Equating equation (4) & (5) we get,

$$V_D + v_d = V_{DD} - I_D R_D - i_d R_D \quad \cdots (6)$$

Substitute equation (1) in (6)

$$\cancel{V_{DD}} - \cancel{I_D R_D} + v_D = \cancel{V_{DD}} - \cancel{I_D R_D} - i_d R_D$$

$$\boxed{v_D = -i_d R_D} \quad \cdots (7)$$

→ When the MOSFET characteristics in saturation, the drain current depend on V_{DS} in a linear manner & such model will have finite resistance r_o between drain & source which is given by,

$$r_o = \frac{|V_A|}{I_D} \quad \text{--- (1)}$$

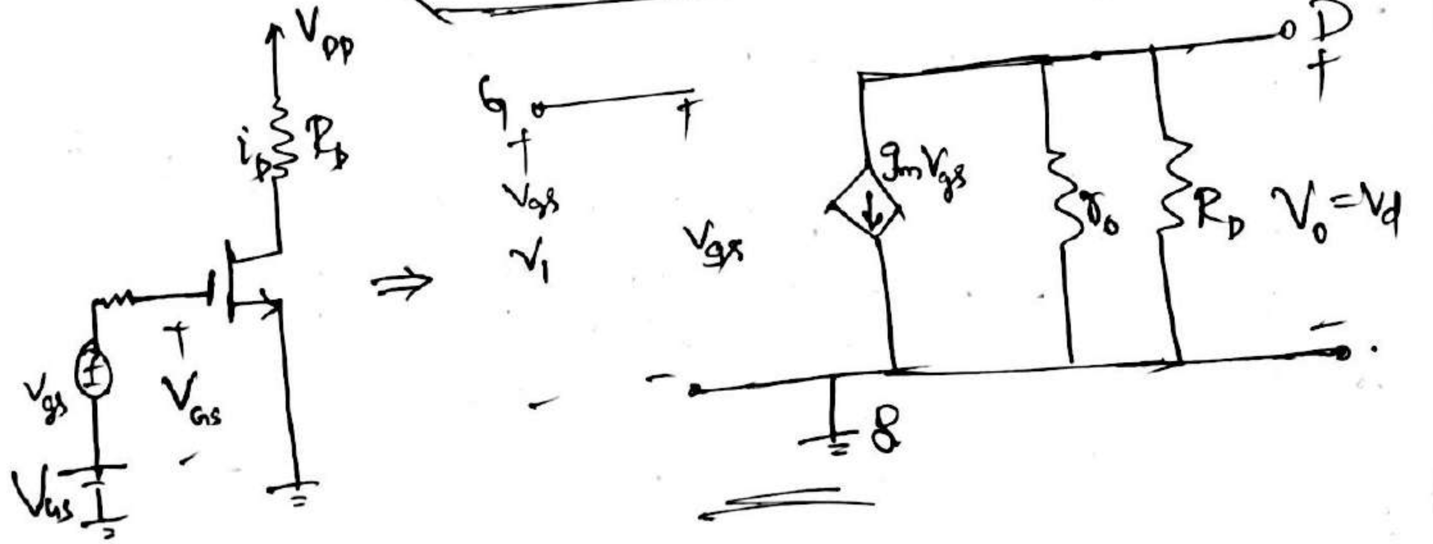
where $|V_A|$ → MOSFET parameter proportional to the MOSFET channel length.

The value of the dc drain current is,

$$\boxed{I_D = \frac{1}{2} K_n' \frac{W}{L} V_{ov}^2} \quad \text{--- (2)}$$

→ If r_o is finite then the voltage gain A_v is given by,

$$\boxed{A_v = -g_m (R_D \| r_o)} \quad \text{--- (3)}$$



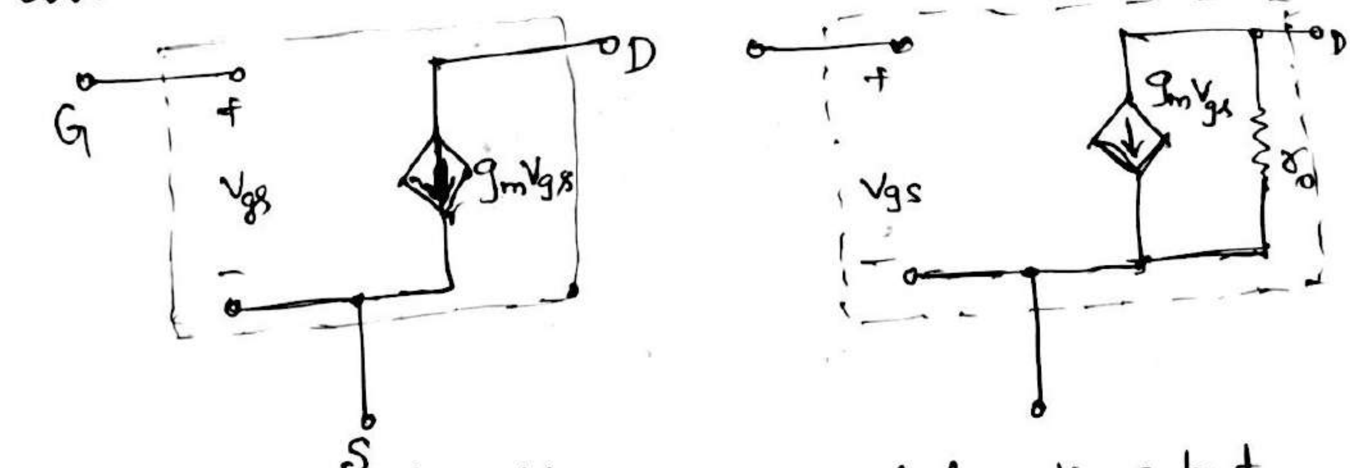
Substitute equation (7) in equation (2) we get,

$$A_v = \frac{-i_d R_D}{v_{gs}}$$

where $\frac{i_d}{V_{gs}}$ is the transconductance "g_m"

$$\boxed{A_v = -g_m R_D} \quad \text{--- (8)}$$

(iv) Small-Signal Equivalent Circuit Models:



Fig(a): Small-signal models for the MOSFET

Fig(b): Including the output resistance r_o

→ The input provided for the circuit is V_{gs} between gate & source which provides a current $g_m V_{gs}$ at the drain terminals.

→ The input resistance of this controlled source is very high (Infinite). The output resistance at drain is also high.

→ The signal current of an ideal constant dc current source will always be zero an ideal constant dc current source can be replaced by open circuit in the small signal equivalent circuit

(v) Transconductance (g_m)

We already know that for small signal the transconductance is given by,

$$g_m = K_n'\left(\frac{W}{L}\right)(V_{GS}-V_t) \quad \cdots (1)$$

or

$$g_m = K_n' \frac{W}{L} V_{ov} \quad \cdots\cdots (2)$$

where $K_n' = \mu_n C_{ox}$

We need to derive alternative expression for g_m, because from equation (1) we can understand that $g_m \propto K_n' \frac{W}{L}$; which means to obtain high $\uparrow g_m$ the device must be short & wide.

→ W.K.T (1)

$$I_D = \frac{1}{2} K_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)^2$$

$$K_n'\left(\frac{W}{L}\right) = \frac{2I_D}{(V_{GS}-V_t)^2} \quad \cdots (3)$$

Substituting equation (3) in equation (1) we get,

$$g_m = \frac{2I_D}{(V_{GS}-V_t)^{2}} \times (V_{GS}-V_t)$$

$$g_m = \frac{2I_D}{V_{GS}-V_t} \qquad g_m = \frac{2I_D}{V_{ov}} \quad \cdots (4)$$

From equation (4) we eliminated the dependency of g_m on $\frac{W}{L}$ or K_n'.

(b) W.K.T $I_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2$

$$(V_{GS} - V_t)^2 = \frac{2 I_D}{K_n' \left(\frac{W}{L}\right)} \cdots$$

$$(V_{GS} - V_t) = \sqrt{\frac{2 I_D}{K_n' \left(\frac{W}{L}\right)}} \cdots\cdots (5)$$

Substitute equation (5) in Equation (1) we get,

$$g_m = K_n' \left(\frac{W}{L}\right) \times \sqrt{\frac{2 I_D}{K_n' \left(\frac{W}{L}\right)}}$$

$$\boxed{g_m = \sqrt{K_n' \frac{W}{L}} \times \sqrt{2 I_D}} \cdots (6)$$

From the above expression we can say that,

(i) For a given MOSFET, g_m is proportional to the square root of the dc bias current.

(ii) At a given bias current, g_m is proportional to $\sqrt{W/L}$.

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SYLLABUS

Module -1

Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis With linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh.

Module -2

Network Theorems: Superposition, Reciprocity, Millman‘s theorems, Thevinin‘s and Norton‘s theorems and Maximum Power transfer theorem.

Module -3

Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.

Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.

Module -4

Resonant Circuits: Series and parallel resonance, frequency- response of series and Parallel circuits, Q–Factor, Bandwidth.

Module -5

Two port network parameters: Definition of z, y, h and transmission parameters, modeling with these parameters, relationship between parameters sets.

Text Books:

1. M.E. Van Valkenberg (2000), "Network analysis", Prentice Hall of India, 3rd edition, 2000, ISBN: 9780136110958.

2. Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677.

Reference Books:

1. Hayt, Kemmerly and Durbin "Engineering Circuit Analysis", TMH 7th Edition, 2010.

2. J. David Irwin /R. Mark Nelms, "Basic Engineering Circuit Analysis", John Wiley, 8th edition, 2006.

3. Charles K Alexander and Mathew N O Sadiku, "Fundamentals of Electric Circuits", Tata McGraw-Hill, 3rdEd, 2009.

Module 1: Basic Circuit Concepts

Circuit Elements:

Any two terminal circuit components are called circuit elements.

Types:

1) Active elements: Deliver the energy to the network

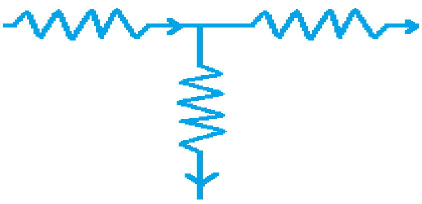
Examples: Voltage Source, Current Source

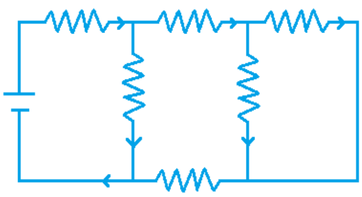
2) Passive elements: Absorb the energy from the network

Examples: Resistors, Capacitors, Inductors

Network:

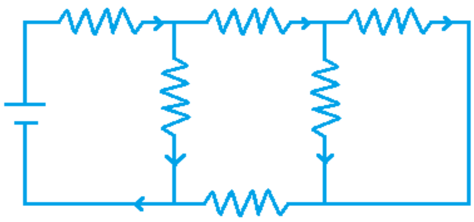
Interconnection of two are more circuit elements is called network





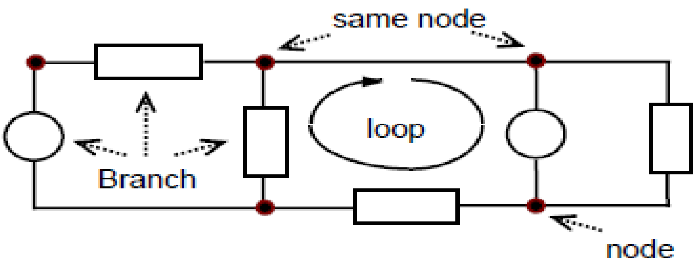
Circuit:

Network with at least one closed path is called circuit



Note: Every circuit is a network but all networks are not circuits

Network Terminology



- **Branch**

  A branch represents a single element, such as a resistor or a battery

- **Node**

  A node is the point or junction in a circuit connecting two or more branches or circuit elements. The node is usually indicated by a dot (**.**) in a circuit

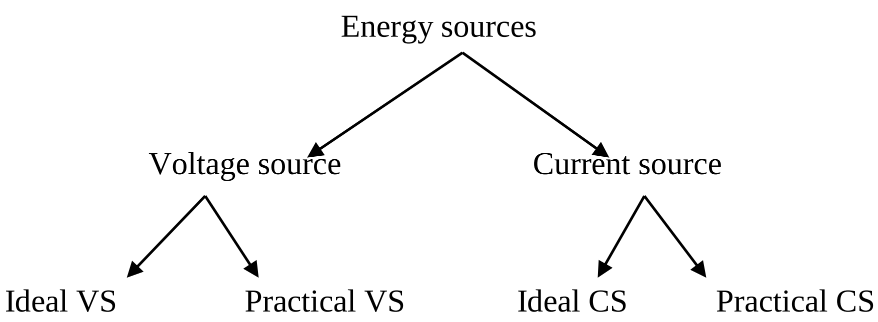
- **Loop**

  A loop is any closed path in a circuit

- **Mesh**

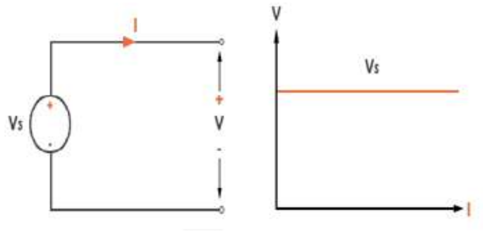
  It is a loop that contains no other loop within it.

Energy sources:



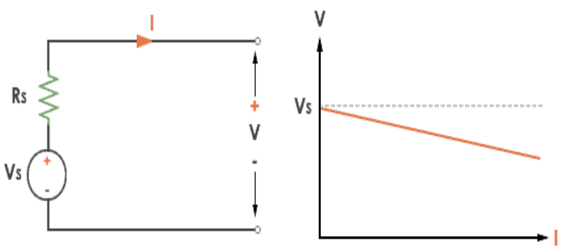
Ideal VS:

- Whose internal resistance is zero
- Irrespective of the load current, terminal voltage is constant



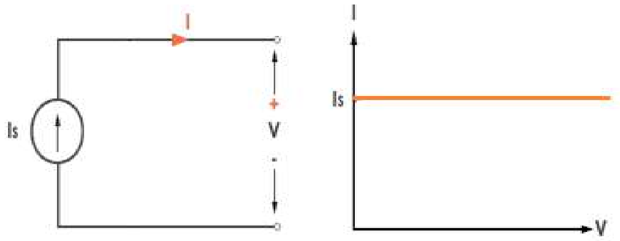
Practical VS:

- Which has finite internal resistance and connected in series with the source
- Terminal voltage decreases with increase in load current



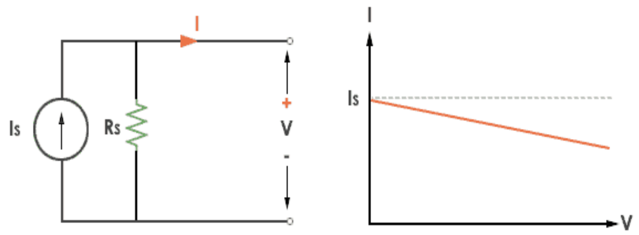
Ideal CS:

- Has infinite internal resistance
- Irrespective of the load voltage, terminal current is constant



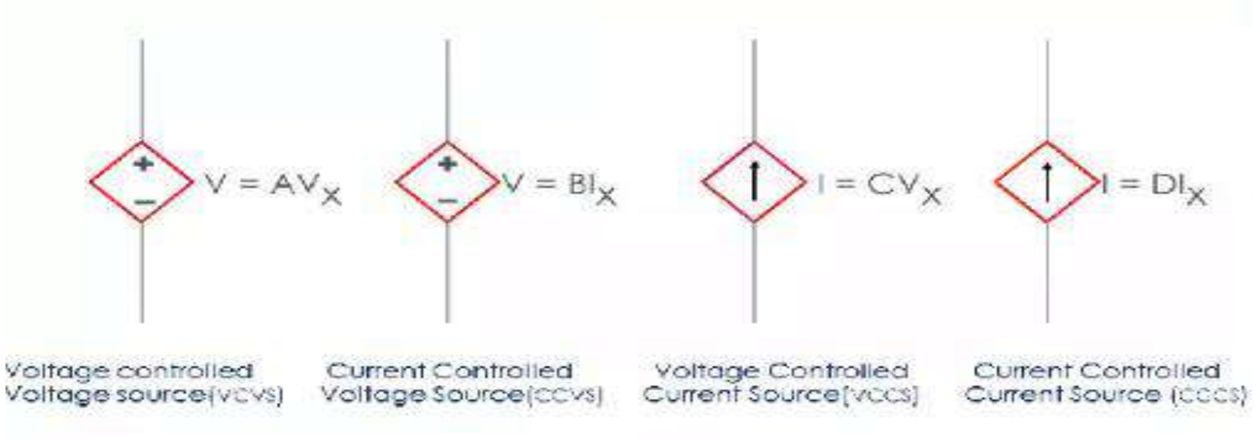
Practical CS:

- Has finite internal resistance
- Terminal current decreases with increase in load current



Dependent sources/ Controlled sources:

- Sources whose voltage/current depends on voltage/current that appears at some other location of the network.
- Represented by diamond symbol
- 4 types



Classification of Networks:

1) Linear and Non linear networks

A ***Linear circuit*** is one whose parameter are constant i.e., they do not change with voltage or current.

Examples: Network consisting of R, L and C

A ***Non linear circuit*** is one whose parameters change with voltage or current.

Examples: Network consisting of diode and transistor

2) **Unilateral and Bilateral networks**

The circuit whose properties or characteristics change with the direction of its operation is said to be ***Unilateral***.

Examples: A diode rectifier is a unilateral, because it cannot perform rectification in both directions.

A ***Bilateral circuit*** is one whose properties or characteristics are the same in either direction.

Examples: R, L & C.

3) Active and Passive network

Network consisting of only passive elements is called **Passive** network

Examples: Network consisting of R, L and C

Network consisting of at least one active element is called **Active** network

Examples: Network consisting VS and CS

4) Lumped and Distributed network

Network in which elements are physically separable is called **Lumped** network.

Examples: R, L and C

Network in which elements cannot be physically separable is called **Distributed** network.

Examples: Transmission lines having R, L, C all along their length.

Source Transformation

Source Transformation involves the transformation of voltage source to its equivalent current source and vice-versa.

Consider a voltage source with series resistance R and a current source with same resistance R in parallel as shown below.

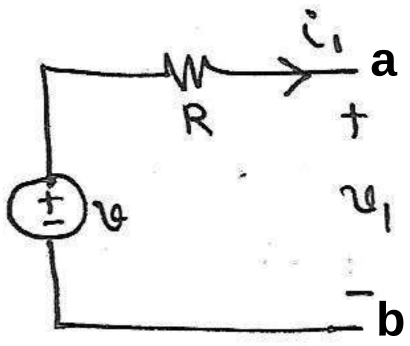


Fig: Voltage source

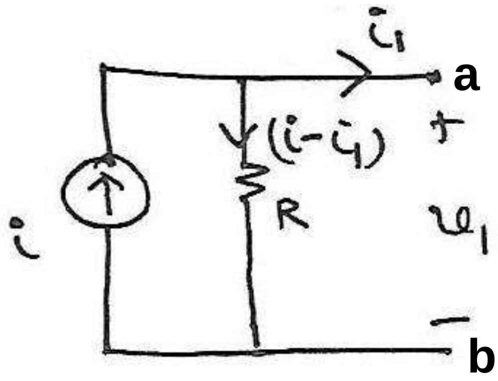


Fig: Current source

The terminal voltage and current relationship in the case of voltage source is;

$v_1 = v - i_1 R$ …… (1)

The terminal voltage and current relationship in the case of current source is;

$i_1 = i - v_1 / R$

$v_1 = i R - i_1 R$ …… (2)

If the voltage source above has to be equivalently transformed to or represented by a current source then the terminal voltages and currents have to be same in both cases.

This means eqn. (1) should be equal to eqn. (2).

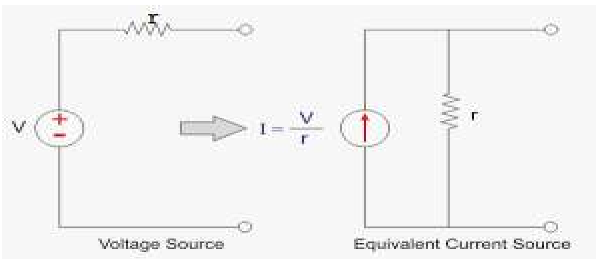
This implies,

$v = i R$

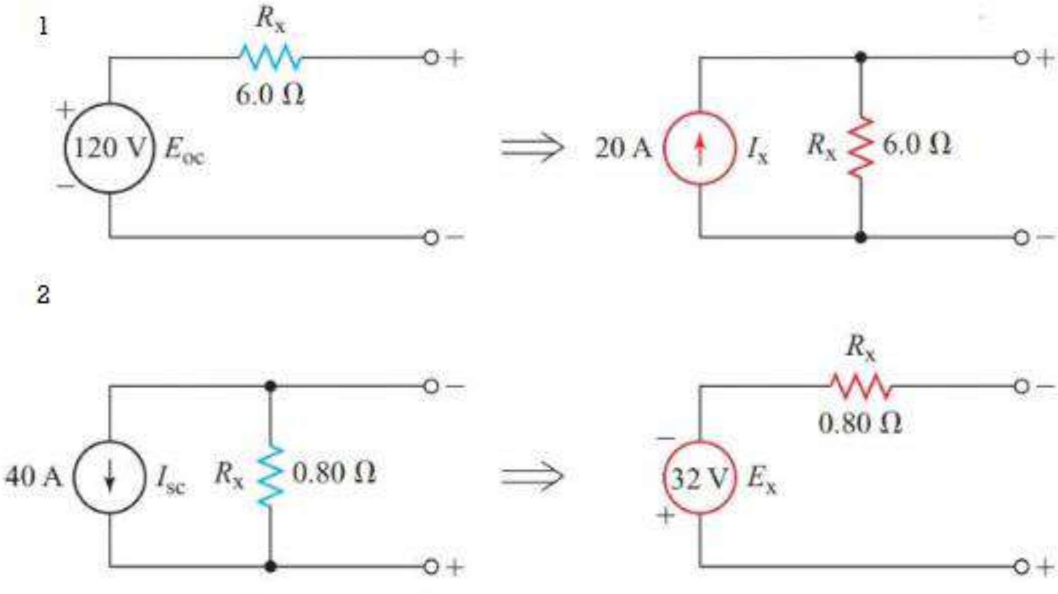
or

$i = v / R$…(3)

If eqn.(3) holds good, then the voltage source above can be equivalently transformed to or represented by, the current source shown above and vice-versa.

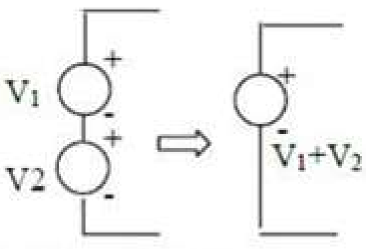


Examples:

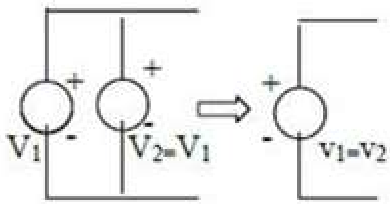


Combination of sources:

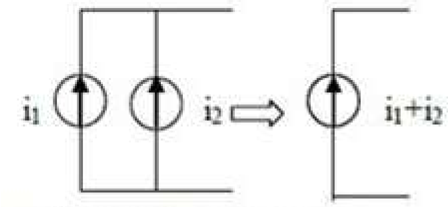
1. Two ideal voltage sources in series



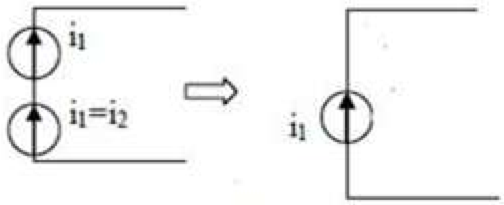
2. Two ideal voltage sources in parallel



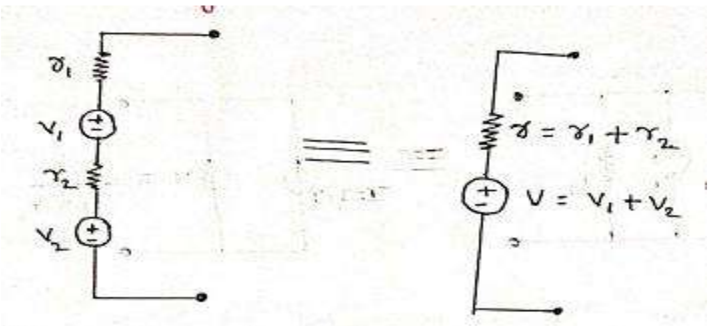
3. Two ideal current sources in parallel



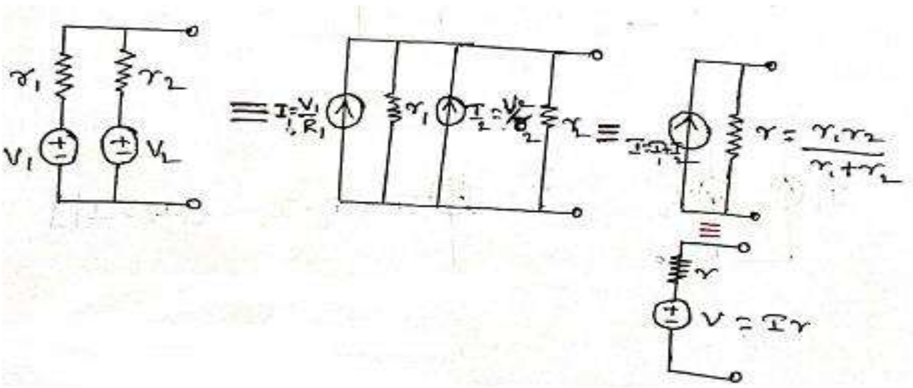
4. Two ideal current sources in series



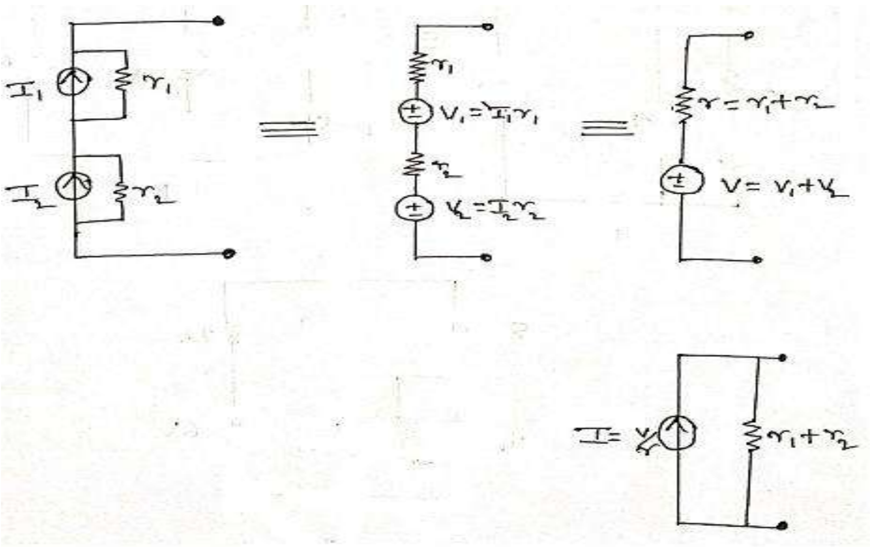
5. Two practical voltage sources in series



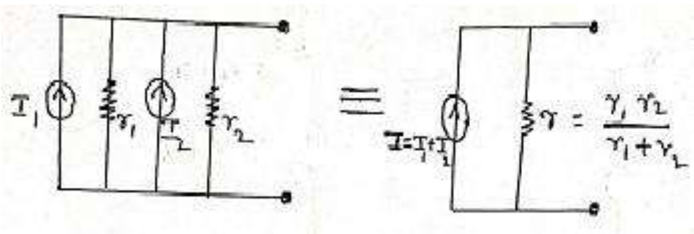
6. Two practical voltage sources in parallel



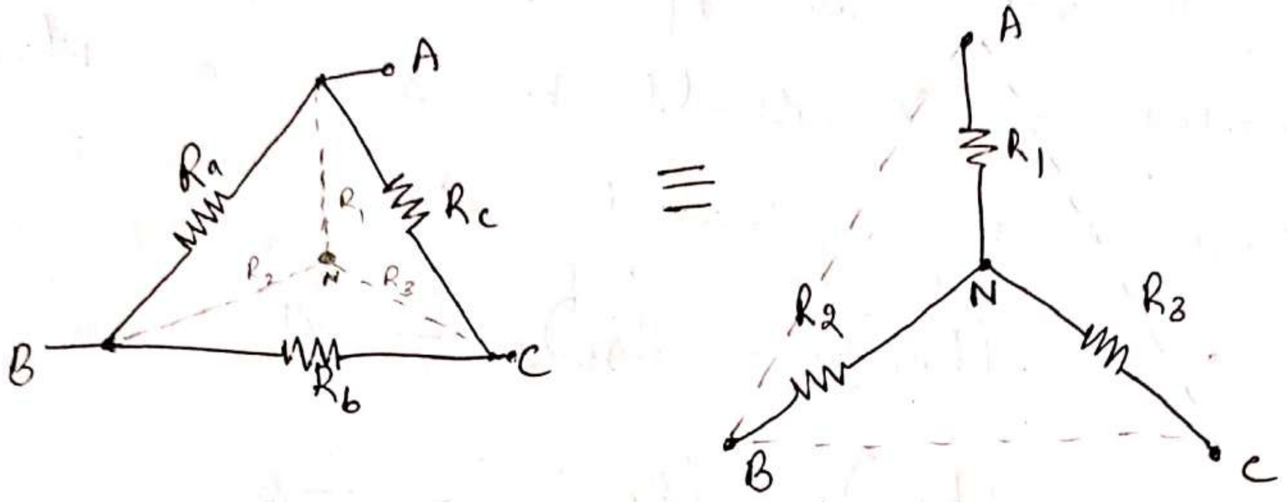
7. Two practical current sources in series



8. Two practical current sources in parallel



Star-Delta transformation (Δ - Y) :-



Let R_a, R_b & R_c be the elements connected in Δ n/w b/n the terminals A, B & C. Let the n/w consisting of R_1, R_2 & R_3 be the equivalent Y n/w across the same terminals A, B & C.

For converting the given Δ n/w into equivalent Y n/w, it is necessary to derive the relations for R_1, R_2 & R_3 in-terms of R_a, R_b & R_c.

Ully to convert the known Y into equivalent Δ n/w, it is necessary to derive the relation for R_a, R_b & R_c in terms of R_1, R_2 & R_3.

i) Delta to Star transformation :-

The resistance b/n A & B when connected in Y should be same as when connected in equivalent Δ.

i.e, $(R_{AB})_Y = (R_{AB})_\Delta$ —— ①

$(R_{BC})_Y = (R_{BC})_\Delta$ —— ②

$(R_{CA})_Y = (R_{CA})_\Delta$ —— ③

$$(R_{AB})_Y = R_1 + R_2$$

$$(R_{AB})_\Delta = \frac{R_a(R_b+R_c)}{R_a+R_b+R_c}$$

from ①

$$R_1+R_2 = \frac{R_a(R_b+R_c)}{R_a+R_b+R_c} \quad \text{—— ④}$$

lly $$R_2+R_3 = \frac{R_b(R_c+R_a)}{R_a+R_b+R_c} \quad \text{—— ⑤}$$

$$R_3 + R_1 = \frac{R_c(R_a + R_b)}{R_a + R_b + R_c} \quad \text{——} (6)$$

→ (4) − (5) gives.

$$R_1 + \cancel{R_2} - \cancel{R_2} - R_3 = \frac{R_a(R_b + R_c) - R_b(R_c + R_a)}{R_a + R_b + R_c}$$

$$R_1 - R_3 = \frac{R_a \cancel{R_b} + R_a R_c - R_b R_c - \cancel{R_b} R_a}{R_a + R_b + R_c}$$

$$R_1 - R_3 = \frac{R_a R_c - R_b R_c}{R_a + R_b + R_c} \quad \text{——} (7)$$

→ (6) + (7) gives.

$$\cancel{R_3} + R_1 + R_1 - \cancel{R_3} = \frac{R_c R_a + \cancel{R_c R_b} + R_a R_c - \cancel{R_b R_c}}{R_a + R_b + R_c}$$

$$\cancel{2} R_1 = \frac{\cancel{2} R_a R_c}{R_a + R_b + R_c}$$

$$\boxed{R_1 = \frac{R_a R_c}{R_a + R_b + R_c}} \quad \text{——} (8)$$

$$\text{ully } \quad R_2 = \frac{R_b R_a}{R_a + R_b + R_c} \quad \text{—— (9)} \quad \& \quad R_3 = \frac{R_c R_b}{R_a + R_b + R_c} \quad \text{—— (10)}$$

ii) Star to delta transformation :-

To get the expressions for R_a, R_b & R_c in terms of R_1, R_2 & R_3, eqns (8), (9) & (10) are used.

(8) × (9) gives
$$R_1 \times R_2 = \frac{R_a^2 R_b R_c}{(R_a + R_b + R_c)^2} \quad \text{—— (11)}$$

(9) × (10) gives
$$R_2 \times R_3 = \frac{R_a R_b^2 R_c}{(R_a + R_b + R_c)^2} \quad \text{—— (12)}$$

(10) × (8) gives
$$R_3 \times R_1 = \frac{R_a R_b R_c^2}{(R_a + R_b + R_c)^2} \quad \text{—— (13)}$$

→ (11) + (12) + (13) gives

$$R_1 R_2 + R_2 R_3 + R_3 R_1 = \frac{R_a^2 R_b R_c + R_a R_b^2 R_c + R_a R_b R_c^2}{(R_a + R_b + R_c)^2}$$

$$R_1R_2 + R_2R_3 + R_3R_1 = \frac{R_aR_bR_c\left[R_a+R_b+R_c\right]}{(R_a+R_b+R_c)^2}$$

$$= \frac{R_aR_bR_c}{(R_a+R_b+R_c)}$$

R_3

from eqn (10) $R_3 = \frac{R_bR_c}{R_a+R_b+R_c}$

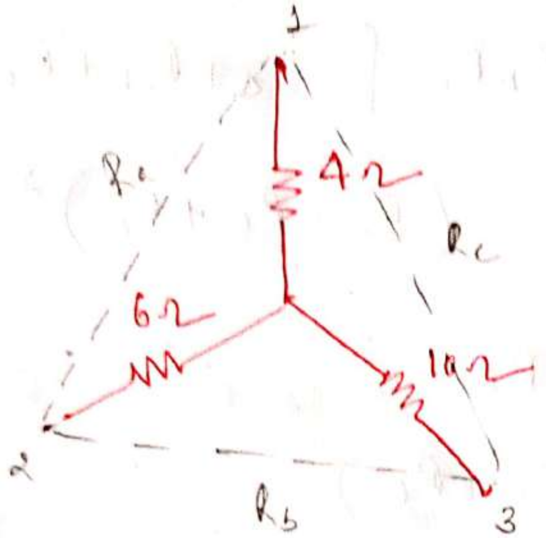
$\therefore \quad R_1R_2 + R_2R_3 + R_3R_1 = R_a R_3$

$$\Longrightarrow \boxed{R_a = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_3}}$$

llly $\boxed{R_b = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_1}}$

$$\boxed{R_c = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_2}}$$

1)



$$R_a = \frac{4\times6 + 6\times10 + 10\times4}{10}$$

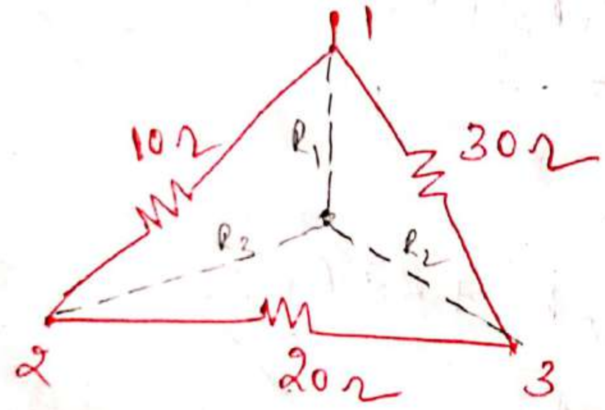
$$\hookrightarrow = 12.4\,\Omega$$

$$R_b = \frac{4\times6 + 6\times10 + 10\times4}{4}$$

$$\hookrightarrow = 31\,\Omega$$

$$R_c = \frac{124}{6} = 20.66\,\Omega.$$

2)



$$R_1 = \frac{10\times 30}{10+30+20}$$

$$R_1 = 5\,\Omega$$

$$R_2 = \frac{30\times 20}{10+30+20}$$

$$R_2 = 10\,\Omega$$

$$R_3 = \frac{10\times 20}{10+20+30} = \underline{\underline{3.33\,\Omega}}$$

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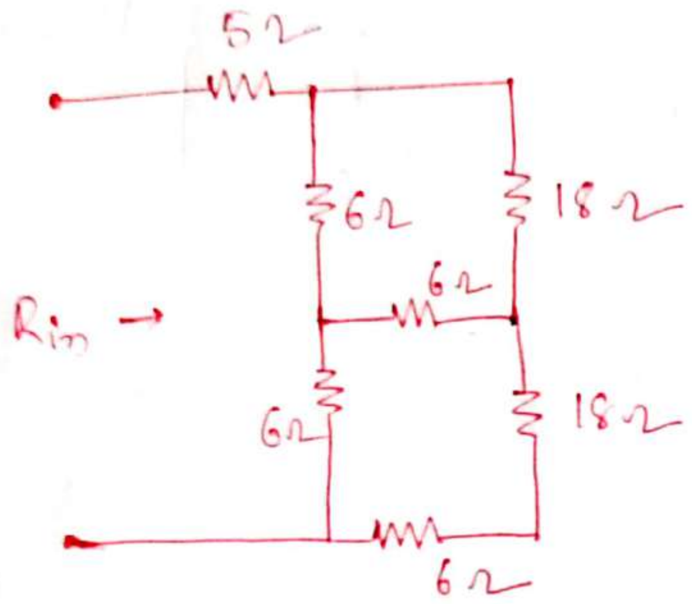
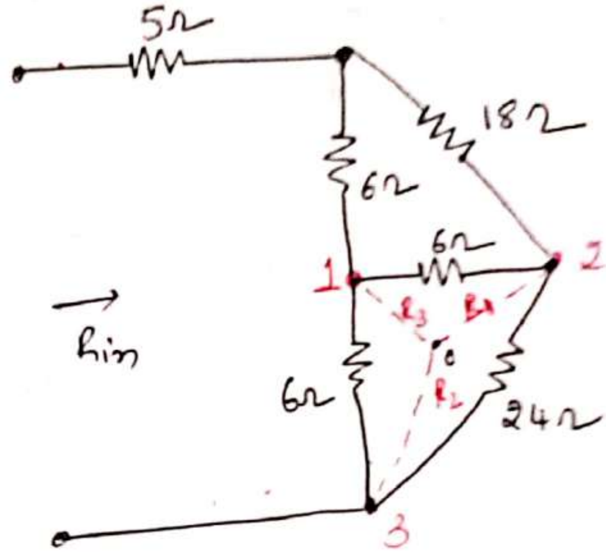
1) Determine R_{in} using Star Delta transformation in the n/w shown below:

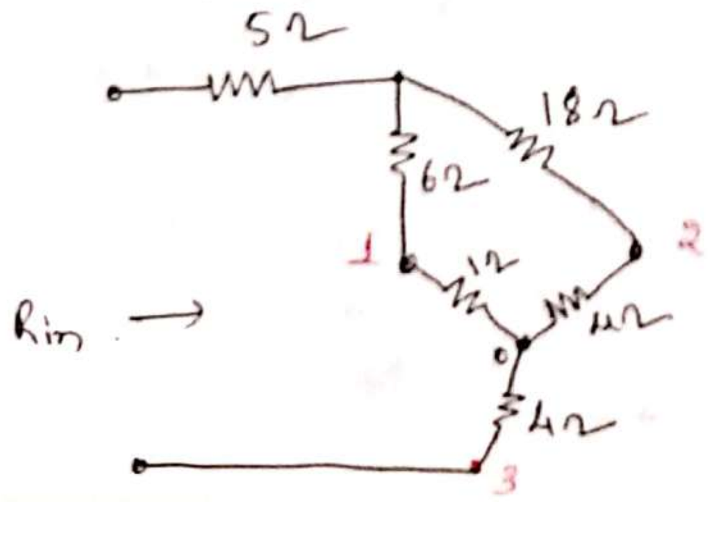


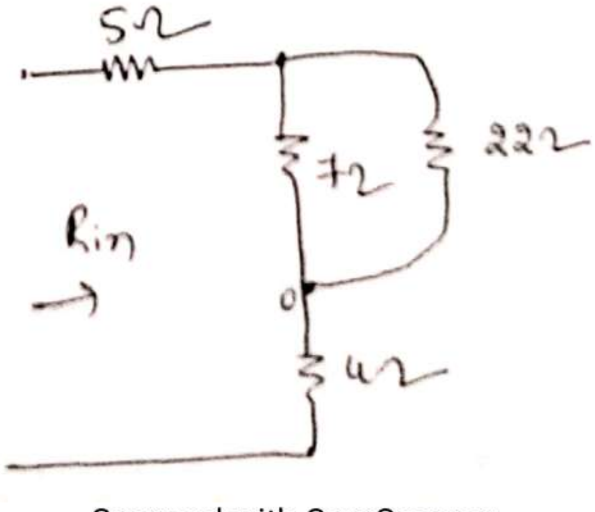


$$R_1 = \frac{24 \times 6}{6+6+24} = 4\Omega$$

$$R_2 = \frac{24 \times 6}{6+6+24} = 4\Omega$$

$$R_3 = \frac{6 \times 6}{6+6+24} = 1\Omega$$





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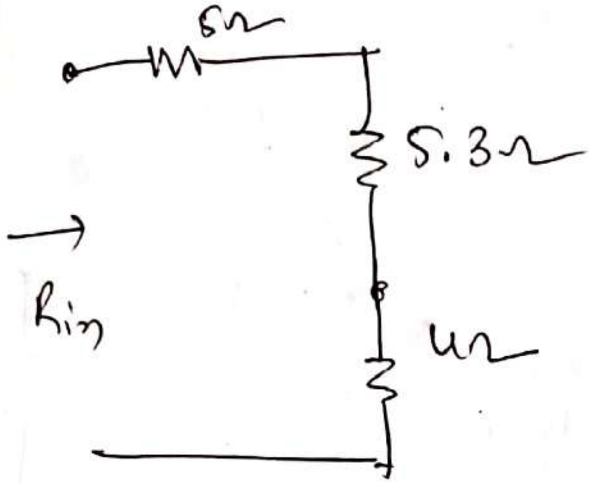
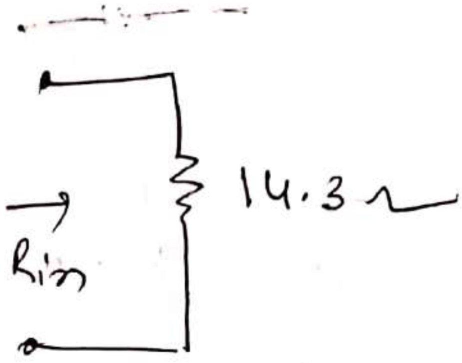
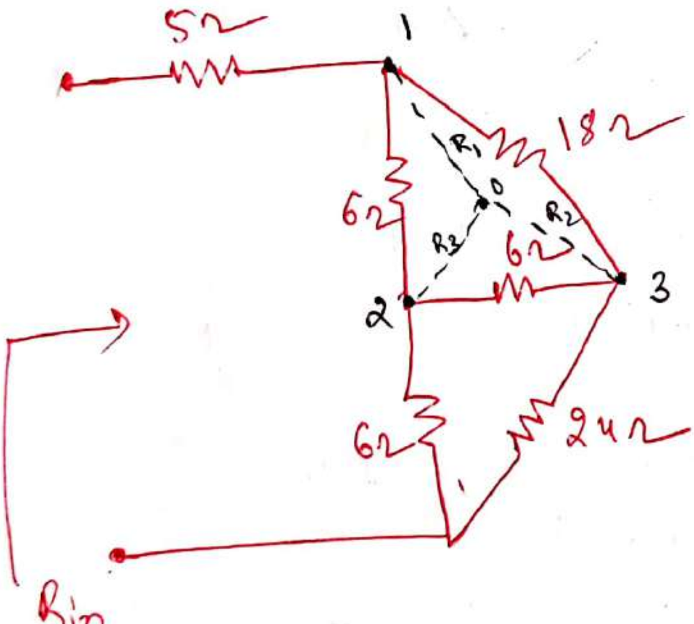
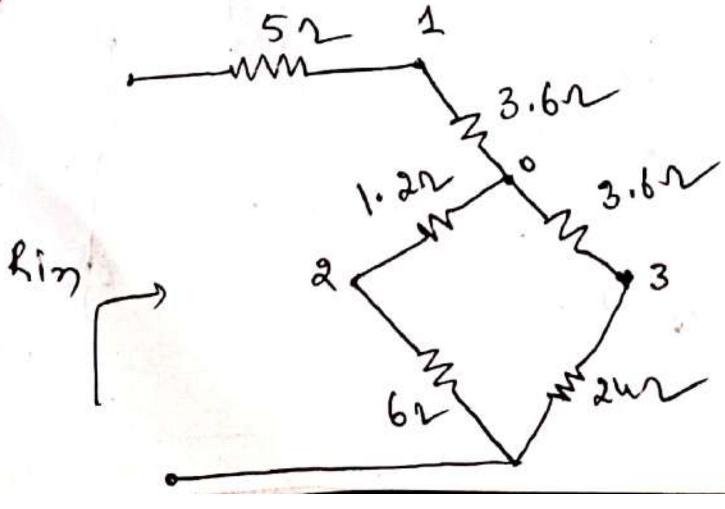




$$\boxed{R_{in} = 14.3\,\Omega}$$

(or)



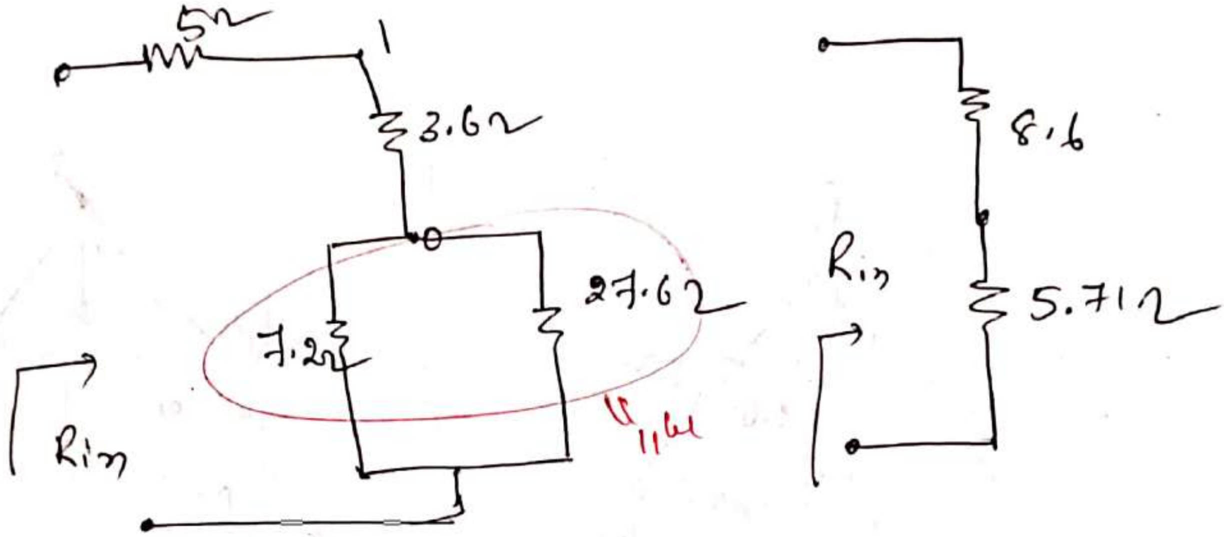


$$R_1 = \frac{6 \times 18}{6+18+6}$$

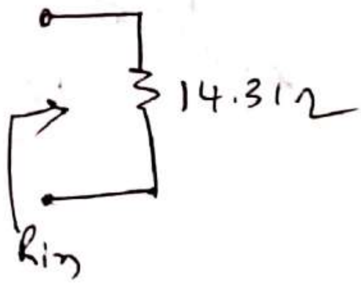
$$R_1 = 3.6\,\Omega$$

$$R_2 = \frac{18\times 6}{6+18+6} = 3.6\Omega$$

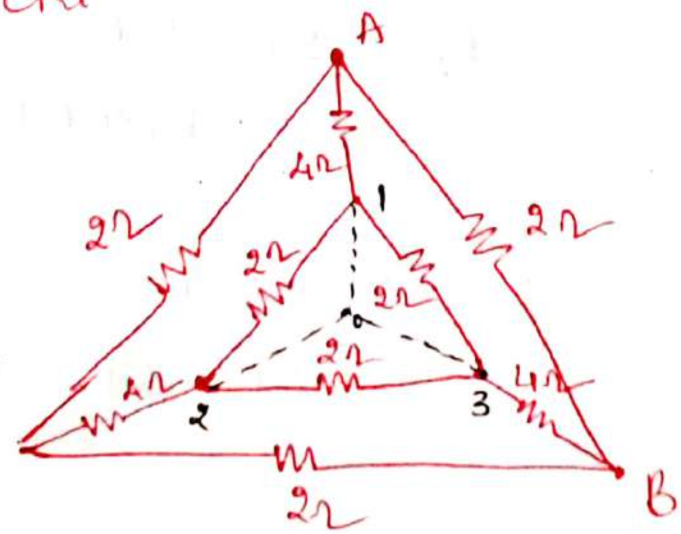
$$R_3 = \frac{6\times 6}{6+18+6} = 1.2\Omega$$



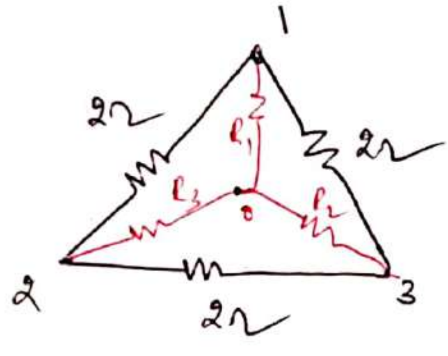
$$\boxed{R_{in} = 14.31\Omega}$$



2) Find the equivalent resistance b/n A & B for the ckt below.

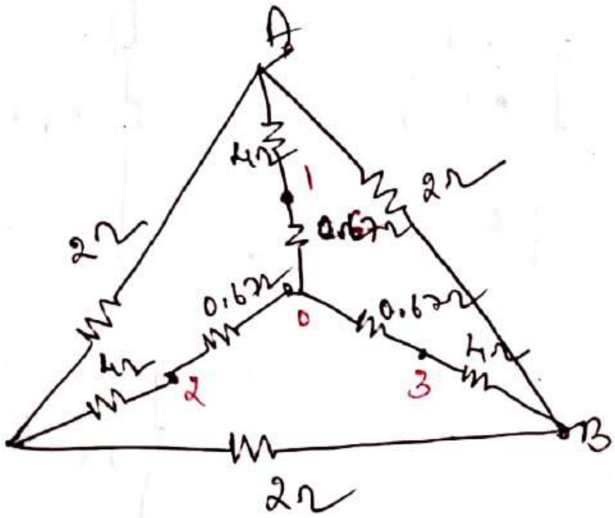


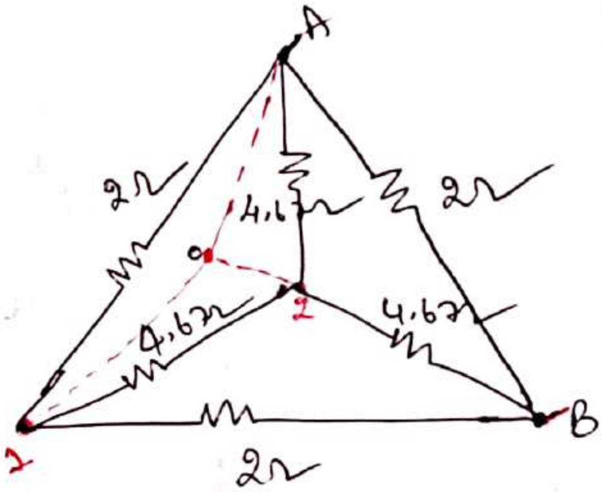
Inner delta into star

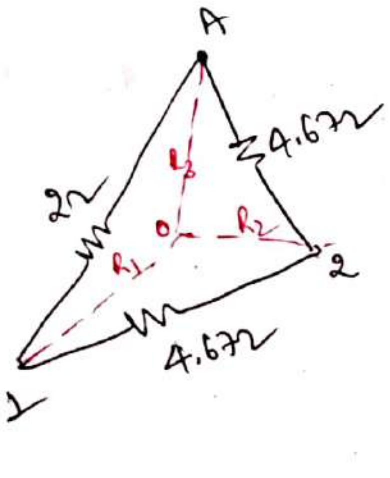


$$R_1 = \frac{2 \times 2}{2+2+2} = 0.67\Omega$$

||ly $R_2 = R_3 = 0.67\Omega$



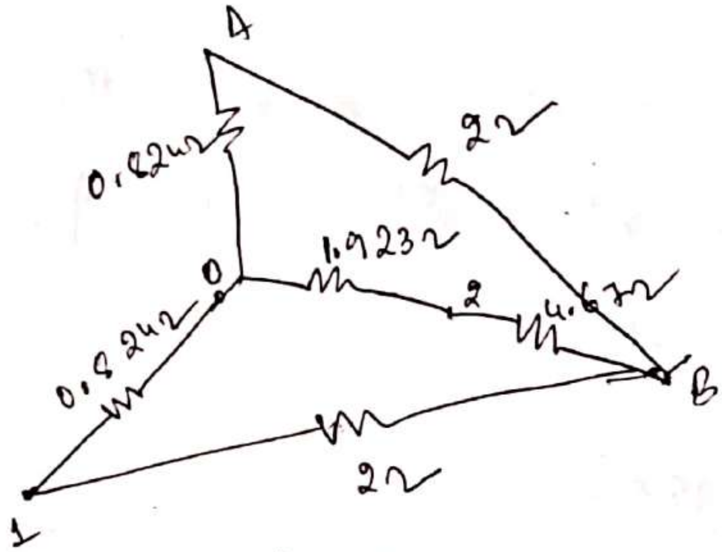


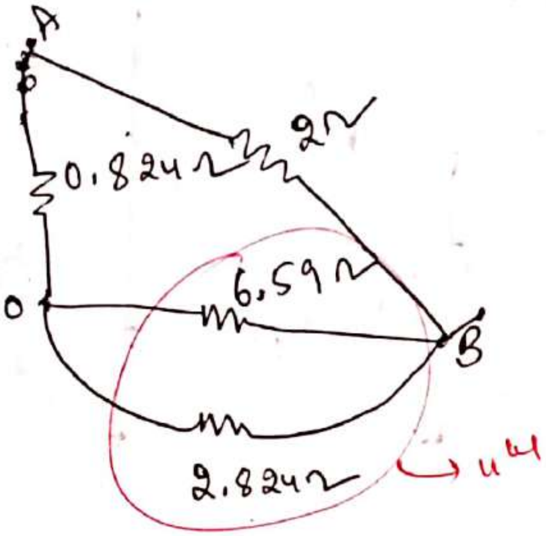


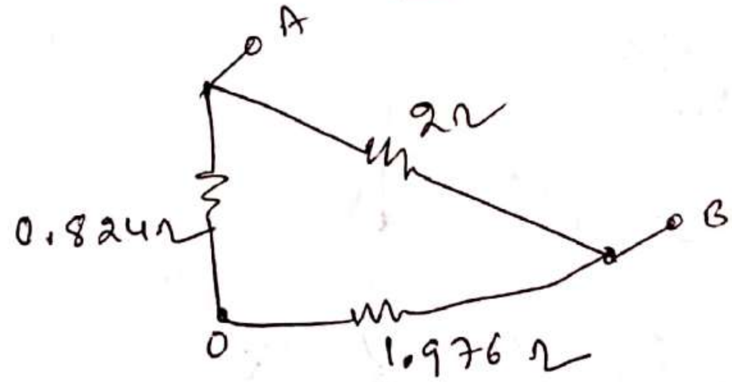
$$R_1 = \frac{2 \times 4.67}{2+4.67+4.67} = 0.824\Omega$$

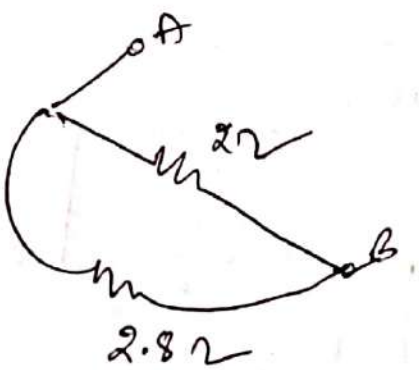
$$R_2 = \frac{4.67 \times 4.67}{2+4.67+4.67} = 1.923\Omega$$

$$R_3 = \frac{2 \times 4.67}{2+4.67+4.67} = 0.824\Omega$$



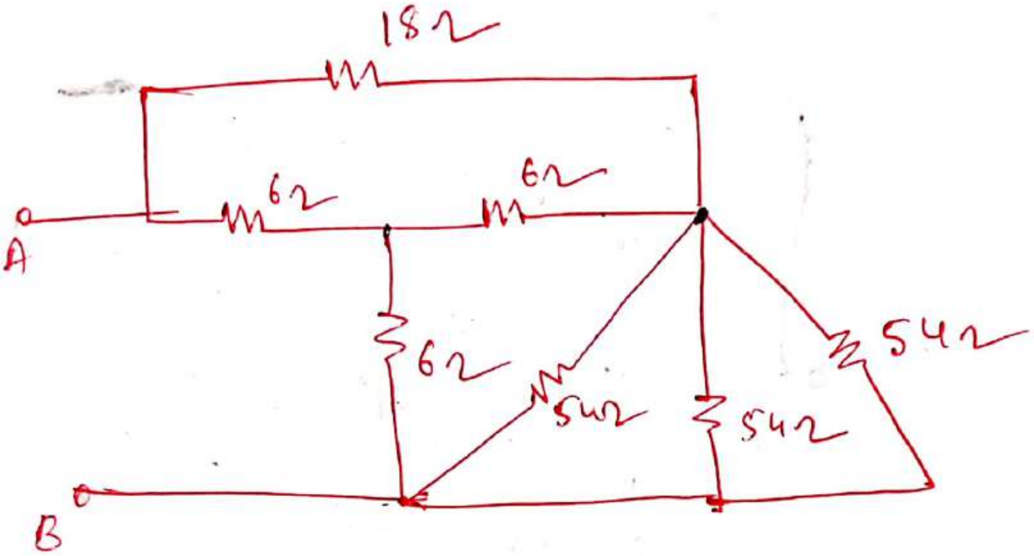


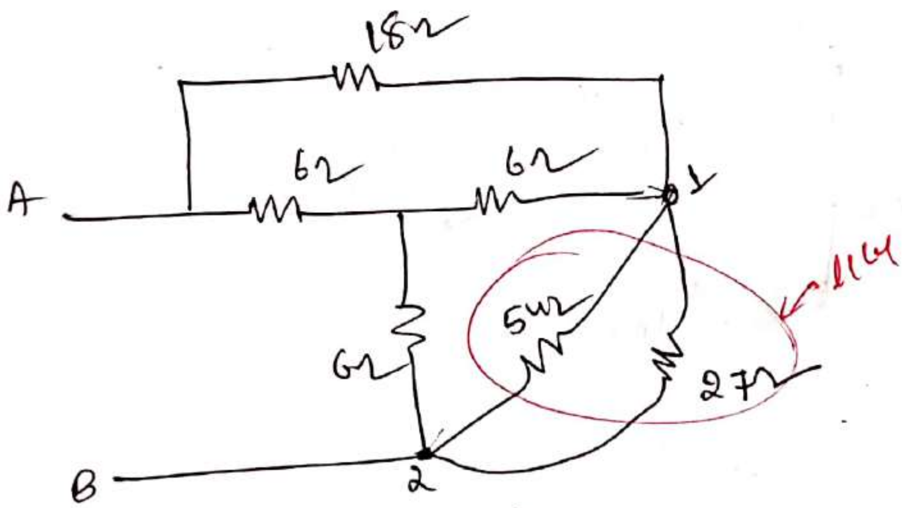


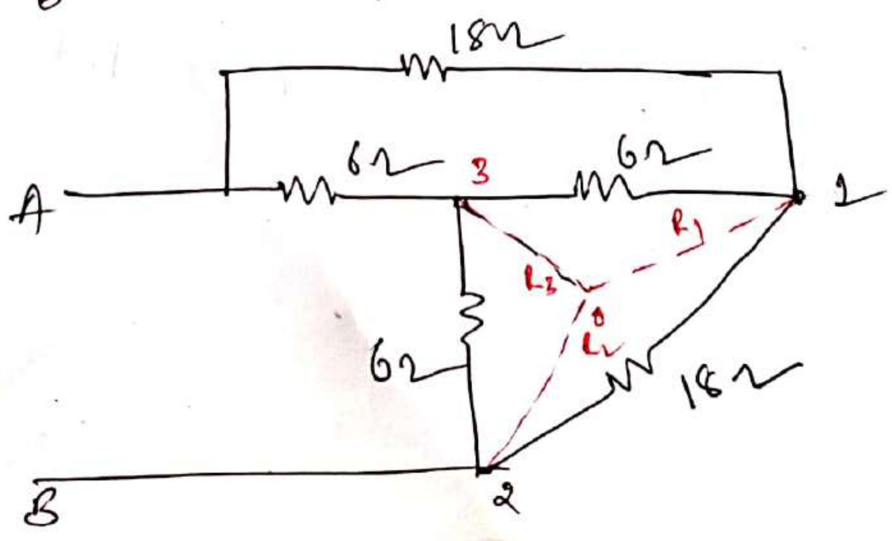


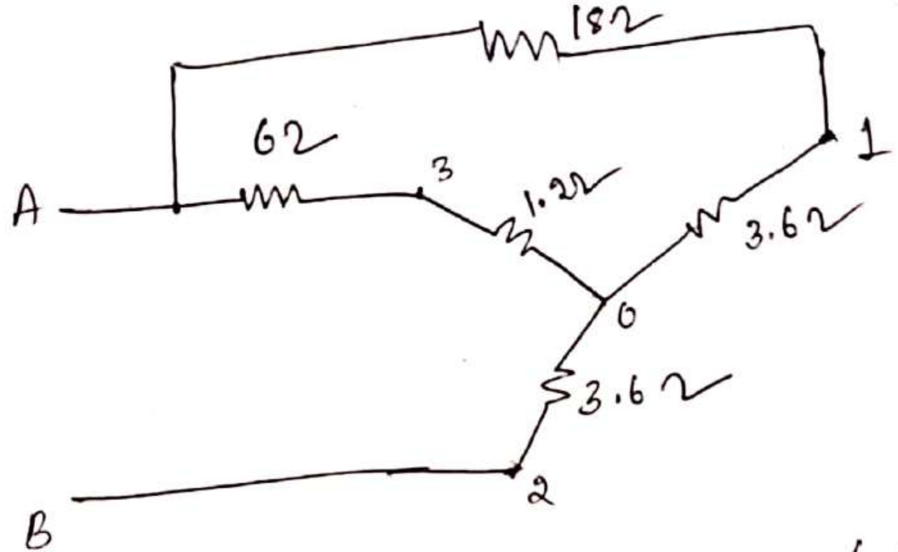
$$R_{AB} = 1.167\,\Omega$$

3) Compute the resistance across the terminals A & B of the n/w shown in fig using Δ-Y transformation





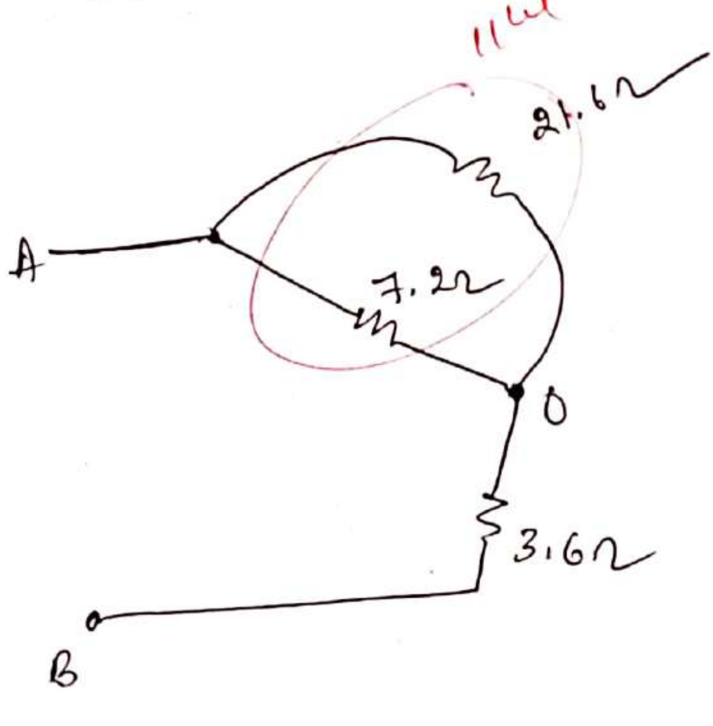


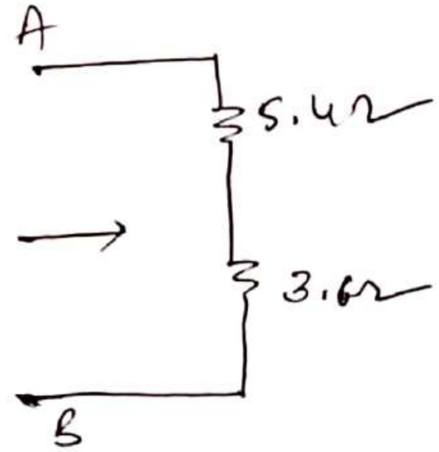


$$R_1 = \frac{6 \times 18}{6+18+6} = 3.6\Omega$$

$$R_2 = \frac{6 \times 18}{6+18+6} = 3.6\Omega$$

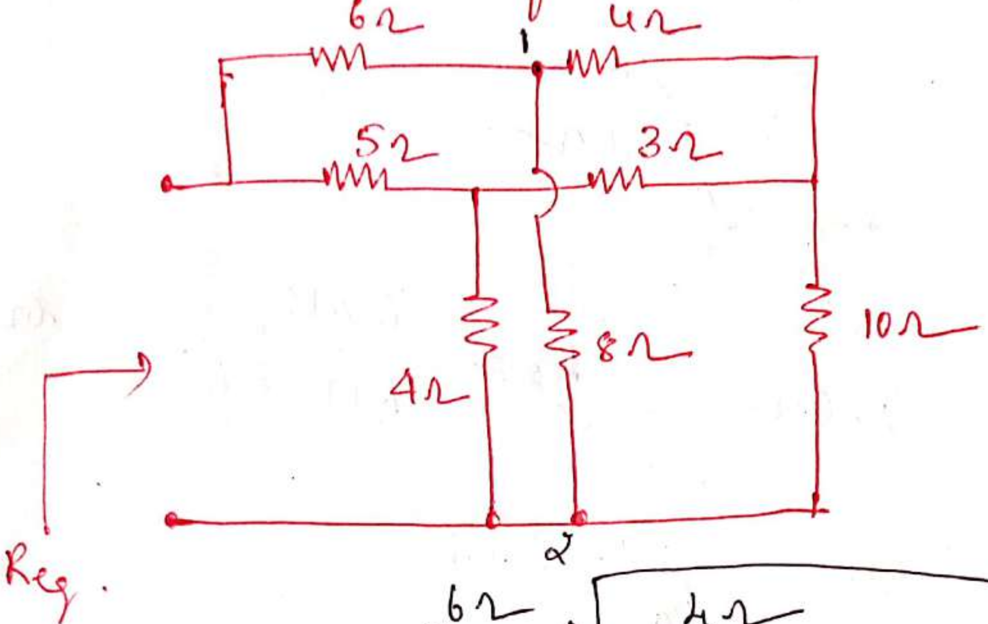
$$R_3 = \frac{6 \times 6}{6+18+6} = 1.2\Omega$$

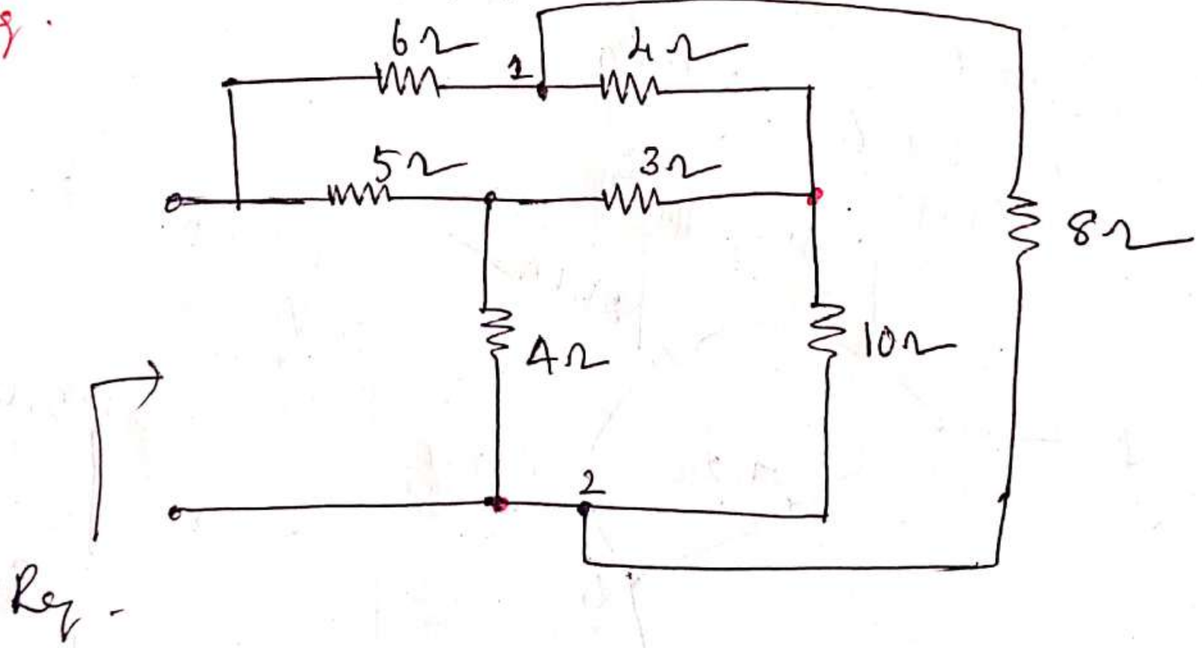


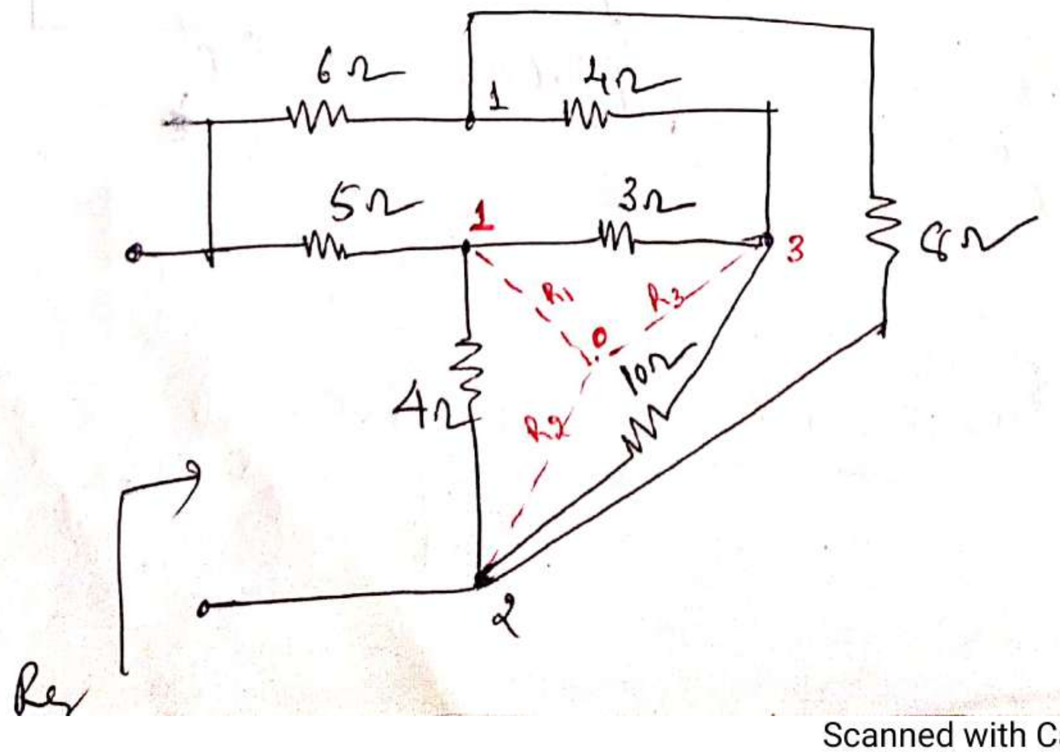


$$\boxed{R_{AB} = 9\Omega}$$

4) In the n/w shown below, find Req using Star delta transformation.



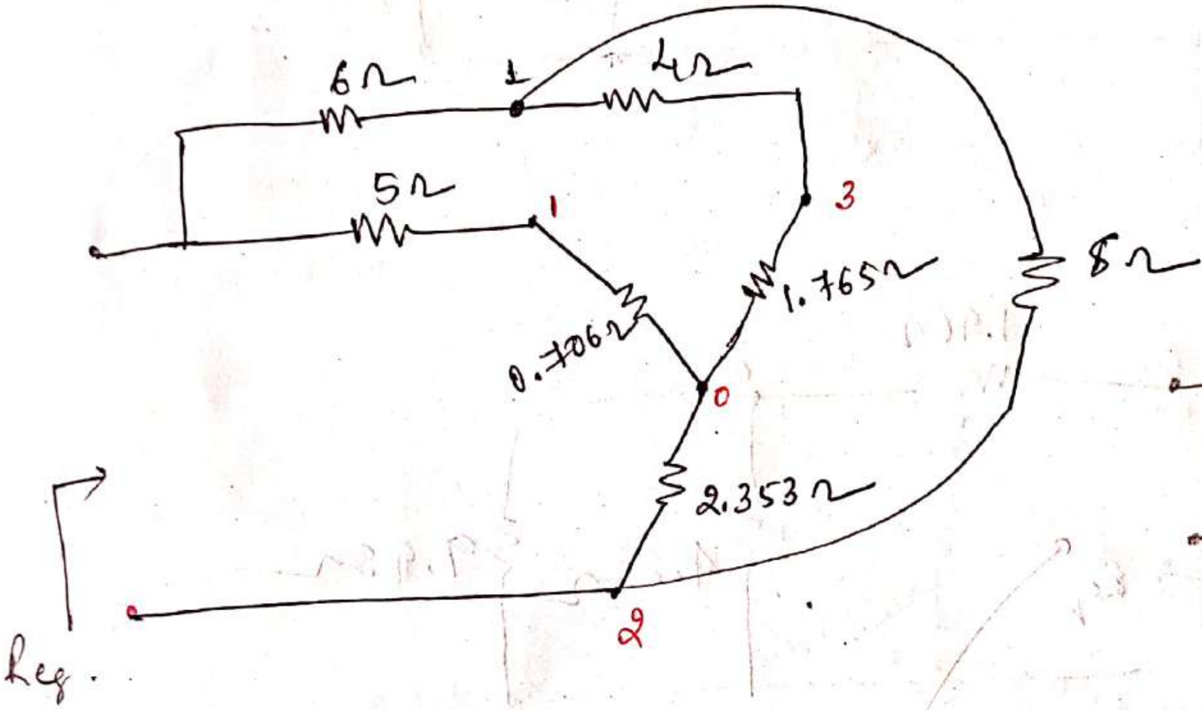


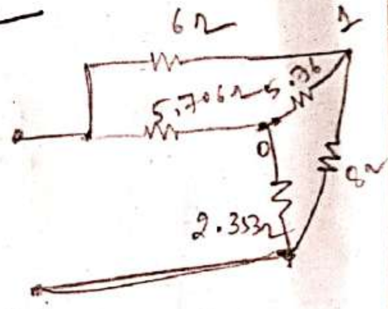


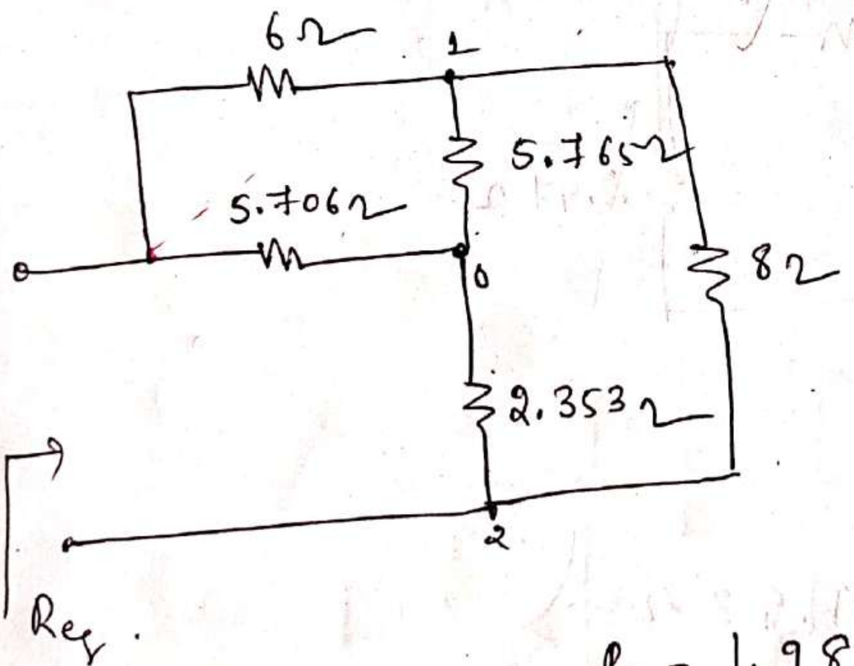
$$R_1 = \frac{4\times 3}{4+3+10} = 0.706\,\Omega \qquad R_2 = \frac{4\times 10}{4+10+3}$$

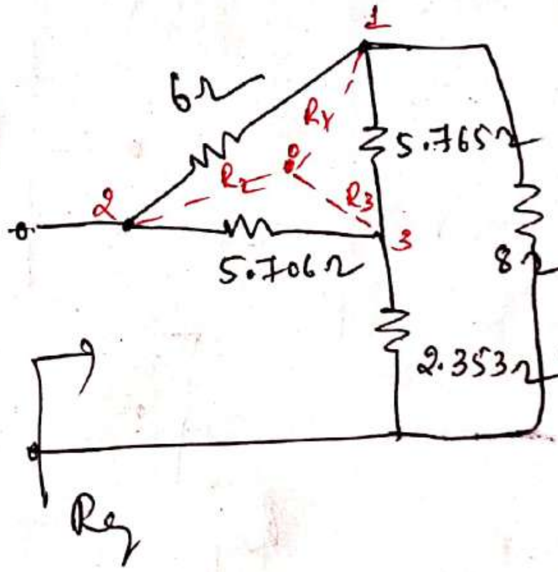
$$R_2 = 2.353$$

$$R_3 = \frac{3\times 10}{3+4+10} = 1.765\,\Omega$$



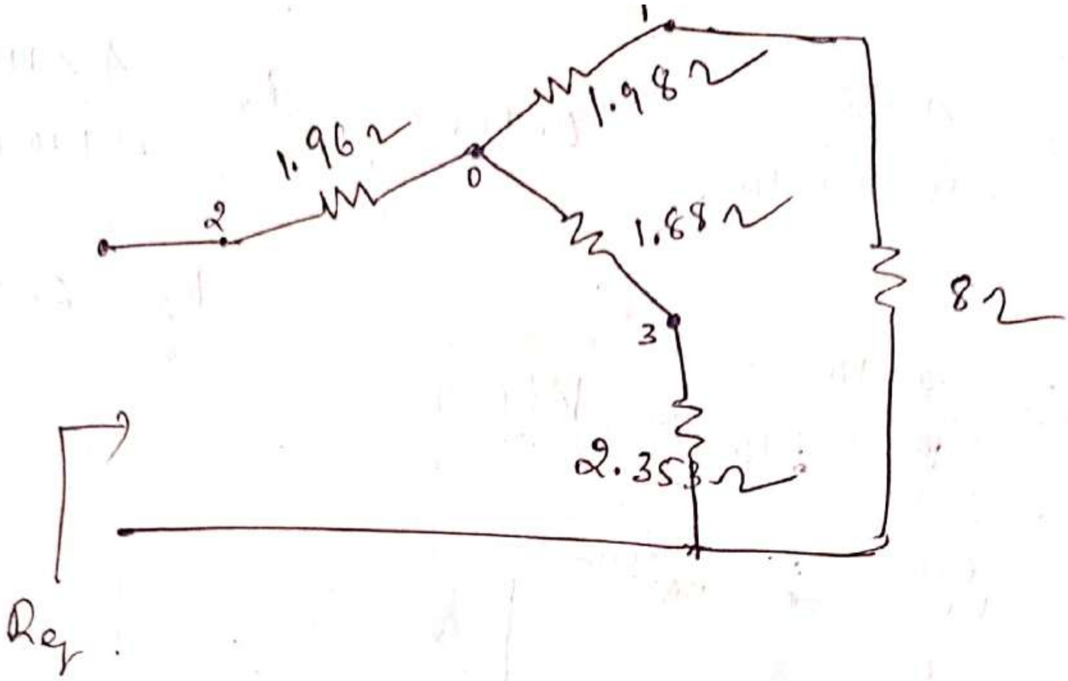


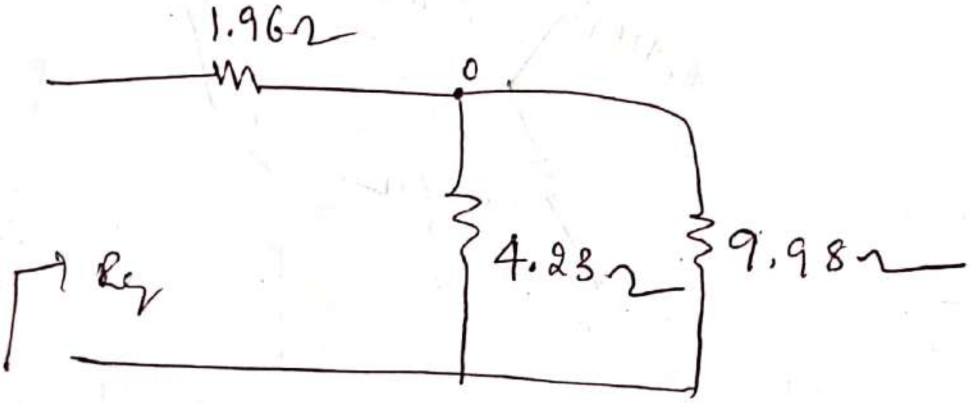


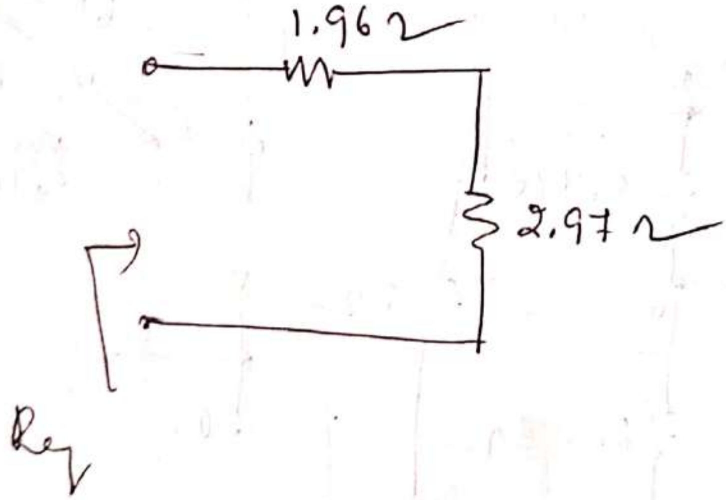


$$R_1 = 1.98\,\Omega \qquad R_3 = 1.88\,\Omega$$

$$R_2 = 1.96\,\Omega$$

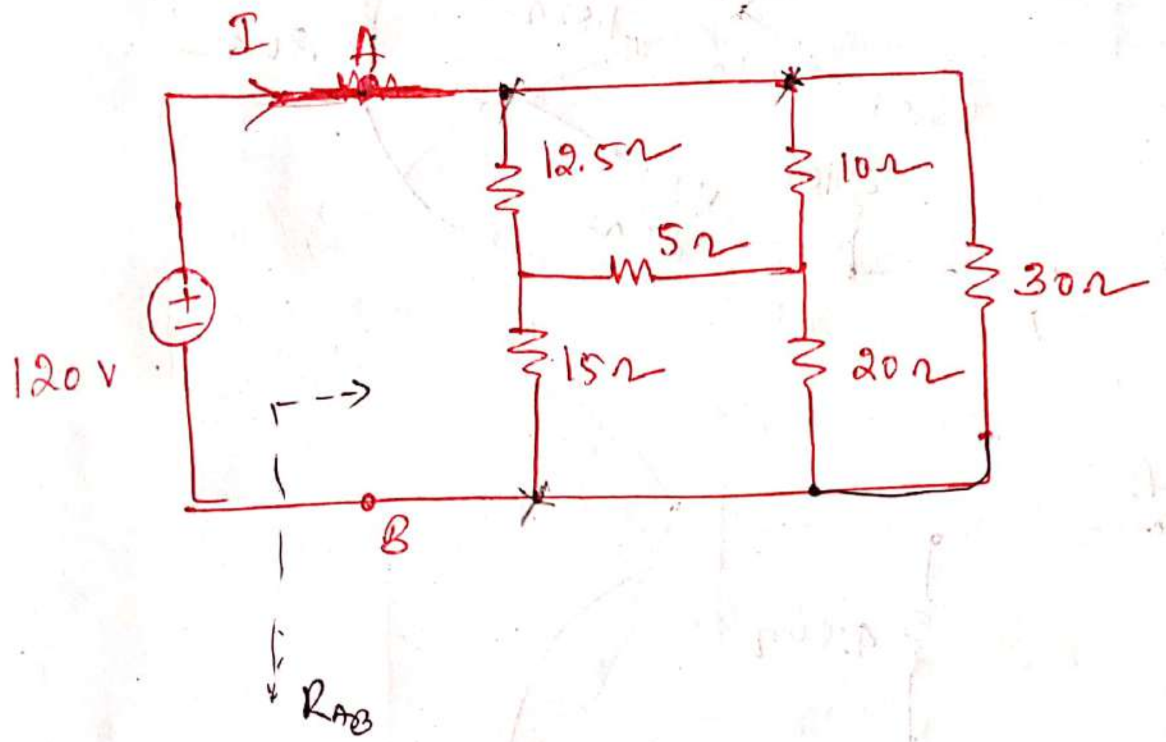


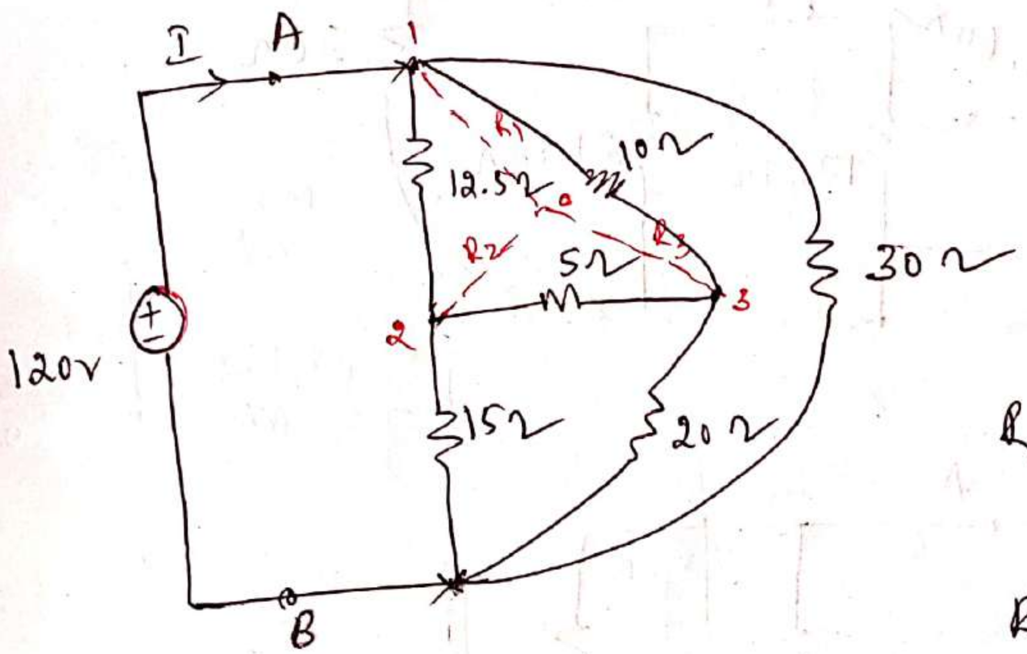




$R_{eq} = 4.93\,\Omega$

5) Obtain equivalent resistance R_{AB} for the given ckt & find I.





$$R_1 = \frac{12.5 \times 10}{12.5+10+5}$$

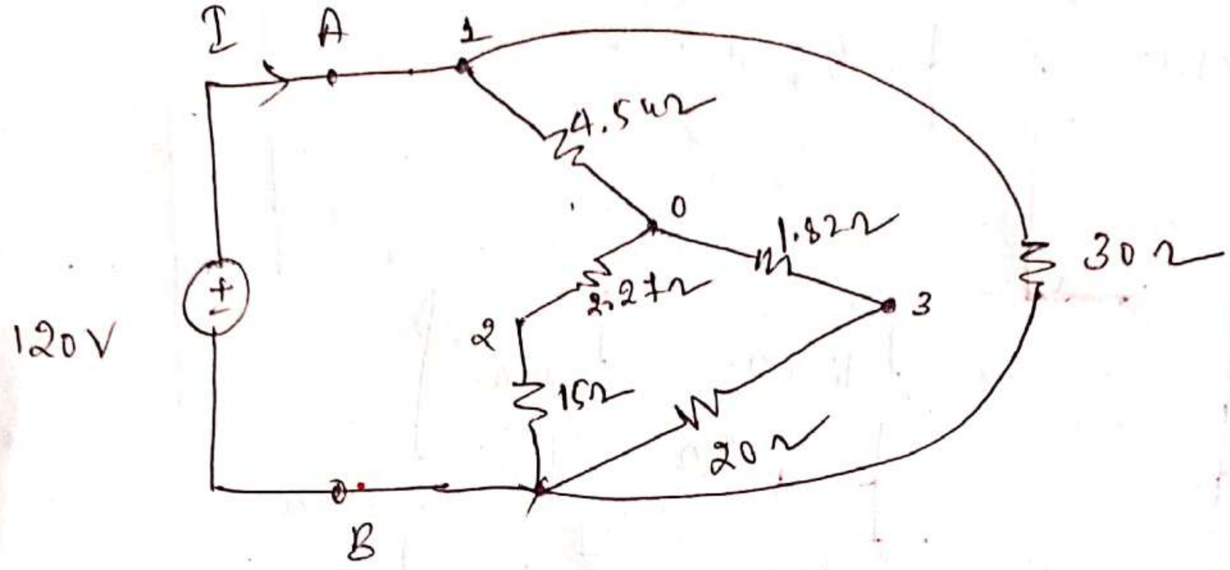
$$R_1 = 4.54\,\Omega$$

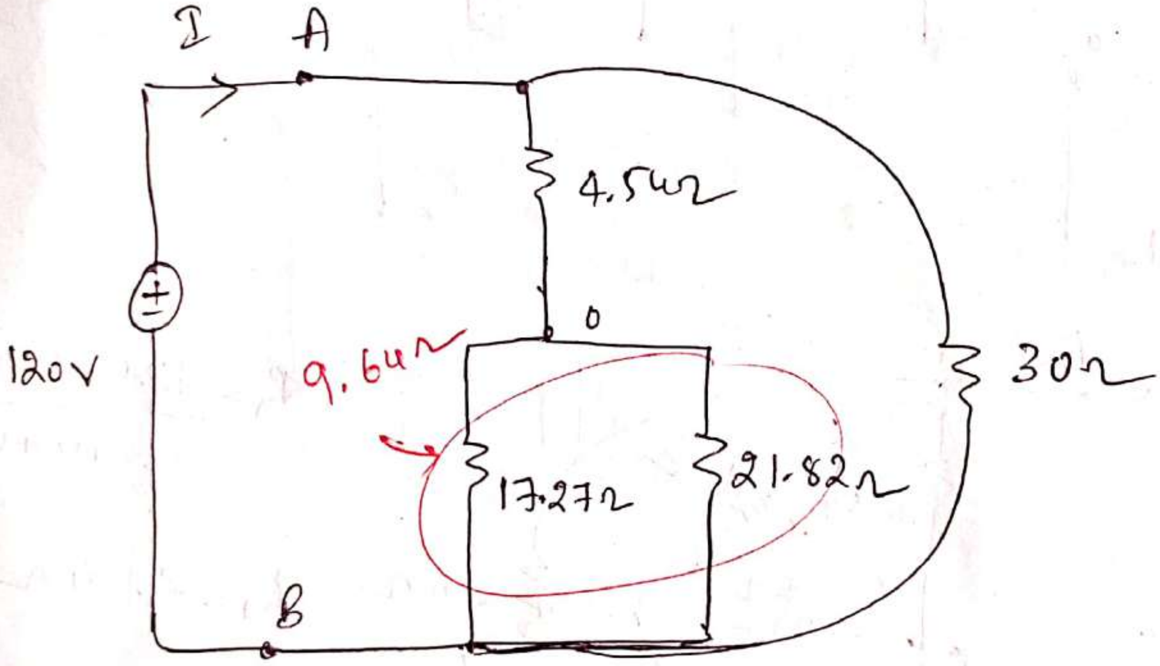
$$R_2 = \frac{12.5 \times 5}{12.5+10+5}$$

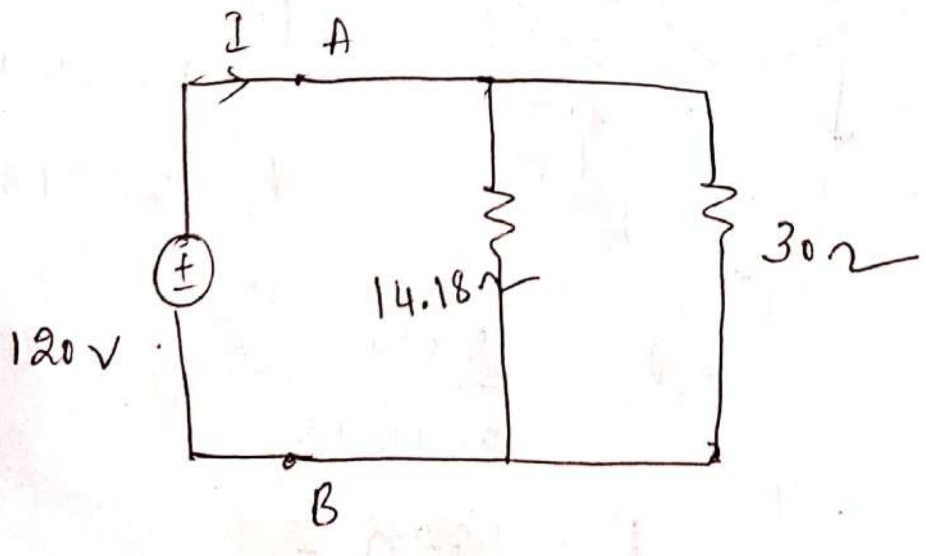
$$R_2 = 2.273\,\Omega$$

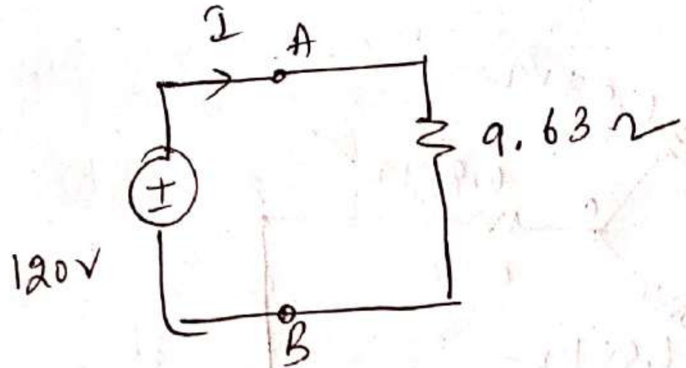
$$R_3 = \frac{5 \times 10}{12.5+10+5}$$

$$R_3 = 1.82\,\Omega$$


I
A
1
4.54Ω
0
1.82Ω
2.27Ω
3
30Ω
120V
2
15Ω
20Ω
B


I
A
4.54Ω
0
120V
9.64Ω
17.27Ω
21.82Ω
30Ω
B

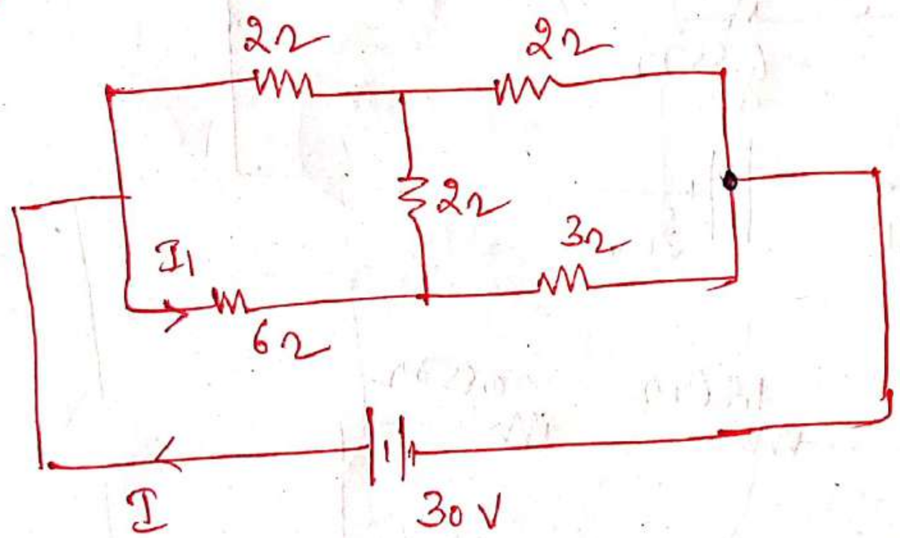

I
A
30Ω
14.18Ω
120V
B

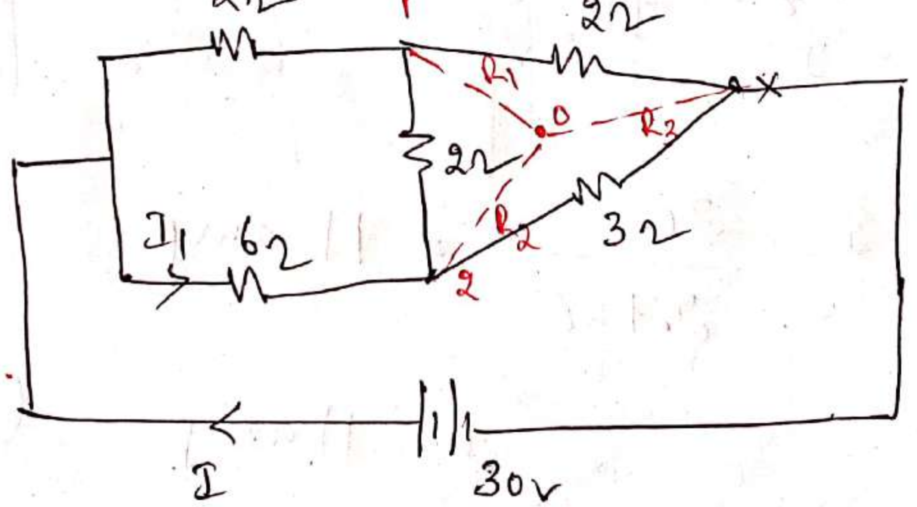


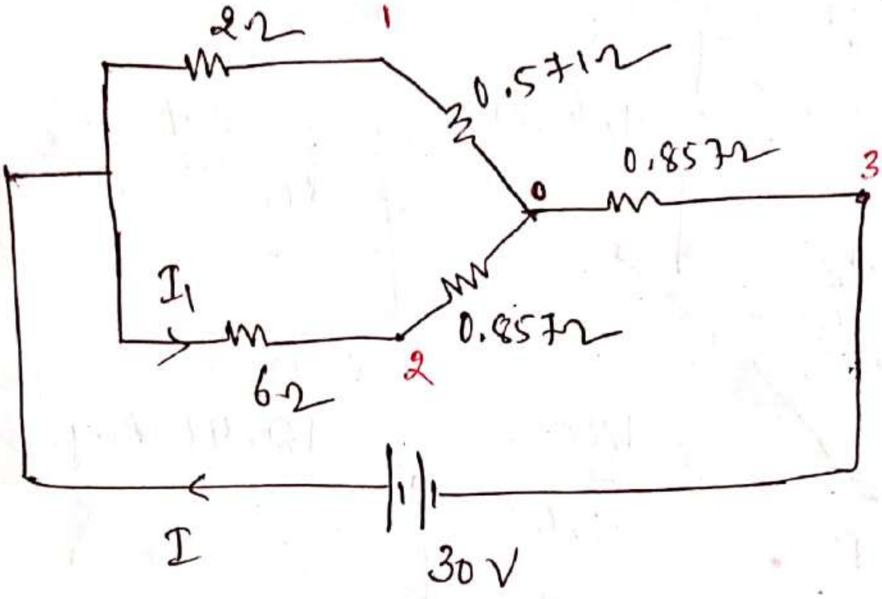
$R_{AB} = 9.63\,\Omega$

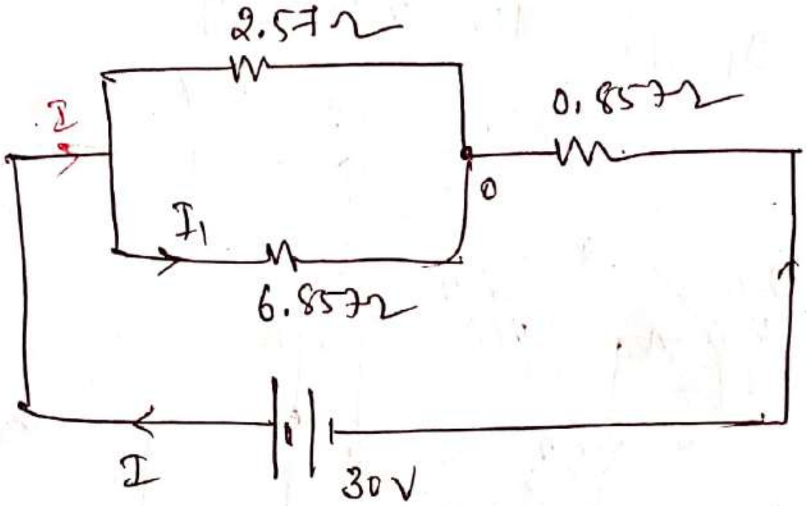
$$I = \frac{V}{R} = \frac{120}{9.63} = 12.46 \text{ Amp.}$$

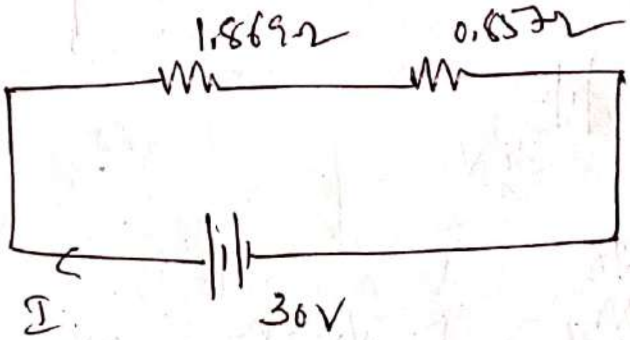
6) Find I & I_1 in the n/w shown using Δ-Y transformation.











$$I = \frac{30}{2.726} = 11 \text{ amp}$$

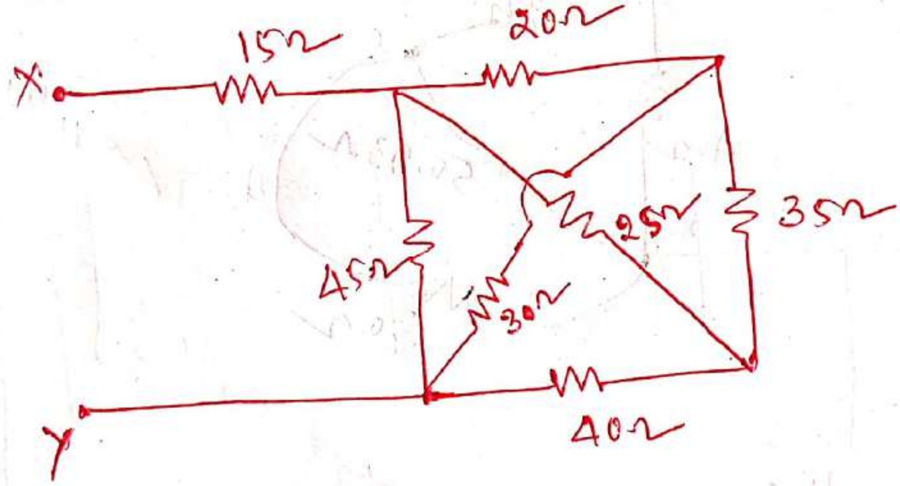
$$\boxed{I = 11 \text{ amp}}$$

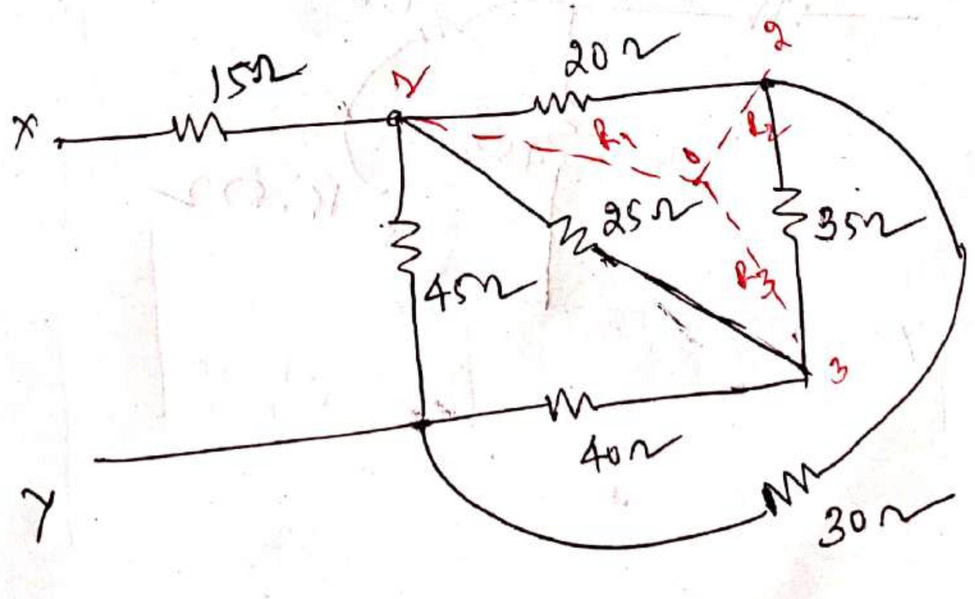
$$I_1 = \frac{I \times 2.57\Omega}{2.57 + 6.857\Omega}$$

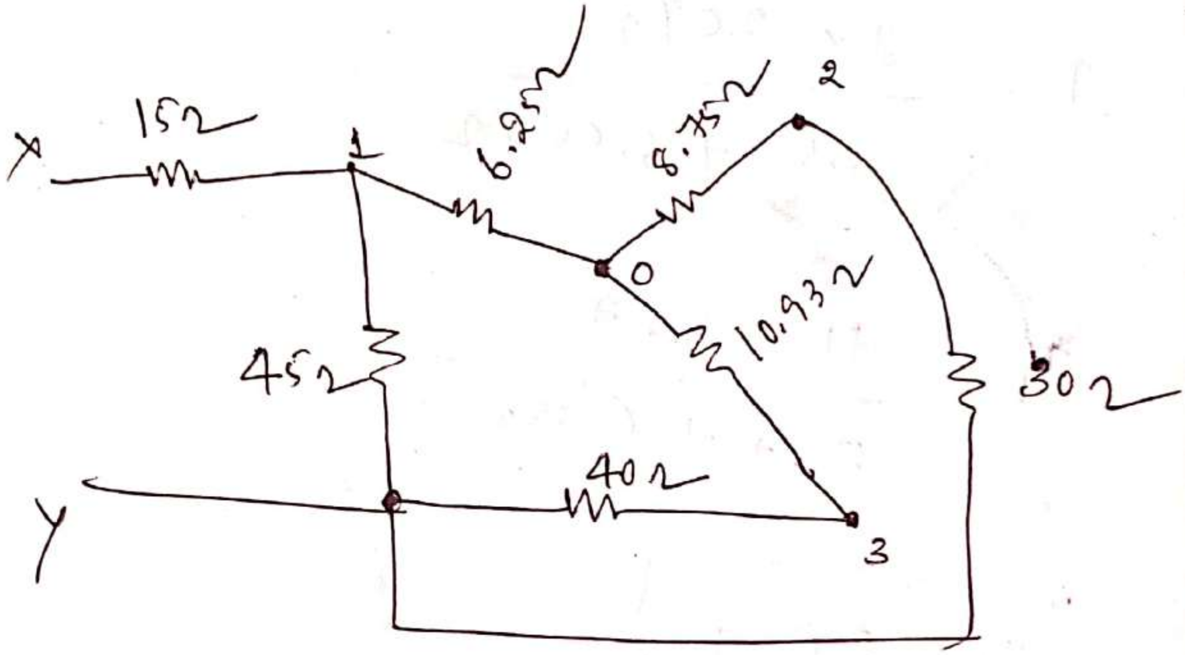
$$I_1 = \frac{11 \times 2.57}{2.57 + 6.857}$$

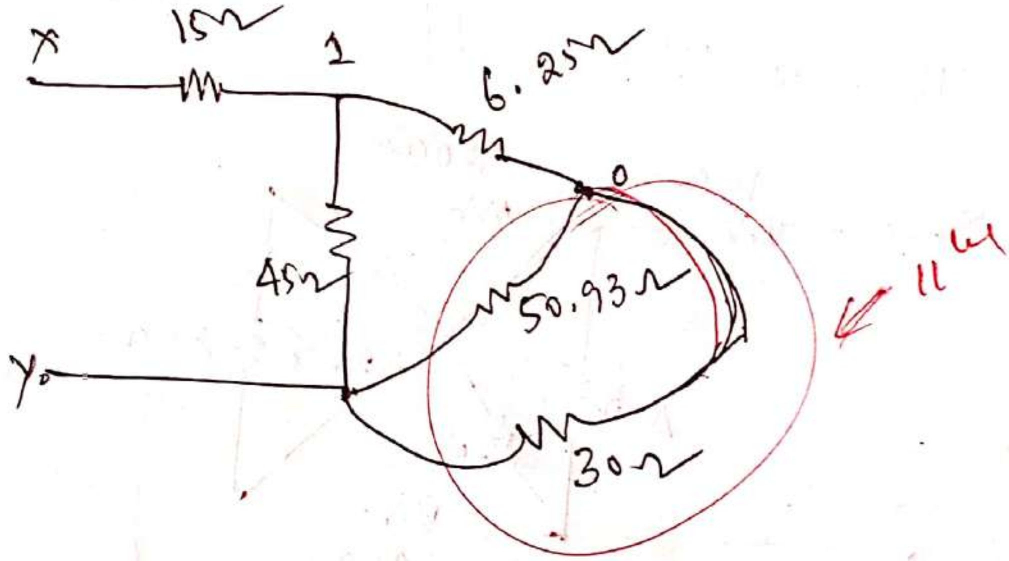
$$\boxed{I_1 = 3\ \text{Amp}}$$

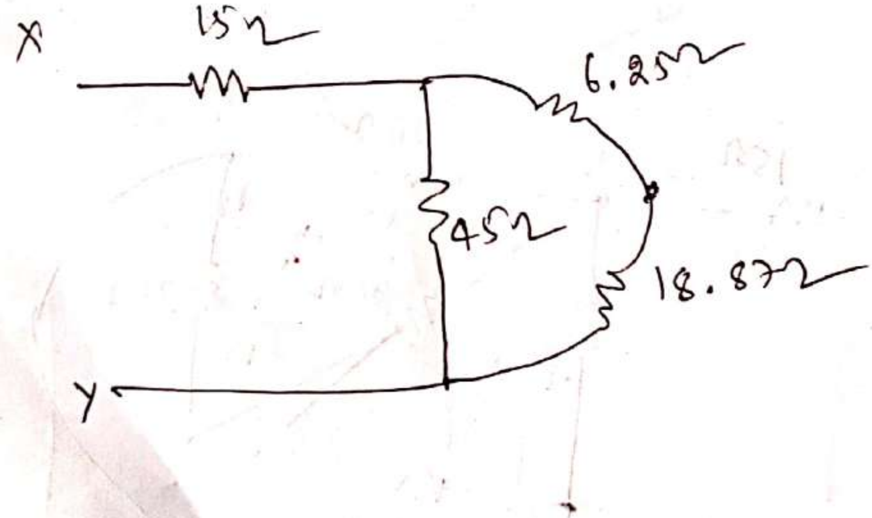
7) Find the resistance b/n the terminals X & Y











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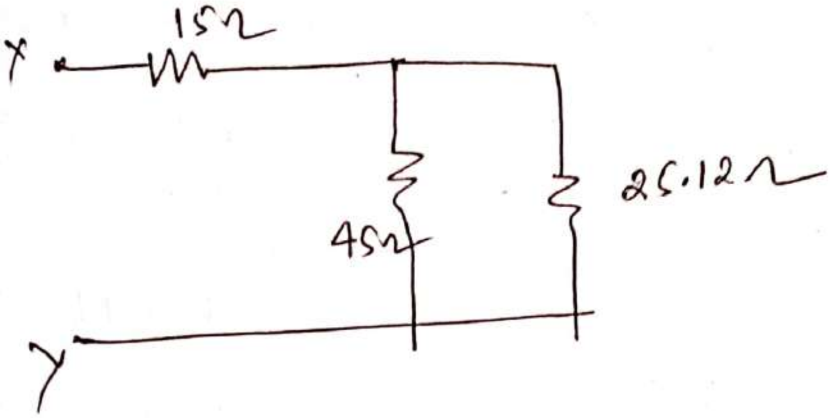
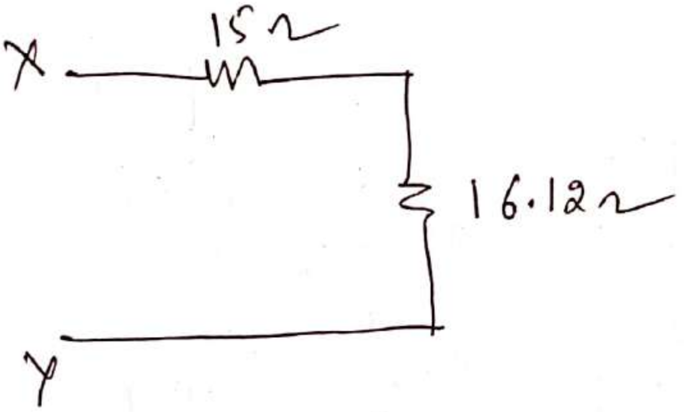
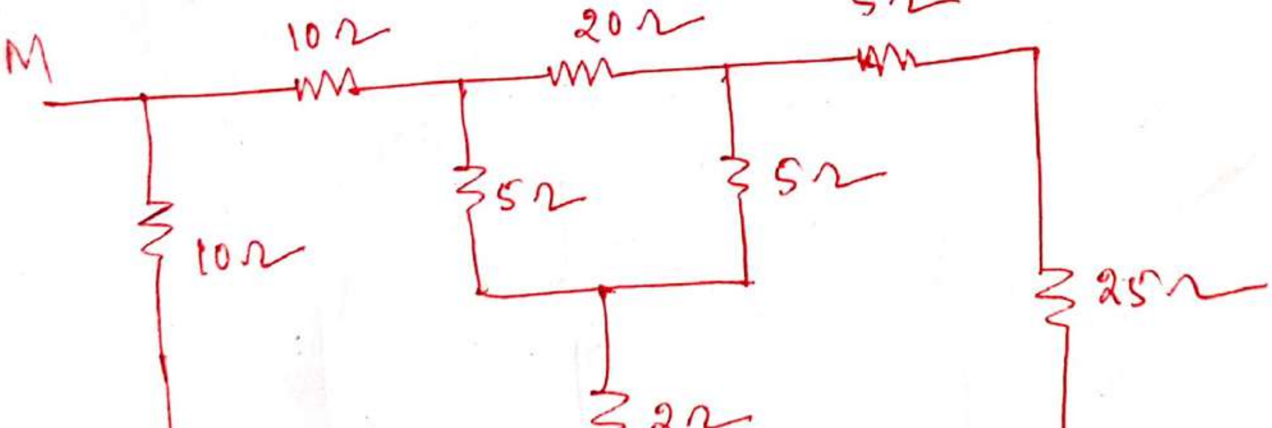




$$\boxed{R_{XY} = 31.12\ \Omega}$$

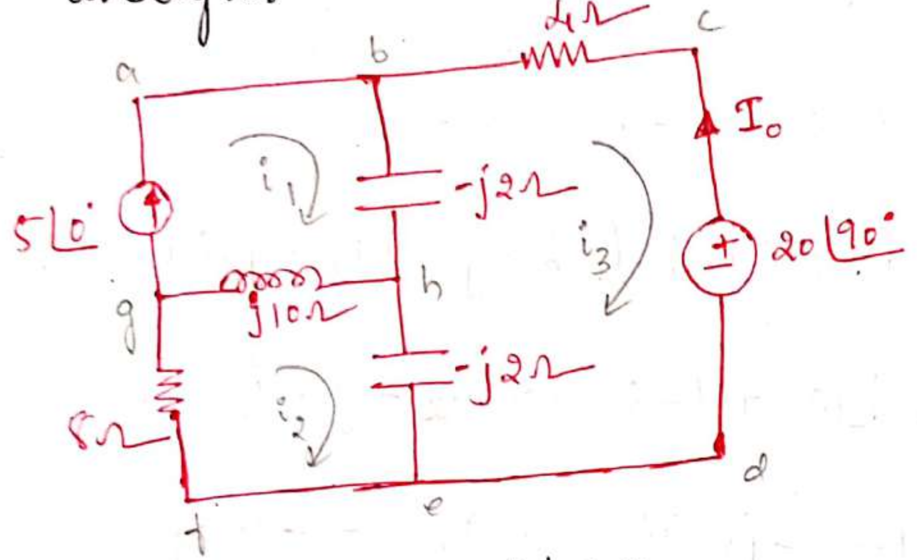
9)



$$\boxed{R_{MN} = 22.84\ \Omega}$$

Mesh Analysis :- (Loop or Current Analysis)

1) Determine the current I_0 in the circuit using mesh analysis.



$j = 1\angle 90^\circ$

$-j = 1\angle -90^\circ$

$j2 = 2\angle 90^\circ$

From the mesh abhga

$$i_1 = 5\angle 0^\circ \quad \text{——— (1)}$$

→ KVL to the mesh bcdehb

$$-4i_3 - 20\angle 90^\circ + j2(i_3 - i_2) + j2(i_3 - i_1) = 0$$

$$-4i_3 - 20\angle 90^\circ + j2i_3 - j2i_2 + j2i_3 - j2i_1 = 0.$$

$$-j2i_2 + (-4 + j4i_3) - 20\angle 90^\circ - j2(5\angle 0^\circ) = 0$$

$$-j2i_2 + (-4 + j4i_3) - 20\angle 90^\circ - 10\angle 90^\circ = 0$$

$$-j2i_2 + (-4 + j4i_3) = 30\angle 90^\circ \quad \text{——— (2)}$$

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→ KVL to ghefg

$$-j10(i_2 - i_1) + j2(i_2 - i_3) - 8i_2 = 0$$

$$-j10\,i_2 + j10\,i_1 + j2\,i_2 - j2\,i_3 - 8\,i_2 = 0$$

$$j10\,i_1 + (-8 - j8)\,i_2 - j2\,i_3 = 0$$

$$j10(5\angle 0^\circ) + (-8 - j8)\,i_2 - j2\,i_3 = 0$$

$$50\angle 90 + (-8 - j8)\,i_2 - j2\,i_3 = 0$$

50j

$$(-8 - j8)\,i_2 - j2\,i_3 = -50j$$

$$(-8 - j8)\,i_2 - j2\,i_3 = 50\angle -90^\circ \quad \text{——— (3)}$$

matrix form

$$\begin{bmatrix} -j2 & -4+j4 \\ -8-j8 & -j2 \end{bmatrix} \begin{bmatrix} I_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 30\angle 90^\circ \\ 50\angle -90^\circ \end{bmatrix}$$

$$\Delta = \begin{vmatrix} -j2 & -4+j4 \\ -8-j8 & -j2 \end{vmatrix}$$

$$\Delta = -4 - (-8 - j8)(-4 + j4)$$

$$\Delta = -4 - (+32 + \cancel{32}j - \cancel{32}j + 32)$$

$$\Delta = -4 - 64 = -68$$

$$\Delta = -68$$

$$\Delta_2 = \begin{vmatrix} -j2 & 30j \\ -8-j8 & -50j \end{vmatrix}$$

$$\Delta_2 = -100 - [(-8-j8)(30j)]$$

$$\Delta_2 = -100 - [-240j + 240]$$

$$\Delta_2 = -340 + j240$$

$I_0 = 6.12 \angle 144.79° A$

$$I_3 = \frac{\Delta_2}{\Delta} = \frac{-340 + j240}{-68}$$

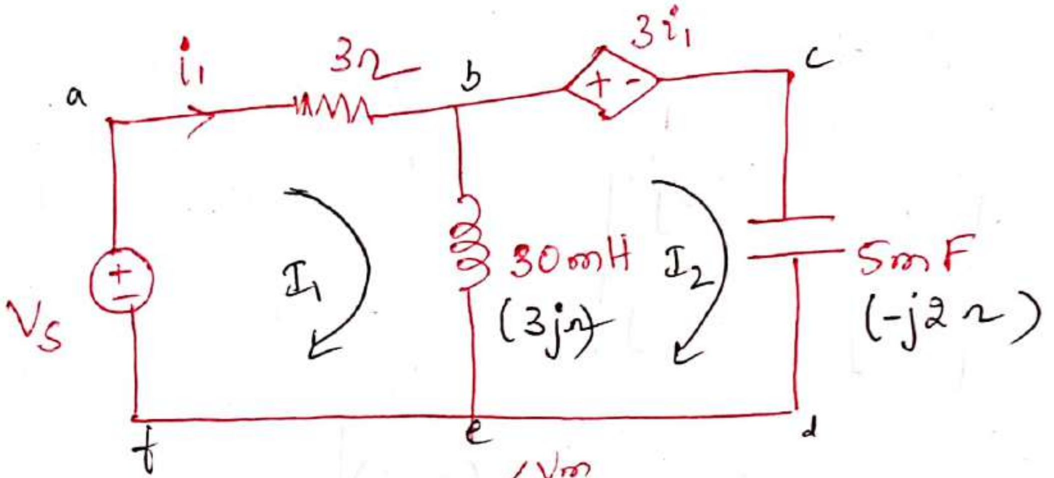
$$I_3 = 5 - j3.53$$

$$I_3 = 6.12 \angle -35.21 \text{ Amp}$$

From the fig

$$I_0 = -I_3 = -6.12 \angle -35.21° \text{ Amp}.$$

2) Find the Steady State Sinusoidal Current i_1 for the Circuit when $V_S = 10\sqrt{2}\cos(100t + 45°)$



$$\text{Given} \quad V_s = \underbrace{10\sqrt{2}}_{V_m} \cos(\underbrace{100t}_{\omega t} + 45°)$$

$$V_S = \frac{V_m}{\sqrt{2}} \angle 45°$$

$$= \frac{10\cancel{\sqrt{2}}}{\cancel{\sqrt{2}}} \angle 45° = 10 \angle 45° \text{ volts}$$

$\omega t = 100t$

$\omega = 100$

$X_L = 2\pi f L$

$= \omega L$

$= 100 \times 30\,mH$

$= 3\Omega$ $\boxed{X_L = j3\Omega}$

$X_C = \dfrac{1}{2\pi f C}$

$= \dfrac{1}{\omega C}$

$X_C = \dfrac{1}{100 \times 5 \times 10^{-3}}$

$\boxed{X_C = -j2\Omega}$

From the figure

$$\boxed{i_1 = I_1}$$

→ KVL to mesh abefa

$$-3I_1 - j3(I_1 - I_2) + 10\angle 45 = 0$$

$$-3I_1 - 3jI_1 + 3jI_2 = -10\angle 45^\circ$$

$$(-3-3j)I_1 + 3jI_2 = -10\angle 45^\circ] \quad \text{——} \quad (1)$$

→ KVL to mesh bcdeb.

$$-3(i_1) + 2jI_2 - 3j(I_2 - I_1) = 0$$

$$-3I_1 + 2jI_2 - 3jI_2 + 3jI_1 = 0$$

$$(-3+3j)I_1 - jI_2 = 0 \quad \text{——} \quad (2)$$

WKT,

$$\begin{bmatrix} -3-3j & 3j \\ -3+3j & -j \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} -10\angle 45^\circ \\ 0 \end{bmatrix}$$

$$\Delta = \begin{vmatrix} -3-3j & 3j \\ -3+3j & -j \end{vmatrix}$$

$$= 3j - 3 - (3j)(-3+3j)$$

$$= 3j - 3 + 9j + 9 = 6 + j12$$

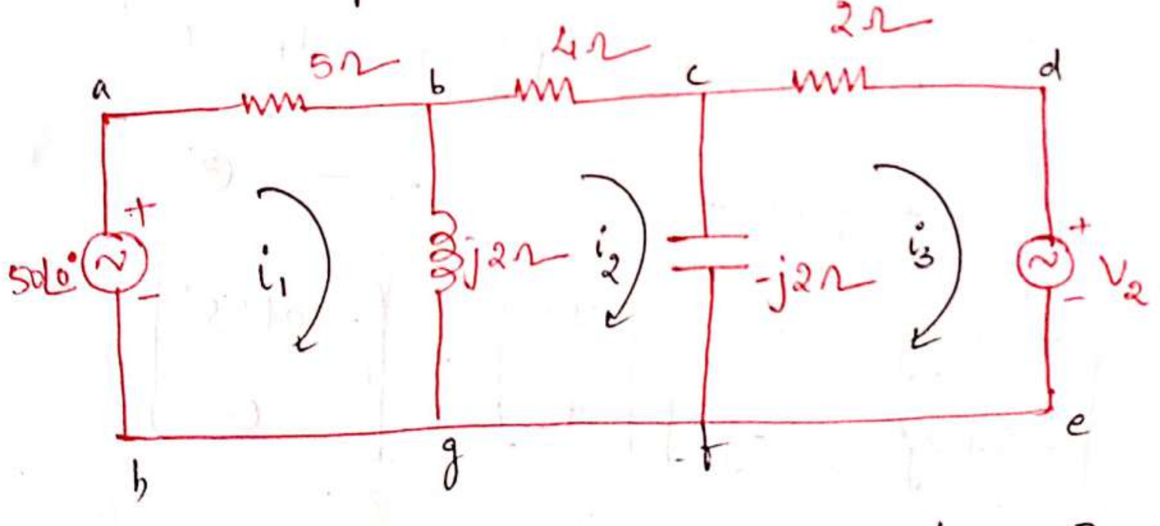
$$\Delta_1 = \begin{vmatrix} -10\angle 45 & 3j \\ 0 & 1\angle -90 \end{vmatrix}$$

$$\Delta_1 = -10\angle -45^\circ$$

$$\therefore\ I_1 = \frac{\Delta_1}{\Delta} = \frac{-10\angle -45^\circ}{6+12j} = 0.745\angle 71.57^\circ$$

Imp July-6
July-07

3) In the circuit shown determine V_2 which results
*4 in '0' (zero) current through 4Ω resistor
use mesh analysis



Given, current through 4Ω is zero

$$\boxed{i_2 = 0}$$

→ KVL to the mesh abgha

$$-5i_1 - j2(i_1 - i_2) + 50\angle 0^\circ = 0$$

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$$-5i_1 - j2i_1 = -50\angle 0^\circ$$

$$\cancel{-}(5+j2)i_1 = \cancel{-}50\angle 0^\circ$$

$$i_1 = \frac{50\angle 0^\circ}{5+j2} = 9.28\angle -21.81^\circ \text{ amp}$$

→ KVL to mesh bcfgb

$$-4i_2 + j2(i_2 - i_3) - j2(i_2 - i_1) = 0$$

$$-\cancel{4}i_2 - j2i_3 + j2i_1 = 0$$

$$j2i_1 = j2i_3$$

$$i_3 = i_1 = 9.28\angle -21.81^\circ \text{ amp}$$

→ KVL to mesh cdefc.

$$-2i_3 - V_2 + j2(i_3 - i_2) = 0$$

$$-2i_3 - V_2 + j2i_3 = 0$$

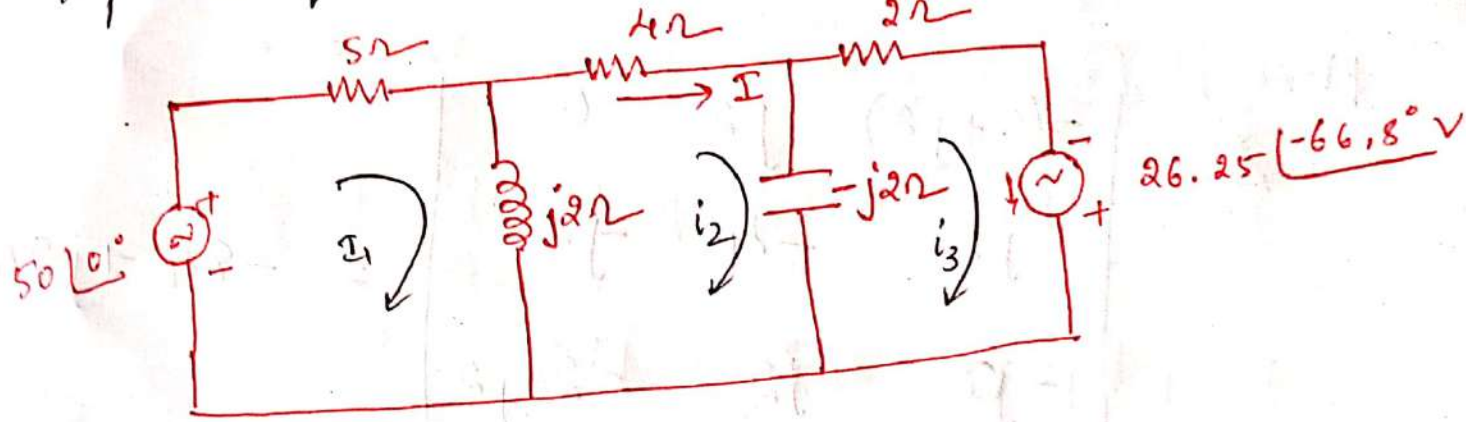
$$V_2 = (-2+j2)i_3$$

$$V_2 = 2.82\angle 135^\circ \times 9.28\angle -21.81^\circ$$

$$V_2 = 26.16\angle 113.19^\circ \text{ volts}$$

mesh analysis

4) In the Circuit shown below, find I through loop analysis.



→ KVL to Loop 1

$$-5i_1 - j2(i_1 - i_2) + 50\angle 0° = 0$$

$$-5i_1 - j2i_1 + j2i_2 = -50\angle 0°$$

$$(-5-j2)i_1 + j2i_2 = -50\angle 0° \quad \text{——} \; (1)$$

→ KVL to loop 2

$$-4i_2 + j2(i_2 - i_3) - j2(i_2 - i_1) = 0$$

$$-4i_2 + \cancel{j2i_2} - j2i_3 - \cancel{j2i_2} + j2i_1 = 0$$

$$+j2i_1 - 4i_2 - j2i_3 = 0 \quad \text{——} \; (2)$$

→ KVL to loop 3.

$$-2i_3 + 26.25\angle -66.8° + j2(i_3 - i_2) = 0$$

$$-2i_3 + 26.25\angle -66.8° + j2i_3 - j2i_2 = 0$$

$-j2i_2 + (-2+j2)\, i_3 = -26.25 \angle -66.8^\circ$ ——— (3)

Here

$$\Delta = \begin{vmatrix} -5-j2 & j2 & 0 \\ j2 & -4 & -j2 \\ 0 & -j2 & -2+j2 \end{vmatrix} = -84 + j24$$

From the figure $I = I_2 = \dfrac{\Delta_2}{\Delta}$

$$\therefore \quad \Delta_2 = \begin{vmatrix} -5-j2 & -50\angle 0^\circ & 0 \\ j2 & 0 & -j2 \\ 0 & -26.25\angle -66.8^\circ & -2+j2 \end{vmatrix}$$

$2\angle -90^\circ$

$\Delta_2 = (-5-j2)\left[0 + 52.5 \angle -156.8\right] + 50\angle 0^\circ \left[j2(-2+j2)\right]$

$\Delta_2 = 5.38 \angle -158.19 \times 52.5 \angle -156.8 + 50 \angle 0^\circ \left[-4j - 4\right]$

$\Delta_2 = 282.4 \angle -315^\circ + 50\angle 0^\circ \times 5.65 \angle -135^\circ$

$$\Delta_2 = 282.4 \angle{-315^\circ} + 282.5 \angle{-135^\circ}$$

$$\Delta_2 = \cancel{282.3}\ 199.6 + j199.6 - 199.7 - j199.7$$

$$\boxed{\Delta_2 = 0}$$

$$\therefore \boxed{I = 0}$$

Node analysis or voltage analysis :-

Procedure :-

→ All the principle node of the n/w are identified & one of them is taken as reference node at zero potential. Usually the node at which maximum no of branches are connected is taken as reference node.

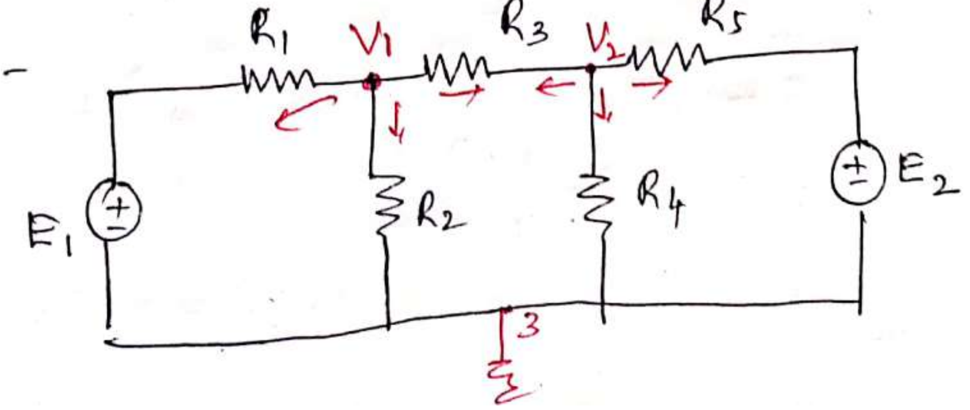
→ The remaining nodes are assigned with node voltages V_1, V_2, V_3 .... etc.

→ The node voltage equations are written using the KCL method.

→ The node voltage equations are solved using cramer's rule to get V_1, V_2, V_3 ... etc.

→ Once the node voltages are known the current in all the branches of the n/w can be found.

Ex:-



Applying KCL at node 1,

$$\frac{V_1 - E_1}{R_1} + \frac{V_1}{R_2} + \frac{V_1 - V_2}{R_3} = 0$$

$$\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right] V_1 - \frac{V_2}{R_3} = \frac{E_1}{R_1} \qquad \text{—— (1)}$$

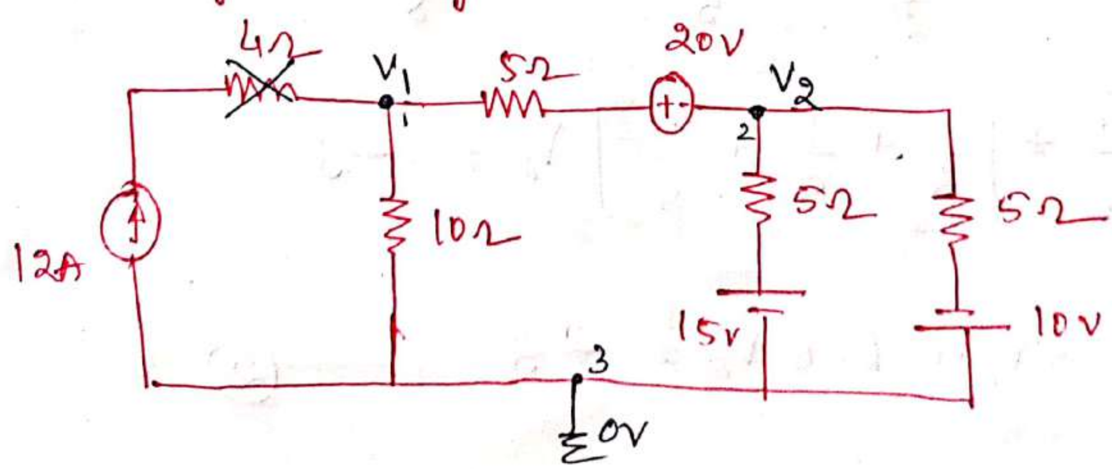
Applying KCL @ node 2.

$$\frac{V_2 - V_1}{R_3} + \frac{V_2}{R_4} + \frac{V_2 - E_2}{R_5} = 0$$

$$\frac{V_2}{R_3} - \frac{V_1}{R_3} + \frac{V_2}{R_4} + \frac{V_2}{R_5} - \frac{E_2}{R_5} = 0$$

$$-\frac{V_1}{R_3} + \left[\frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5}\right] V_2 = \frac{E_2}{R_5} \qquad \text{—— (2)}$$

1) In the network shown, find V_1 & V_2 using node voltage analysis.



Apply KCL at node 1

$$-12 + \frac{V_1}{10} + \frac{V_1 - 20 - V_2}{5} = 0$$

$$-12 + \frac{V_1}{10} + \frac{V_1}{5} - \frac{20}{5} - \frac{V_2}{5} = 0$$

$$-12 + \left[\frac{1}{10} + \frac{1}{5}\right] V_1 - 4 - \frac{V_2}{5} = 0$$

$$\left[\frac{1}{10} + \frac{1}{5}\right] V_1 - \frac{V_2}{5} = 16$$

$$0.3V_1 - 0.2V_2 = 16 \quad \text{——— (1)}$$

Apply KCL @ node 2.

$$\frac{V_2 + 20 - V_1}{5} + \frac{V_2 - 15}{5} + \frac{V_2 + 10}{5} = 0$$

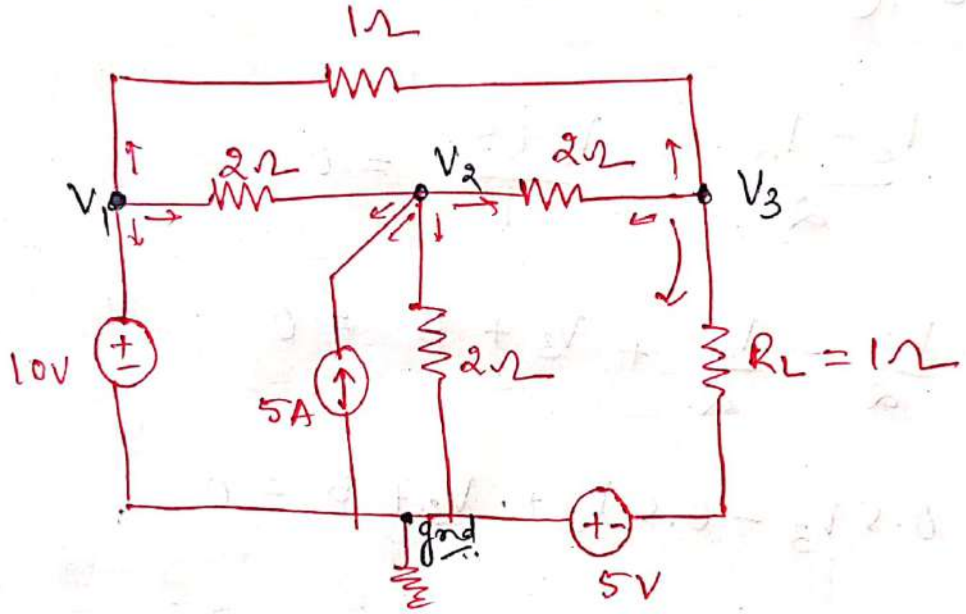
$$\frac{V_2}{5} + 4 - \frac{V_1}{5} + \frac{V_2}{5} - 3 + \frac{V_2}{5} + 2 = 0$$

$$-\frac{V_1}{5} + \left[\frac{1}{5} + \frac{1}{5} + \frac{1}{5}\right] V_2 = -3$$

$$-0.2V_1 + 0.6V_2 = -3 \quad \text{——— (2)}$$

$$\boxed{V_1 = 64.28\,V} \quad \& \quad \boxed{V_2 = 16.42\,V}$$

2) Find 'I' through R_L in the n/w shown



From the figure

$$V_1 - 10 = 0$$

$$\boxed{V_1 = 10\,V}$$

Apply KCL @ node V_2.

$$\frac{V_2 - V_1}{2} + \frac{V_2}{2} - 5 + \frac{V_2 - V_3}{2} = 0$$

$$\frac{V_2}{2} - \frac{V_1}{2} + \frac{V_2}{2} - 5 + \frac{V_2}{2} - \frac{V_3}{2} = 0$$

$$0.5V_2 - 0.5V_1 + 0.5V_2 - 5 + 0.5V_2 - 0.5V_3 = 0$$

$$-0.5V_1 + 1.5V_2 - 0.5V_3 - 5 = 0$$

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$$-0.5\times 10 + 1.5V_2 - 0.5V_3 - 5 = 0$$

$$1.5V_2 - 0.5V_3 = 10 \quad \text{——} \quad (1)$$

Apply KCL @ node V_3.

$$\frac{V_3 - V_1}{1} + \frac{V_3 - V_2}{2} + \frac{V_3 + 5}{1} = 0$$

$$V_3 - V_1 + \frac{V_3}{2} - \frac{V_2}{2} + V_3 + 5 = 0$$

$$V_3 - 10 + 0.5V_3 - 0.5V_2 + V_3 + 5 = 0$$

$$-0.5V_2 + 2.5V_3 = 5 \quad \text{——} \quad (2)$$

Solving (1) & (2) we get

$$\boxed{V_3 = 3.57 \text{ volts}}$$

Current through R_L is

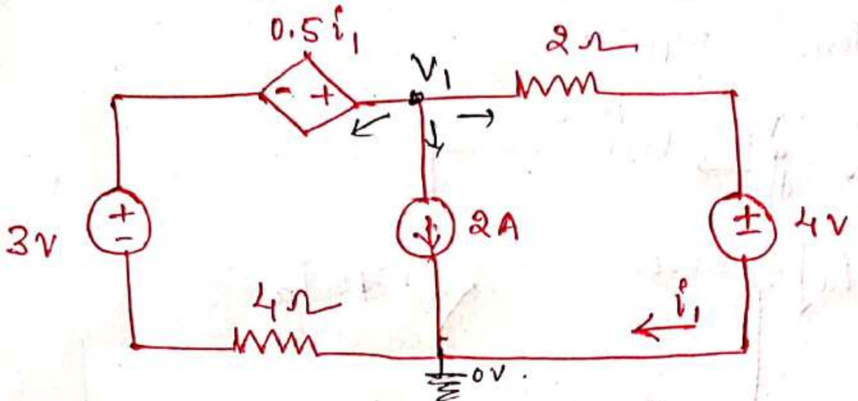
$$I = \frac{V}{R}$$

$$I = \frac{V_3 + 5}{R_L}$$

$$= \frac{3.57 + 5}{1}$$

$$\boxed{I = 8.57 \text{ amp}}$$

3) Find i_1 using nodal analysis.



From the figure $i_1 = \dfrac{V_1 - 4}{2}$

Apply KCL @ node V_1

$$\frac{V_1 - 0.5 i_1 - 3}{4} + 2 + \frac{V_1 - 4}{2} = 0$$

$$\frac{V_1}{4} - \frac{0.5 i_1}{4} - 0.75 + \cancel{2} + 0.5 V_1 - \cancel{2} = 0$$

$$0.25 V_1 - 0.125 \left[\frac{V_1 - 4}{2}\right] - 0.75 + 0.5 V_1 = 0$$

$$0.75 V_1 - 0.0625 V_1 + 0.25 - 0.75 = 0$$

$$0.6875 V_1 - 0.5 = 0$$

$$V_1 = \frac{0.5}{0.6875} = 0.727 \text{ volts}$$

$$\therefore \quad i_1 = \frac{0.727 - 4}{2} = \underline{-1.636 \text{ Amp}}$$

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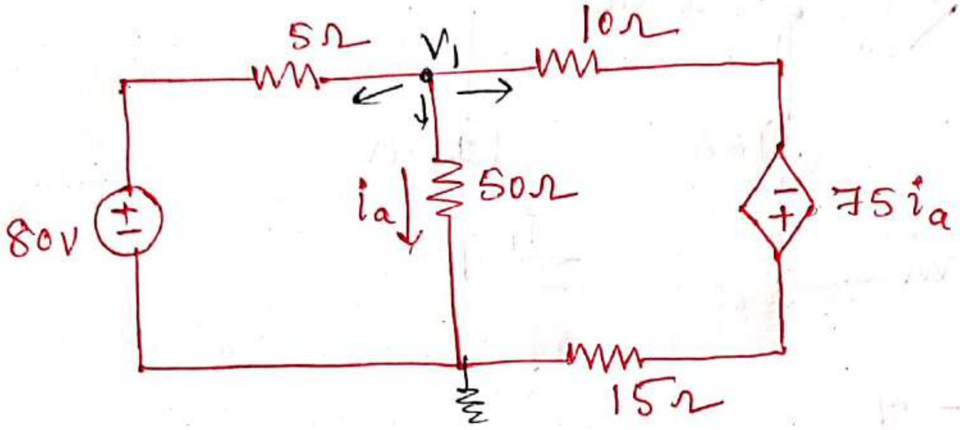
4) Find power delivered by the dependent voltage source in the n/w.



From the figure, $i_a = \frac{V_1}{50}$

Apply KCL @ node V_1..

$$\frac{V_1 - 80}{5} + \frac{V_1}{50} + \frac{V_1 + 75 i_a}{25} = 0$$

$$0.2V_1 - 16 + 0.02V_1 + 0.04V_1 + 3 i_a = 0$$

$$0.26V_1 + 3 i_a - 16 = 0$$

$$0.26V_1 + 3\left(\frac{V_1}{50}\right) = 16$$

$$0.32 V_1 = 16$$

$$V_1 = 16/0.32 = 50 \text{ volts}$$

$$\therefore i_a = \frac{V_1}{50} = 50/50 = 1 \text{ Amp}$$

→ Current through dependent voltage source branch

$$= \frac{V_1 + 75 i_a}{25} = \frac{V_1 + 75\left(\frac{V_1}{50}\right)}{25}$$

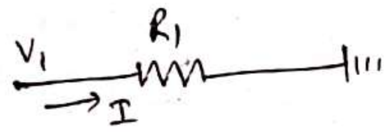
$$= \frac{50 + 75(1)}{25} = 5 \text{ Amp}$$

$\therefore$ power $= V \times I$

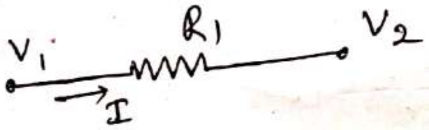
$$= 75 i_a \times 5 = 75 \times 1 \times 5$$

$$= \underline{\underline{375 \text{ watts}}}$$

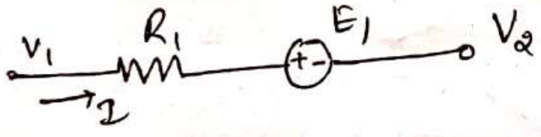
Note :-

1) 

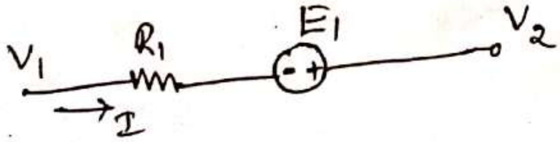
$$\boxed{I = \frac{V_1}{R_1}}$$

2) 

$$\boxed{I = \frac{V_1 - V_2}{R_1}}$$

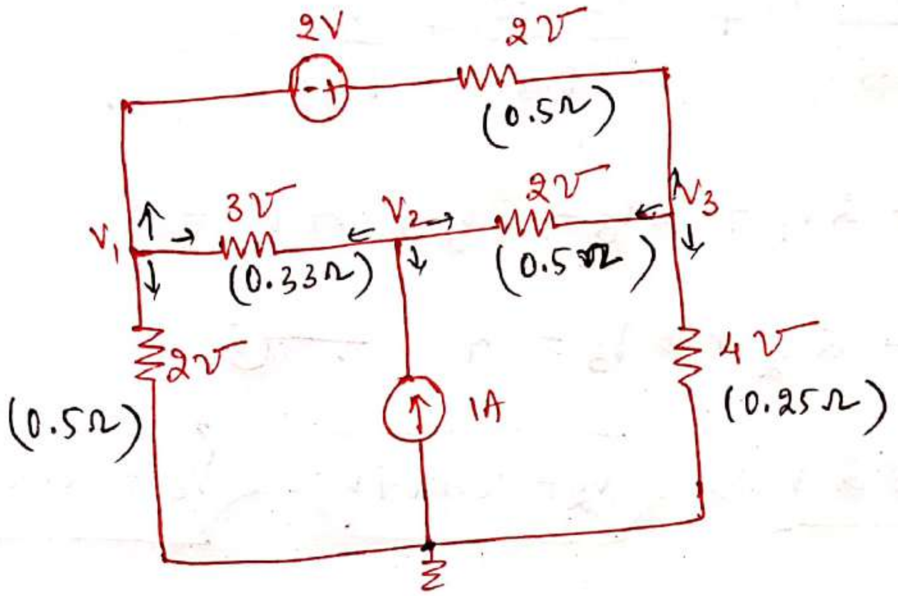
3) 

$$\boxed{I = \frac{V_1 - E_1 - V_2}{R_1}}$$

4) 

$$\boxed{I = \frac{V_1 + E_1 - V_2}{R_1}}$$

5) In the Circuit shown below, Use nodal analysis to determine the voltages V_2 & V_3.



Apply KCL @ node V_1

$$\frac{V_1}{0.5} + \frac{V_1 - V_2}{0.33} + \frac{V_1 + 2 - V_3}{0.5} = 0$$

$$2V_1 + 3V_1 - 3V_2 + 2V_1 - 2V_3 + 4 = 0$$

$$7V_1 - 3V_2 - 2V_3 = -4 \quad \text{——— (1)}$$

@ node 2

$$\frac{V_2 - V_1}{0.33} + \frac{V_2 - V_3}{0.5} - 1 = 0$$

$$-3V_1 + 3V_2 + 2V_2 - 2V_3 - 1 = 0$$

$$-3V_1 + 5V_2 - 2V_3 = 1 \quad \text{——— (2)}$$

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→ @ node 3

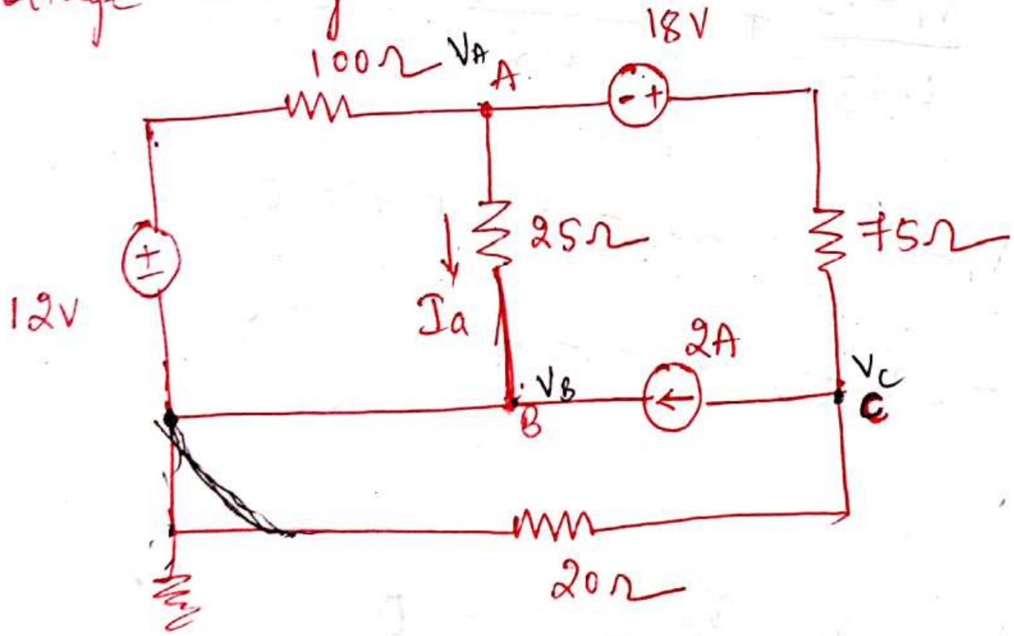
$$\frac{V_3 - 2 - V_1}{0.5} + \frac{V_3 - V_2}{0.5} + \frac{V_3}{0.25} = 0$$

$$2V_3 - 4 - 2V_1 + 2V_3 - 2V_2 + 4V_3 = 0$$

$$-2V_1 - 2V_2 + 8V_3 = 4 \quad \text{—— (3)}$$

$\boxed{V_1 = -0.382\text{ V}}$ $\boxed{V_2 = 0.147\text{ V}}$ $\boxed{V_3 = 0.441\text{ V}}$

6) Find I_a in the circuit shown using node voltage analysis.



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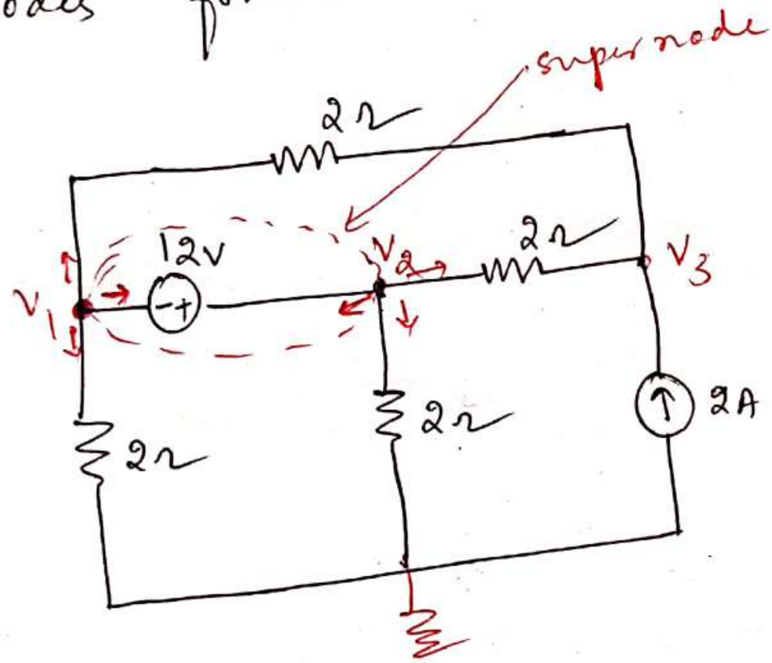
Super node :-

If the ideal voltage source [dependent or independent voltage source] is connected b/n any two non reference nodes, those nodes forms a super node.

Eg:-



→ 12v voltage source exists b/n nodes 1 & 2. Hence node 1 & node 2 forms super node

from super node

$$V_1 + 12 - V_2 = 0$$

$$\boxed{V_1 - V_2 = -12}$$

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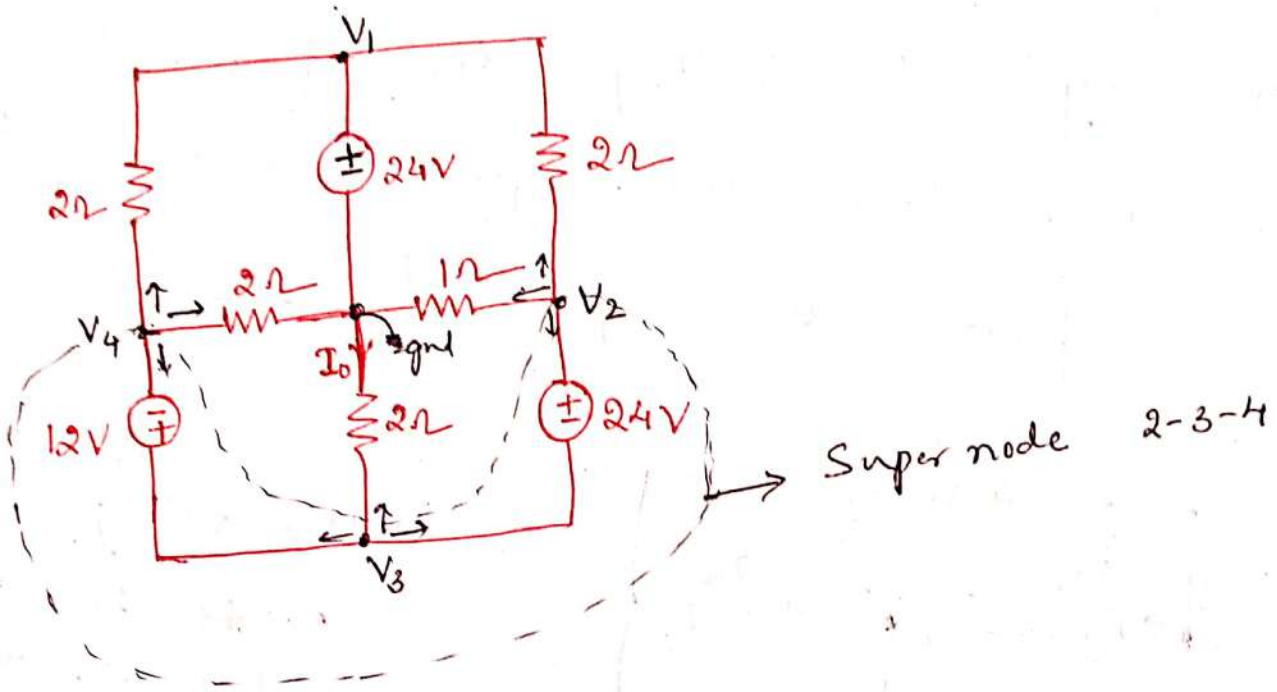
7) For the network shown below, find I_o using nodal analysis.

** Jan-14 10 marks



From the circuit:

$$V_1 - 24 = 0$$

$$\boxed{V_1 = 24 \text{ volts}} \quad \text{——— (1)}$$

→ 24V is in b/n 2 & 3

→ 12V is in b/n 4 & 3.

∴ 2-3-4 forms supernode.

From the super node,

$$\boxed{V_2 - V_3 = 24\,V} \quad \text{——— (2)}$$

$$\boxed{V_3 - V_4 = 12\,V} \quad \text{——— (3)}$$

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Apply KCL @ node '2-3-4',

$$\frac{V_4 - V_1}{2} + \frac{V_4}{2} + \frac{V_2 - V_1}{2} + \frac{V_2}{1} + \frac{V_3}{2} = 0$$

~~$2V_4 - 2V_1 + 2V_4 + 2$~~

$$0.5\,V_4 - 0.5\,V_1 + 0.5\,V_4 + 0.5\,V_2 - 0.5\,V_1 + V_2 + 0.5\,V_3 = 0.$$

24

$$-V_1 + 1.5\,V_2 + 0.5\,V_3 + V_4 = 0$$

$$1.5\,V_2 + 0.5\,V_3 + V_4 = 24 \quad \text{--- (4)}$$

Solving (2), (3) & (4)

$$\left\{\begin{array}{l} V_2 - V_3 + 0V_4 = 24 \quad \text{--- (2)*} \\ 0 + V_3 - V_4 = 12 \quad \text{--- (3)*} \\ 1.5\,V_2 + 0.5\,V_3 + V_4 = 24 \quad \text{--- (4)*} \end{array}\right.$$

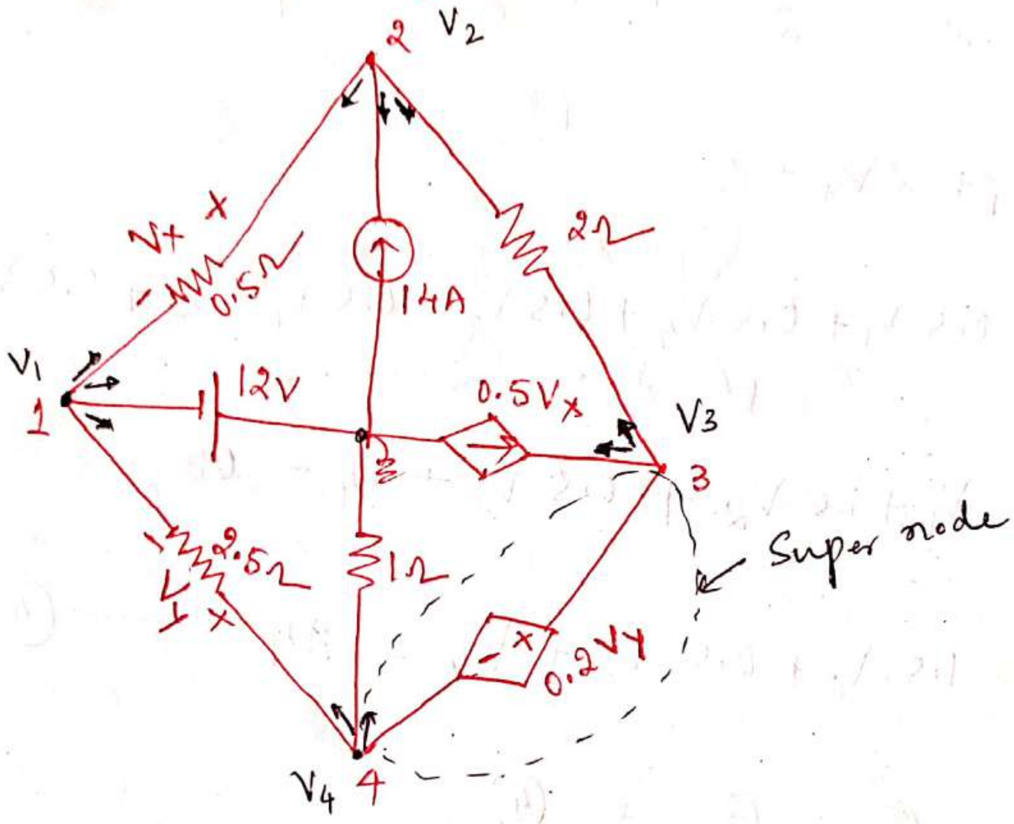
$$\boxed{V_2 = 24\ V} \quad \boxed{V_3 = 0\ V} \quad \boxed{V_4 = -12\ V}$$

From the figure $I_0 = \dfrac{0 - V_3}{2} = \underline{\underline{0\ \text{Amp}}}$

8) Find the voltages at nodes 1, 2, 3, 4

Jan-8

for the n/w using nodal analysis.



From the circuit,

$$V_1 + 12 = 0$$

$$\boxed{V_1 = -12 \text{ volts}}$$

Apply KCL @ node 2,

$$\frac{V_2 - V_1}{0.5} - 14 + \frac{V_2 - V_3}{2} = 0$$

$$2V_2 - 2V_1 - 14 + 0.5V_2 - 0.5V_3 = 0$$

-2×-12

$$-2V_1 + 2.5V_2 - 0.5V_3 = 14$$

$\cdot 24$

$$2.5V_2 - 0.5V_3 = 14 - 24$$

$$2.5V_2 - 0.5V_3 = -10 \quad \text{———} \quad (1)$$

→ $0.2V_y$ exists b/n node 3 & 4

∴ 3 & 4 forms super node.

from super node,

$$\frac{V_3 - V_2}{2} - 0.5V_x + \frac{V_4}{1} + \frac{V_4 - V_1}{2.5} = 0$$

$$0.5V_3 - 0.5V_2 - 0.5V_x + V_4 + 0.4V_4 - 0.4V_1 = 0$$

$$-0.4V_1 - 0.5V_2 + 0.5V_3 + 1.4V_4 - 0.5V_x = 0$$

But $V_x = V_2 - V_1$ & $\underline{\underline{V_1 = -12 \text{ volts}}}$.

$$\therefore \quad -0.4(-12) - 0.5V_2 + 0.5V_3 + 1.4V_4 - 0.5(V_2 - V_1) = 0.$$

0.5 × −12

$$\rightarrow \quad 4.8 - 0.5V_2 + 0.5V_3 + 1.4V_4 - 0.5V_2 + 0.5V_1 = 0$$

−12

$$\rightarrow \quad 4.8 - V_2 + 0.5V_3 + 1.4V_4 - 6 = 0$$

$$-V_2 + 0.5V_3 + 1.4V_4 = 1.2 \quad \text{———} \quad (2)$$

from super node.

$$V_3 - V_4 = 0.2V_y$$

But $V_y = V_4 - V_1$

$$\rightarrow V_3 - V_4 = 0.2(V_4 - V_1)$$

$$\rightarrow V_3 - V_4 = 0.2V_4 - 0.2V_1$$

or $0.2V_1 + V_3 - V_4 - 0.2V_4 = 0$

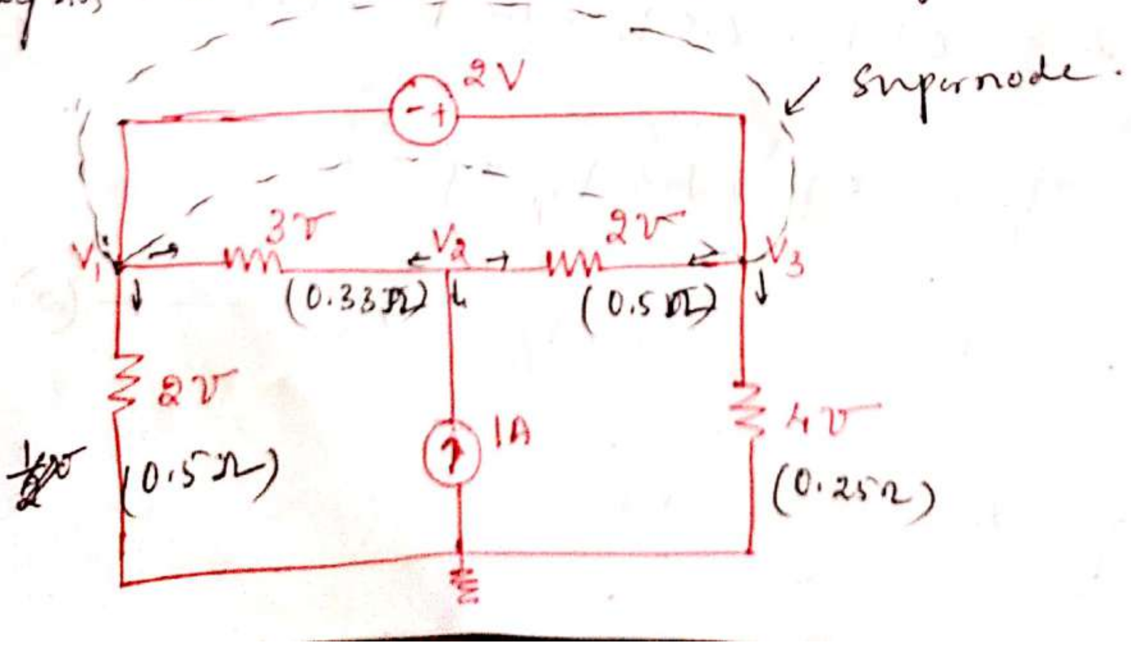
$$0.2(-12) + V_3 - 1.2V_4 = 0$$

$$V_3 - 1.2V_4 = 2.4 \quad \text{——— (3)}$$

Solving (1), (2), & (3)

$\boxed{V_1 = -12V}$ $\boxed{V_2 = -4V}$ $\boxed{V_3 = 0V}$ $\boxed{V_4 = -2V}$

9) In the Circuit shown below, use nodal analysis to determine the voltages V_2 & V_3



From the super node (1-3)

$$\boxed{V_3 - V_1 = 2V} \rightarrow -V_1 + V_3 = 2V \quad \text{——— (1)}$$

KCL @ super node (1-3)

$$\frac{V_1}{0.5} + \frac{V_1 - V_2}{0.33} + \frac{V_3 - V_2}{0.5} + \frac{V_3}{0.25} = 0.$$

$$2V_1 + 3V_1 - 3V_2 + 2V_3 - 2V_2 + 4V_3 = 0.$$

$$5V_1 - 5V_2 + 6V_3 = 0 \quad \text{——— (2)}$$

→ Apply KCL @ node 2

$$\frac{V_2 - V_1}{0.33} - 1 + \frac{V_2 - V_3}{0.5} = 0$$

$$3V_2 - 3V_1 - 1 + 2V_2 - 2V_3 = 0$$

$$-3V_1 + 5V_2 - 2V_3 = 1 \quad \text{——— (3)}$$

Solving (1), (2) & (3) we get -

$$\boxed{V_1 = -1.667 \text{ volts}} \quad \boxed{V_2 = -0.1667 \text{ volts}}$$

$$\boxed{V_3 = 0.833 \text{ volts}}$$

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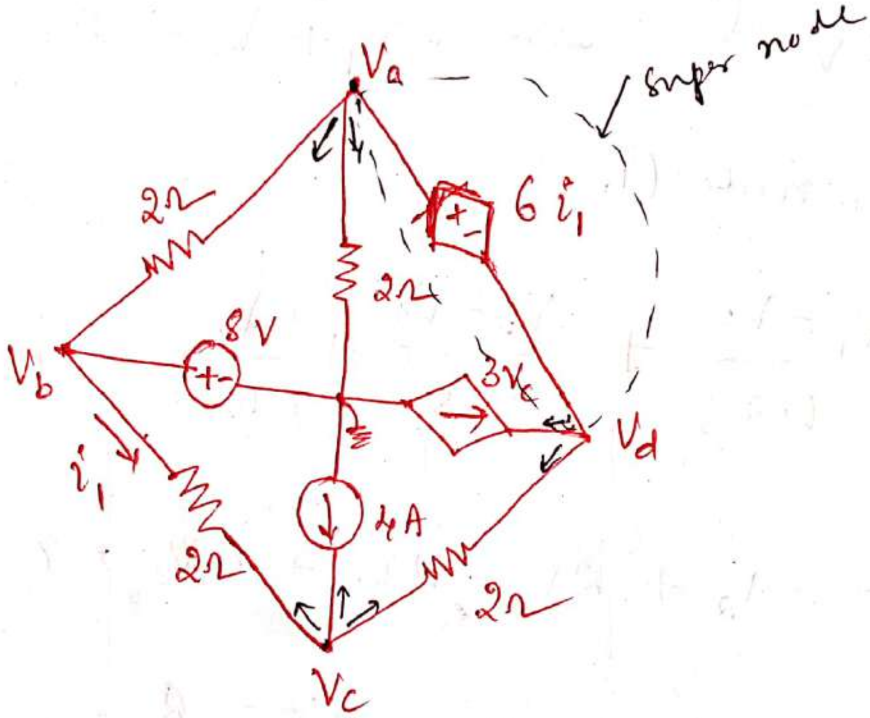
10) Find V_c & V_d using nodal analysis.



From the figure, (@ node V_b)

$$V_b - 8 = 0 \Rightarrow \boxed{V_b = 8V}$$

Apply KCL @ node c

$$\frac{V_c - V_b}{2} + \frac{V_c - V_d}{2} - 4 = 0$$

$$0.5V_c - 0.5V_b + 0.5V_c - 0.5V_d - 4 = 0$$

$$-0.5V_b + V_c - 0.5V_d - 4 = 0$$

$$-0.5(8) + V_c - 0.5V_d - 4 = 0$$

$$V_c - 0.5 V_d = 8 \quad \text{—— (1)}$$

from super node, (a-d)

$$V_a - V_d = 6 i_1$$

from the figure,

$$i_1 = \frac{V_b - V_c}{2}$$

$$V_a - V_d = {}^{3}\cancel{6}\left[\frac{V_b - V_c}{\cancel{2}}\right]$$

$$V_a - V_d = 3V_b - 3V_c$$

$$\boxed{V_a + 3V_c - V_d = 24} \quad \text{—— (2)}$$

$$V_a - V_d - 3V_b + 3V_c = 0$$

$$V_a - 3 V_b^{\,8} + 3V_c - V_d = 0 \quad \text{—— (2)}$$

Apply KCL to super node (a-d)

$$\frac{V_a - V_b}{2} + \frac{V_a}{2} - 3V_c + \frac{V_d - V_c}{2} = 0$$

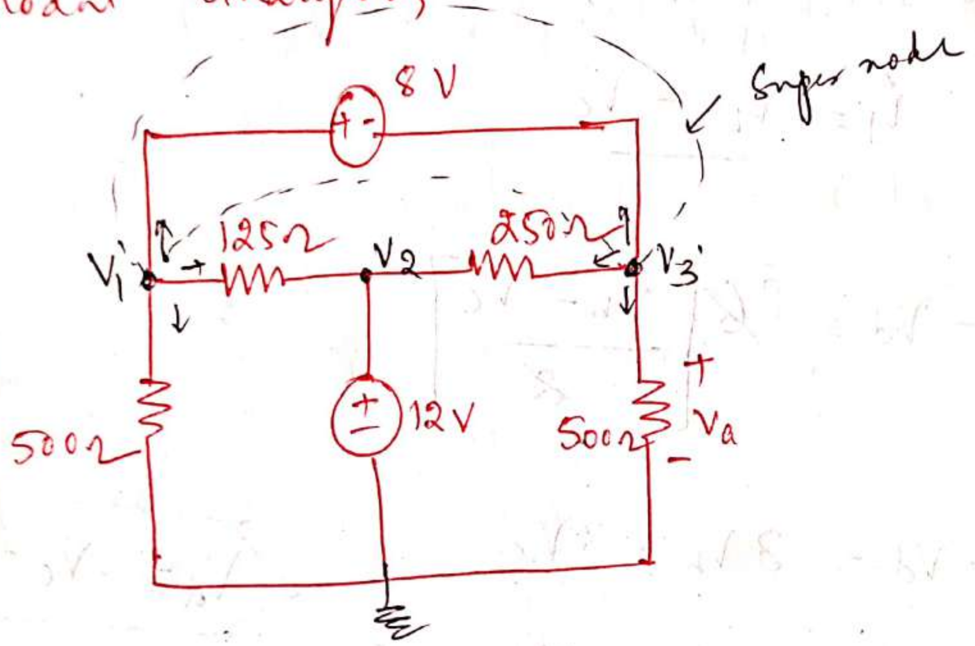
$$0.5V_a - 0.5V_b + 0.5V_a - 3V_c + 0.5V_d - 0.5V_c = 0$$

$$V_a - 0.5 \overset{8}{V_b} - 3.5V_c + 0.5V_d = 0$$

$$\boxed{V_a - 3.5V_c + 0.5V_d = 4} \quad \text{—— (3)}$$

$\boxed{V_a = 9.14}$ $\boxed{V_c = -1.14}$ $\boxed{V_d = -18.28 \text{ volt}}$

11) For the electrical n/w, Find V_a Using nodal analysis



@ node 2 :-

$$V_2 - 12 = 0 \Rightarrow \boxed{V_2 = 12 V}$$

From Super node (1-3)

$$V_1 - V_3 = 8 V \quad \text{——— (1)}$$

Apply KCL to Super node,

$$\frac{V_1}{500} + \frac{V_1 - V_2}{125} + \frac{V_3 - V_2}{250} + \frac{V_3}{500} = 0$$

$$2\times10^{-3}V_1 + 8\times10^{-3}V_1 - 0.096 + 4\times10^{-3}V_3 - 0.048 + 2\times10^{-3}V_3 = 0$$

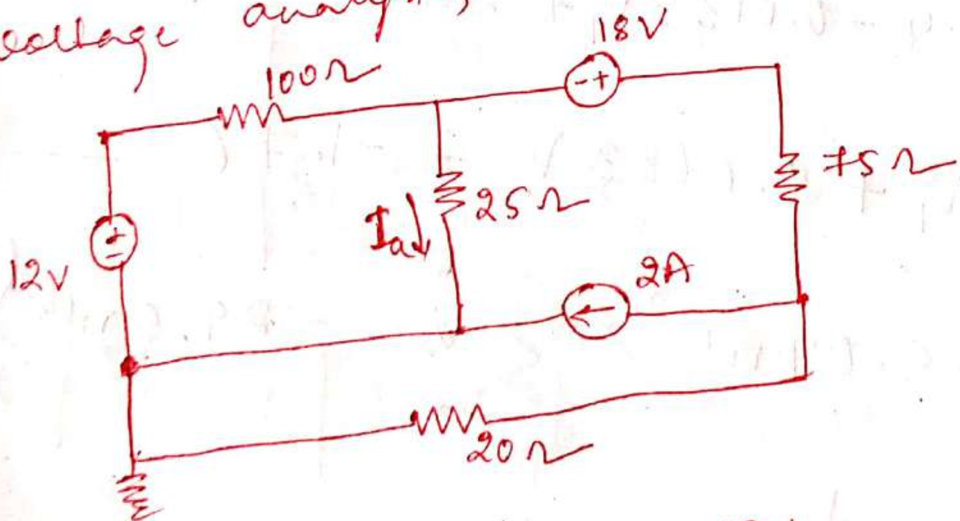
$$10\times10^{-3}V_1 + 6\times10^{-3}V_3 = 0.144 \quad \text{—— (2)}$$

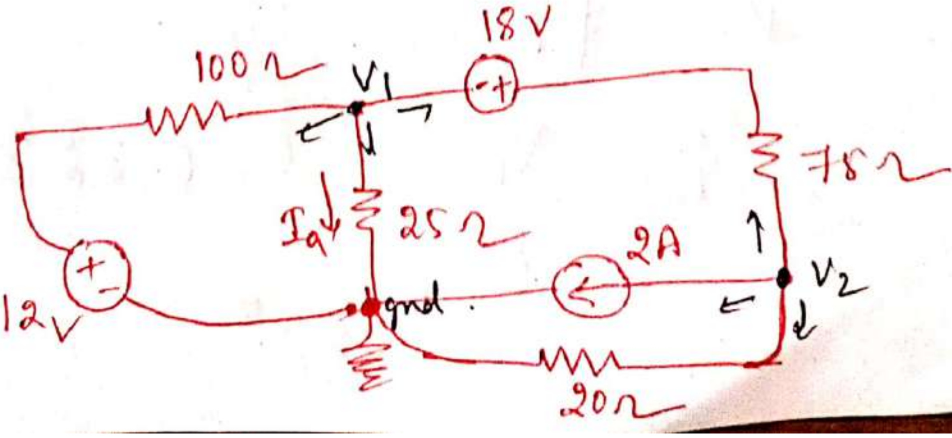
$\boxed{V_1 = 12V}$ $\boxed{V_3 = 4\text{ volts}}$

from the figure.

$\boxed{V_a = V_3 = 4\text{ volts}}$.

6) Find I_a in the circuit shown using node voltage analysis





Apply KCL @ node 1

$$\frac{V_1 - 12}{100} + \frac{V_1}{25} + \frac{V_1 + 18 - V_2}{75} = 0$$

$$0.01V_1 - 0.12 + 0.04V_1 + 0.0133V_1 + 0.24 - 0.0133V_2 = 0$$

$$0.0633V_1 - 0.0133V_2 = -0.12 \quad \text{—— (1)}$$

Apply KCL @ node 2

$$\frac{V_2 - 18 - V_1}{75} + 2 + \frac{V_2}{20} = 0$$

$$0.0133V_2 - 0.24 - 0.0133V_1 + 2 + 0.05V_2 = 0$$

$$-0.0133V_1 + 0.0633V_2 = -1.76 \quad \text{—— (2)}$$

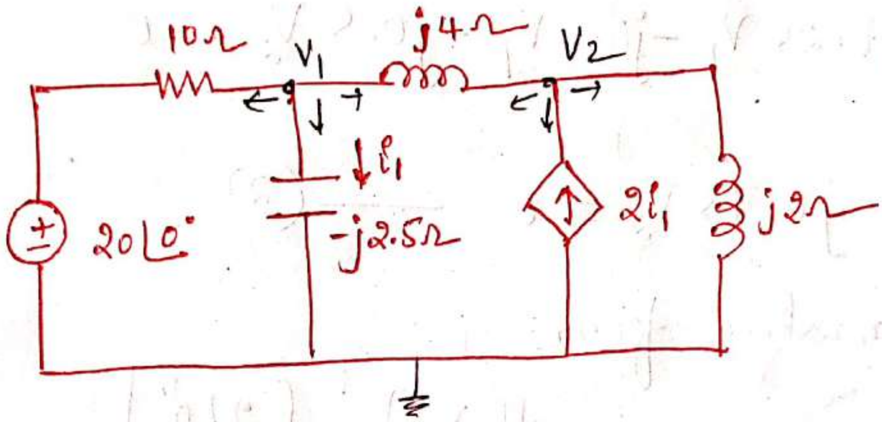
$V_1 = -8.09$ volts $V_2 = -29.5$ volts

From the fig.

$$i_a = \frac{V_1}{25} = -0.323 \text{ volts}$$

Problems on AC Analysis :-

1) Find i_1 for the Circuit using nodal analysis.



From the Circuit

$$i_1 = \frac{V_1}{-j2.5\Omega}$$

$$\left\{ \begin{aligned} \frac{1}{j} &= -j \\ \frac{1}{-j} &= j \end{aligned} \right.$$

Apply KCL @ node 1

$$\frac{V_1 - 20\angle 0^\circ}{10} + \frac{V_1}{-j2.5} + \frac{V_1 - V_2}{j4} = 0$$

$$\frac{V_1}{10} - \frac{20\angle 0^\circ}{10} + j\frac{V_1}{2.5} + (-j)\frac{V_1}{4} + j\frac{V_2}{4} = 0$$

$$0.1V_1 - 2\angle 0^\circ + j0.4V_1 - j0.25V_1 + j0.25V_2 = 0$$

$$[0.1 + \underbrace{j0.4 - j0.25}_{j0.15}]V_1 + j0.25V_2 = 2\angle 0^\circ \quad \text{—— (1)}$$

Apply KCL @ node 2.

$$\frac{V_2 - V_1}{j4} - 2i_1 + \frac{V_2}{j2} = 0$$

$$-j0.25(V_2 - V_1) - \frac{2V_1}{-j2.5} + (-j0.5)V_2 = 0$$

$$-j0.25V_2 + j0.25V_1 - j0.8V_1 - j0.5V_2 = 0$$

$$-j0.55V_1 - j0.75V_2 = 0 \quad \text{——} \quad (2)$$

In matrix form:

$$\begin{bmatrix} 0.1+j0.15 & j0.25 \\ -j0.55 & -j0.75 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 2\angle 0^\circ \\ 0 \end{bmatrix}$$

$$\Delta = \begin{vmatrix} 0.1+j0.15 & j0.25 \\ -j0.55 & -j0.75 \end{vmatrix}$$

$$= \left[(0.1+j0.15)(-j0.75) + (j0.25)(j0.55)\right]$$

$$= 0.1125 - j0.075 - 0.1375$$

$$= -0.025 - j0.075$$

$$\Delta_1 = \begin{vmatrix} 2\angle 0^\circ & j0.25 \\ 0 & -j0.75 \end{vmatrix}$$

$$= -j1.5$$

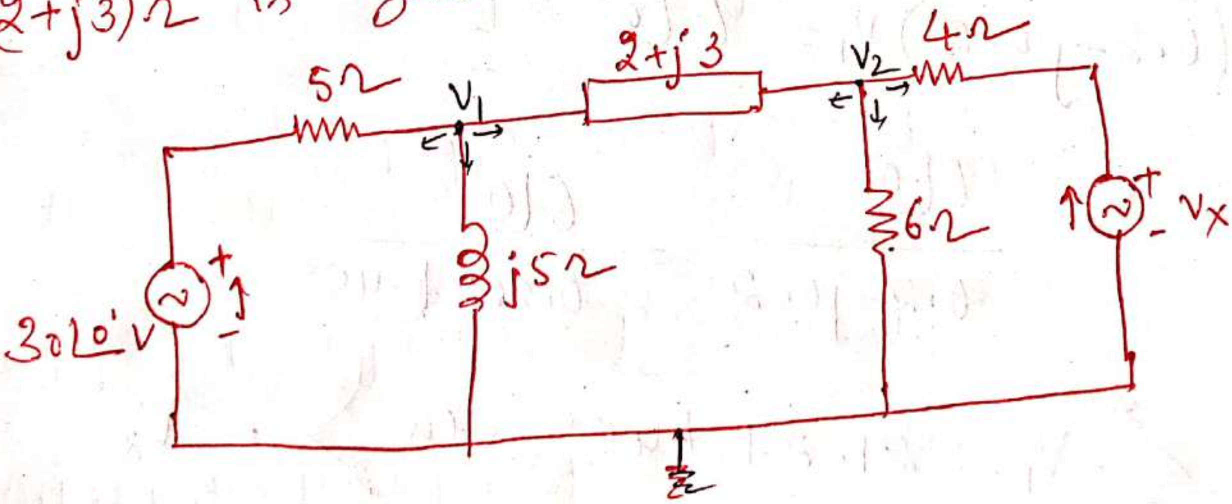
$$\therefore V_1 = \frac{\Delta_1}{\Delta} = \frac{-1.5j}{-0.025 - j0.075}$$

$$\boxed{V_1 = 18.97 \angle 18.43^\circ \text{ V}}$$

$$\therefore i_1 = \frac{18.97 \angle 18.43}{-j2.5} = \frac{18.97 \angle 18.43}{2.5 \angle -90^\circ}$$

$$\boxed{i_1 = 7.59 \angle 108^\circ.43 \text{ Amp}}$$

2) Use the nodal analysis & find the value of V_x in the circuit shown in below fig such that the current through the impedance $(2+j3)\Omega$ is zero



From the figure (data)

$$I_{(2+j3)\Omega} = \frac{V_1 - V_2}{2+j3}$$

Given the current $\boxed{I_{(2+3)\Omega} = 0}$

$$\therefore \quad 0 = \frac{V_1 - V_2}{2+j3}$$

$$0 = V_1 - V_2$$

$$\Rightarrow \boxed{V_1 = V_2} \quad (\because \text{Equipotential})$$

Apply KCL @ node 1,

$$\frac{V_1 - 30\angle 0^\circ}{5} + \frac{V_1}{j5} + \cancel{\frac{V_1 - V_2}{2+j3}}^{\,0} = 0$$

$$0.2V_1 - 6\angle 0^\circ - j0.2V_1 = 0$$

$$(0.2 - j0.2)V_1 = 6\angle 0^\circ$$

$$V_1 = \frac{6\angle 0^\circ}{0.2 - j0.2} = \frac{6\angle 0^\circ}{0.282\angle -45^\circ}$$

$$\boxed{V_1 = 21.27\angle 45^\circ \text{ volts}} = V_2$$

Apply KCL @ node 2,

$$\cancel{\frac{V_2 - V_1}{2+j3}}^{\,0} + \frac{V_2}{6} + \frac{V_2 - V_x}{4} = 0$$

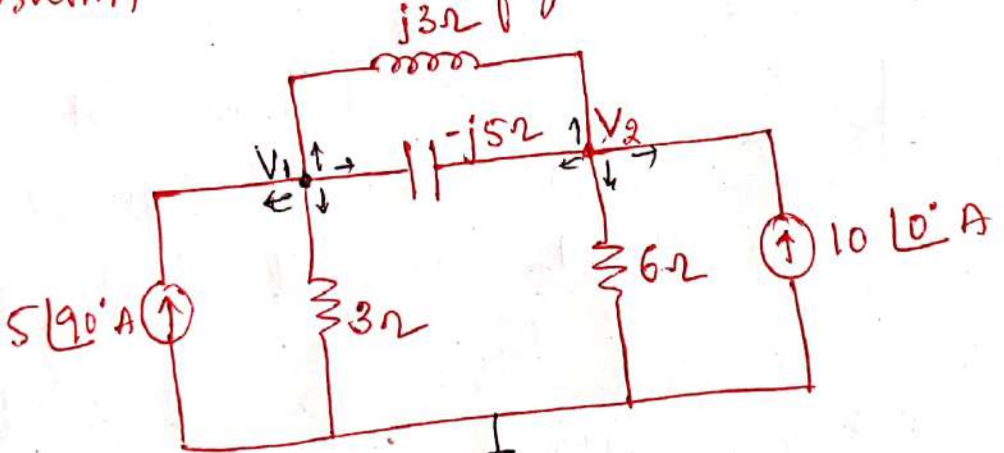
$$0.167 V_2 + 0.25 [V_2 - V_x] = 0$$

$$0.417 V_2 = 0.25 V_x$$

$$V_x = \frac{0.417 V_2}{0.25} = \frac{0.417 \times 21.27 \angle 45^\circ}{0.25}$$

$$\boxed{V_x = 35.47 \angle 45^\circ \text{ volts}}$$

3) Use nodal analysis to find V_2 in the circuit shown in the figure.



At node 1

$$-5\angle 90^\circ + \frac{V_1}{3} + \frac{V_1 - V_2}{-j5} + \frac{V_1 - V_2}{j3} = 0$$

$$0.33 V_1 + j0.2 V_1 - j0.2 V_2 - j0.33 V_1 + j0.33 V_2 = 5\angle 90^\circ$$

$$[0.33 - j0.133] V_1 + j0.133 V_2 = 5\angle 90^\circ \quad \text{—— (1)}$$

At node 2

$$\frac{V_2}{6} + \frac{V_2 - V_1}{-j5} + \frac{V_2 - V_1}{j3} - 10\angle 0^\circ = 0$$

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$$0.166\,V_2 + j\,0.2V_2 - j\,0.2V_1 - j\,0.333\,V_2 + j\,0.33\,V_1$$
$$= 10\angle 0^\circ$$

$$\cancel{0.166} \; -j\,0.133\,V_1 + (0.166 - j\,0.133)\,V_2 = 10\angle 0^\circ \quad \text{--- (2)}$$

$$\Delta = \begin{vmatrix} 0.33 - j\,0.133 & 0.133j \\ -0.133j & 0.166 - j\,0.133 \end{vmatrix}$$

$$\Delta = \left[(0.33 - j\,0.133)(0.166 - j\,0.133) + (0.133j)(0.133j) \right]$$

$$= 0.0547 - j\,0.022 - j\,0.0442 - 0.01768$$
$$- 0.01768$$

$$= 0.0193 - j\,0.0658$$

$$\Delta = \underline{0.0686 \angle -73.67}$$

$$\Delta_2 = \begin{vmatrix} 0.33 - j\,0.133 & 5j \\ -0.133j & 10 \end{vmatrix}$$

$$= (0.33 - j\,0.133)10 + 5j\,(0.133j)$$

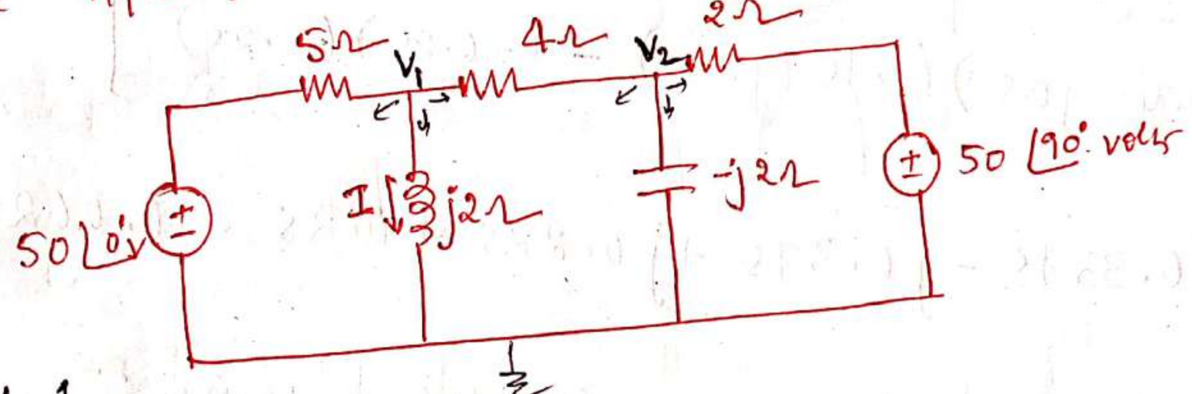
$$\Delta_2 = 3.33 - j1.33 - 0.665$$

$$\Delta_2 = 2.665 - j1.33 = 2.978 \angle -26.52$$

$$\therefore V_2 = \frac{\Delta_2}{\Delta} = \frac{2.978 \angle -26.52}{0.0686 \angle -73.67}$$

$$\boxed{V_2 = 43.41 \angle 47.15^\circ \text{ volts}}$$

4) Use node voltage technique to find I in the n/w shown.



@ node 1

$$\frac{V_1 - 50\angle 0^\circ}{5} + \frac{V_1}{j2} + \frac{V_1 - V_2}{4} = 0$$

$$0.2V_1 - 10\angle 0^\circ - j0.5V_1 + 0.25V_1 - 0.25V_2 = 0$$

$$(0.45 - j0.5)V_1 - 0.25V_2 = 10\angle 0^\circ \quad \text{——— (1)}$$

@ node 2

$$\frac{V_2 - V_1}{4} + \frac{V_2}{-j2} + \frac{V_2 - 50\angle 90^\circ}{2} = 0$$

$$0.25V_2 - 0.25V_1 + j0.5V_2 + 0.5V_2 - 25\angle 90^\circ = 0$$

$$-0.25V_1 + (0.75 + j0.5)V_2 = 25\angle 90^\circ \quad \text{—— (2)}$$

$$\Delta = \begin{vmatrix} 0.45 - j0.5 & -0.25 \\ -0.25 & 0.75 + j0.5 \end{vmatrix}$$

$$\Delta = \left[(0.45 - j0.5)(0.75 + j0.5) - (-0.25)(-0.25)\right]$$

$$= 0.3375 - j0.375 + j0.225 + 0.25 - 0.0625$$

$$= 0.525 - j0.15 = 0.546\angle -15.94^\circ$$

$$\Delta_1 = \begin{vmatrix} 10 & -0.25 \\ 25j & 0.75 + j0.5 \end{vmatrix}$$

$$= 7.5 + j5 + j6.25$$

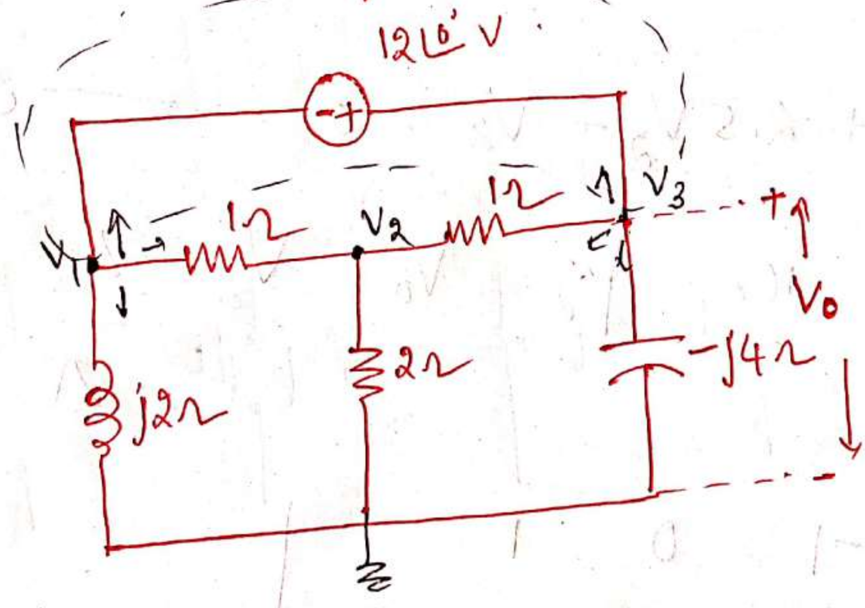
$$\Delta_1 = 7.5 + j11.25 = 13.52 \angle 56.3$$

$$V_1 = \frac{\Delta_1}{\Delta} = 24.76 \angle 72.24°$$

$$I_1 = \frac{V_1}{j2} = \frac{24.76 \angle 72.24}{2 \angle 90}$$

$$\boxed{I_1 = 12.38 \angle -17.76 \text{ Amp}}$$

5) Use nodal analysis to find V_o in the ckt-



from Super node,

$$V_3 - V_1 = 12\angle 0° \longrightarrow -V_1 + 0V_2 + V_3 = 12\angle 0°$$

KCL @ Supernode,

$$\frac{V_1}{j2} + \frac{V_1 - V_2}{1} + \frac{V_3 - V_2}{1} + \frac{V_3}{-j4} = 0$$

$$-j0.5V_1 + V_1 - V_2 + V_3 - V_2 + j0.25V_3 = 0$$

$$(1-j0.5)V_1 - 2V_2 + (1+j0.25)V_3 = 0 \quad \text{—— (2)}$$

KCL @ node 2

$$\frac{V_2 - V_1}{1} + \frac{V_2}{2} + \frac{V_2 - V_3}{1} = 0$$

$$V_2 - V_1 + 0.5V_2 + V_2 - V_3 = 0$$

$$-V_1 + 2.5V_2 - V_3 = 0 \quad \text{—— (3)}$$

from the fig $V_0 = V_3 = \frac{\Delta_3}{\Delta}$

$$\Delta = \begin{vmatrix} -1 & 0 & 1 \\ 1-j0.5 & -2 & (1+j0.25) \\ -1 & 2.5 & -1 \end{vmatrix}$$

$$\Delta = [-1(2 - 2.5 - j0.625) + 1(2.5 - j1.25 - 2)]$$

$$\Delta = \left[-1(-0.5 - j0.625) + 1(0.5 - j1.25) \right]$$

$$\Delta = 0.5 + j0.625 + 0.5 - j1.25$$

$$\Delta = 1 - 0.625j = 1.179 \angle -32^\circ$$

$$\Delta_3 = \begin{vmatrix} -1 & 0 & 12 \\ 1-j0.5 & -2 & 0 \\ -1 & 2.5 & 0 \end{vmatrix}$$

$$\Delta_3 = \left[-1(\cancel{0}-0) + 12\left(2.5 - j\,\overset{j1.25}{\cancel{0.625}} - 2\right) \right]$$

$$\Delta_3 = 12\left(0.5 - j\,\overset{1.25}{\cancel{0.625}}\right) = 6 - j15$$

$$\hookrightarrow = 6 - \overset{j15}{\cancel{j7.5}} = \cancel{9.6 \angle -51.3^\circ}$$

$$16.155 \angle -68.19$$

$$\therefore V_0 = \frac{\cancel{9.6 \angle -51.3^\circ}}{1.179 \angle -32^\circ} = \cancel{8.14 \angle -19.3^\circ}$$

$$V_0 = \frac{16.155 \angle -68.19}{1.179 \angle -32^\circ} = 13.70 \angle -36.2^\circ$$

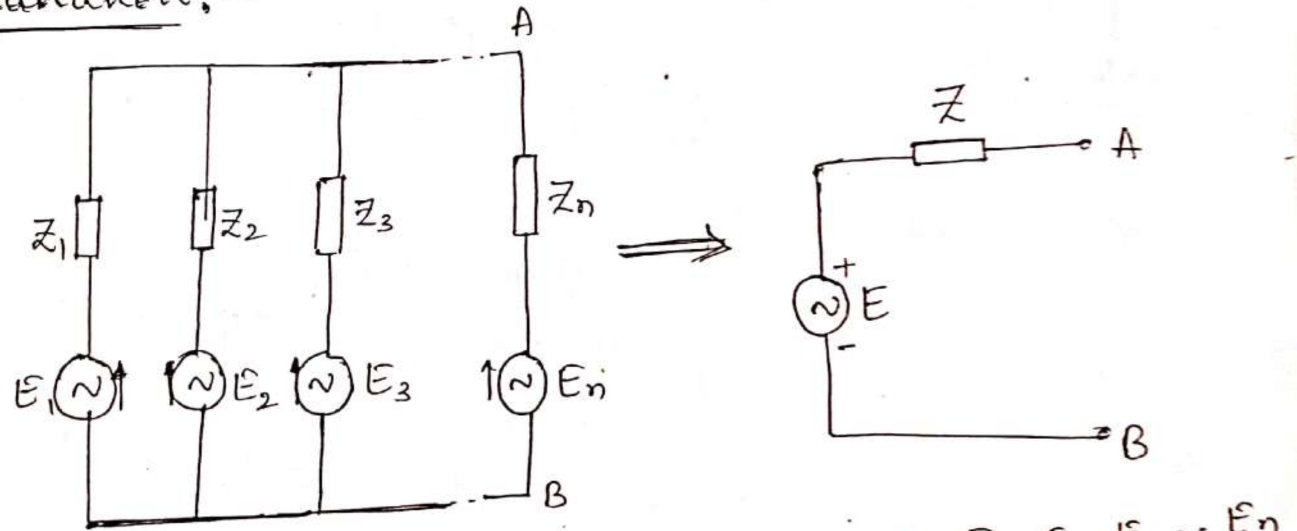
1. Millman's theorem :-

Statement-: "If n no of voltage source $E_1, E_2, E_3 \ldots E_n$ with their internal impedance $Z_1, Z_2 \ldots Z_n$ resp are in parallel. Then these voltage sources may be replaced by a single voltage source of voltage E with the internal impedance Z where

$$E = \frac{E_1Y_1 + E_2Y_2 + E_3Y_3 + \ldots E_nY_n}{Y_1 + Y_2 + Y_3 + \ldots + Y_n}$$

And $Z = \dfrac{1}{Y_1 + Y_2 + \ldots Y_n}$

Explanation:-



Consider n number of voltage source $E_1, E_2, E_3 \ldots E_n$ with their internal impedance $Z_1, Z_2, Z_3 \ldots Z_n$ are connected in parallel are as shown in fig above.

W.K.T $I = I_1 + I_2 + I_3 + \ldots I_n$

But
$$\left.\begin{aligned} I &= EY \\ I_1 &= E_1Y_1 \\ I_2 &= E_2Y_2 \quad \ldots \; I_n = E_nY_n \end{aligned}\right\} \text{——} (1)$$

where $Y_1, Y_2, Y_3 \cdots Y_n$ are the admittences connected in parallel corresponding to impedance $Z_1, Z_2, \cdots Z_n$ respectively

$$\therefore \quad E = \frac{I}{Y}$$

$$E = \frac{I_1 + I_2 + I_3 + \cdots I_n}{Y_1 + Y_2 + \cdots Y_n}$$

$$\boxed{E = \frac{E_1 Y_1 + E_2 Y_2 + E_3 Y_3 + \cdots E_n Y_n}{Y_1 + Y_2 + Y_3 + \cdots + Y_n}}$$

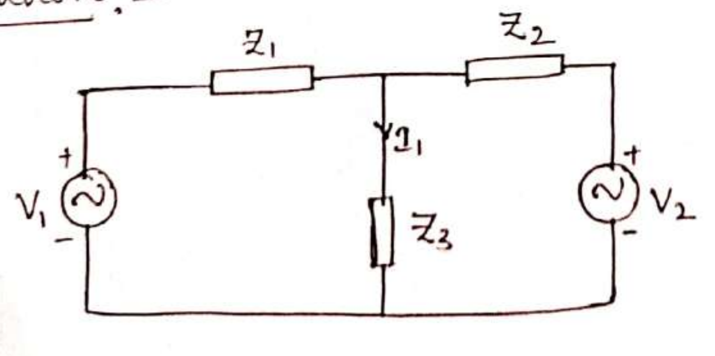
and $\boxed{Z = \frac{1}{Y} = \frac{1}{Y_1 + Y_2 + Y_3 + \cdots Y_n}}$ hence the proof.

2) **Superposition theorem:-**

Statement:- "In any linear bilateral network containing more than one independent source, the current or vg across any element in the network is equal to sum of the individual current or voltage produced by each source acting alone, setting all the other independent sources to zero."

If it is a vg src, it is replaced by short circuit. If it is a current source, it is replaced by an open circuit.

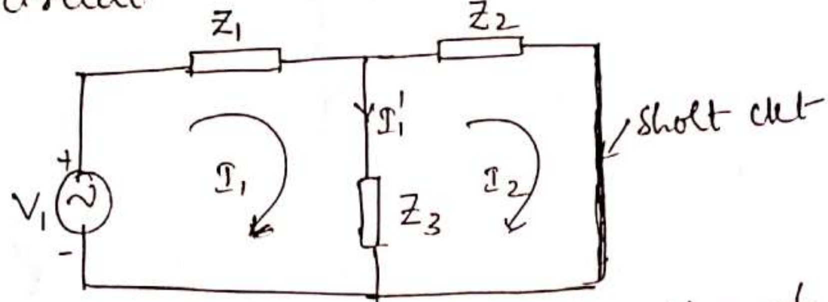
Explanation:-



Consider a linear bilateral network having two voltage source as shown in fig above.

Let I_1 be the current flowing through Z_3 when both the vg sources V_1 & V_2 are present in the circuit.

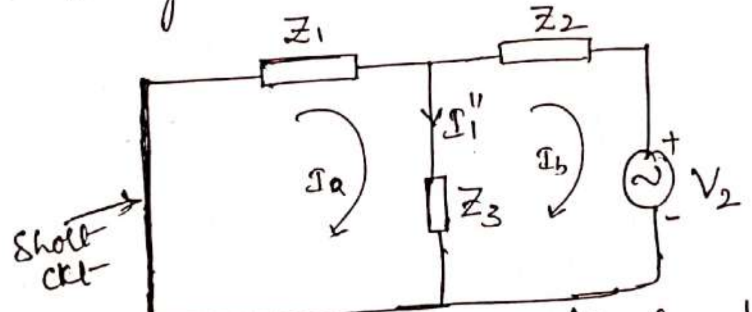
Case i) Consider the voltage source V_1 only, replacing the other V_2 by short circuit



Let I_1' is the current flowing through Z_3. Using ~~only~~ any one of the n/w reduction method find the current I_1'

$$I_1' = I_1 - I_2.$$

Case ii) Consider the voltage source V_2 only. Replacing the other vg source V_1 by short ckt. The resulting n/w is as shown.



Let I_1'' is the current flowing through Z_3. using any one of the n/w reduction method find the current I_1''

$$\Rightarrow I_1'' = I_a - I_b$$

According to superposition theorem, the total current I_1 through Z_3 is the algebraic sum of the current through Z_3 produced by V_1 & V_2 acting alone.

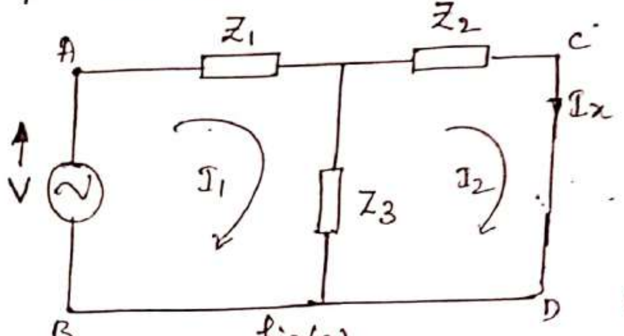
i.e., $\boxed{I_1 = I_1' + I_1''}$

hence the proof.

Reciprocity theorem :-

Statement: "For any linear, bilateral network containing only one independent source, the ratio of excitation to response remains same (constant) when their positions are interchanged."

Explanation:-



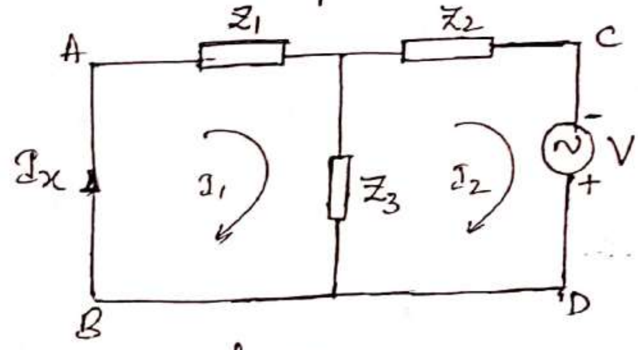
fig(a)

Consider a linear bilateral n/w as shown in fig(a). Let V volts is the excitation across AB & I_x is the response through CD, the ratio of excitation to response is $\frac{V}{I_x}$.

Now interchange the positions of excitation and response as shown in fig.(b)

If V volts is placed across CD, it produces the same current I_x through AB.

Then according to reciprocity theorem the ratio of excitation to response remains same.



fig(b)

Proof:- For first loop (fig(a))

$$(Z_1+Z_3)I_1 - Z_3 I_2 = V \quad \text{——— (1)}$$

For second loop (fig a)

$$-Z_3 I_1 + (Z_2+Z_3) I_2 = 0 \quad \text{——— (2)}$$

$$\therefore \Delta = \begin{bmatrix} Z_1+Z_3 & -Z_3 \\ -Z_3 & Z_2+Z_3 \end{bmatrix}$$

$$\Delta = (Z_1+Z_3)(Z_2+Z_3) - Z_3^2$$

$$\Delta = Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1$$

$$\Delta_2 = \begin{bmatrix} Z_1+Z_3 & V \\ -Z_3 & 0 \end{bmatrix}$$

$$\Delta_2 = V Z_3$$

from fig (a) $I_x = I_2 = \dfrac{\Delta_2}{\Delta}$

$$I_x = \frac{V Z_3}{Z_1 Z_3 + Z_2 Z_3 + Z_3 Z_1} \quad \text{—— (A)}$$

Now consider fig(b) :-

for 1st loop. $-Z_1 I_1 - Z_3(I_1 - I_2) = 0$

$$(Z_1+Z_3)I_1 - Z_3 I_2 = 0 \quad \text{—— (1)}$$

for second loop apply KVL,

$$-Z_2 I_2 + V - Z_3(I_2 - I_1) = 0$$

$$\cancel{(Z_2+Z_3)I} \; -Z_3 I_1 + (Z_2+Z_3)I_2 = V \quad \text{—— (2)}$$

$$\Delta = \begin{bmatrix} (Z_1+Z_3) & -Z_3 \\ -Z_3 & (Z_1+Z_3) \end{bmatrix}$$

$$\Delta = Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1$$

$$\Delta_1 = \begin{bmatrix} 0 & -Z_3 \\ V & Z_1+Z_3 \end{bmatrix}$$

$$\Delta_1 = Z_3 V$$

from fig (b)

$$I_1 = I_x = \frac{\Delta_1}{\Delta} = \frac{VZ_3}{Z_1Z_2 + Z_2Z_3 + Z_3Z_1} \quad \text{———} \quad (B)$$

from (A) & (B), reciprocity theorem is verified.

———— x ————

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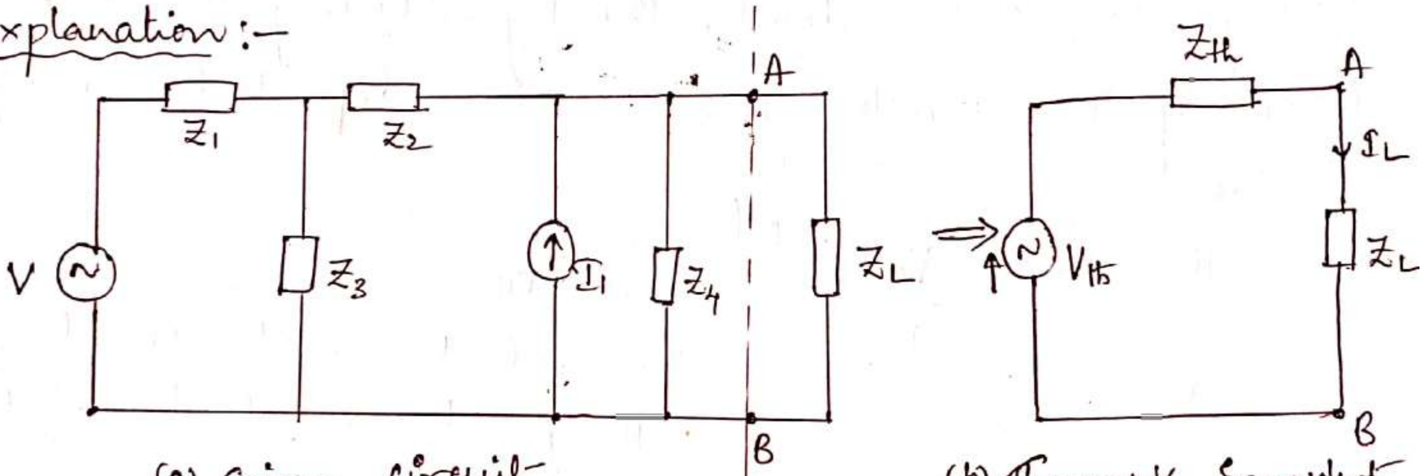
UNIT-4 Network Theorems - II

Thevenin's Theorem:-

Statement:- "In any linear bilateral complicated network connected to load may be replaced by a simple equivalent circuit consisting of a voltage source V_{th} in series with a resistor R_{th}, where V_{th} is the open-circuit voltage at the terminals and R_{th} is the input or equivalent resistance at the terminals when the independent sources are turned off or R_{th} is the ratio of open-circuit voltage to the short circuit current at the terminal pair."

Explanation:-



(a) given circuit (b) Thevenin's Equivalent circuit

Consider a linear bilateral complicated n/w is as shown in fig (a). According to Thevenin's theorem, the above complicated network can be reduced to a simple network as shown in fig (b).

The load current is calculated by,

$$\boxed{I_L = \frac{V_{th}}{Z_{th}+Z_L}}$$

Where, $V_{th} \rightarrow$ Thevenin's Equivalent voltage or open circuit voltage across the terminals A & B.

$Z_{th} \rightarrow$ Equivalent impedance b/n the terminals A & B.

$Z_L \rightarrow$ Load impedance.

Procedure :-

1) Remove the load impedance & create a open circuit across the load terminals A & B

2) Calculate open circuit voltage V_{th} across the load terminals

3) To find R_{th} :-

Case i) If the circuit contains only independent sources & resistors then deactivate the sources i.e, independent current srs are deactivated by opening them while independent voltage sources are deactivated by shorting them.

Case ii) If the circuit contains resistors, dependent & independent sources

then $R_{th} = \frac{V_{oc}}{i_{sc}}$ where,

$V_{oc} = V_{th}$

$i_{sc} \rightarrow$ Short circuit current flowing through the short terminal a-b.

Case iii) If the circuit contains resistors & only dependent sources

a) $V_{oc} = 0$ [Since there is no energy source]

b) Connect 1A current src to terminals a-b & determine V_{ab}

c) $R_{th} = \frac{V_{ab}}{1A}$.

4) After finding V_{th} & R_{th}, write the Thevenin's equivalent circuit.

*) Maximum Power transfer theorem :-

Statement :- "In any linear bilateral network, the maximum power is transferred from source to load when

i) Load resistance is equal to source resistance.

i.e, $\boxed{R_L = R_0}$

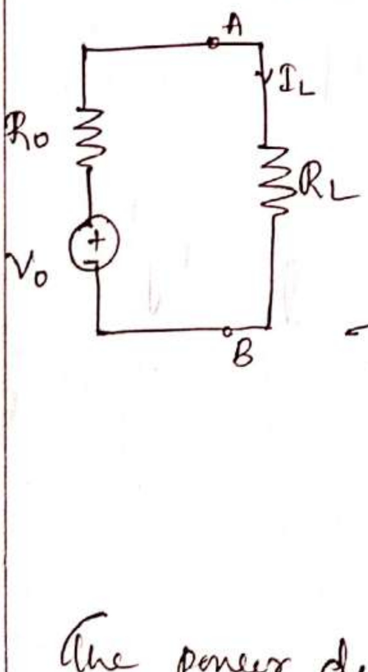
ii) Load resistance is equal to magnitude of source impedance

i.e, $\boxed{R_L = |Z_0|}$

iii) Load impedance is equal to complex conjugate of the source impedance.

i.e, $\boxed{Z_L = Z_0^*}$

Proof :- case i) when both source & load has resistance [DC circuits]



where, $V_0 \rightarrow$ Source voltage.

$R_0 \rightarrow$ Source resistance.

$R_L \rightarrow$ Load resistance.

The current flowing through the load is given by,

$$I_L = \frac{V_0}{R_0 + R_L} \quad \text{——— (1)}$$

The power delivered to the load is given by.

$$P = I_L^2 R_L \quad \text{——— (2)}$$

$$P = \frac{V_0^2}{(R_0+R_L)^2} \times R_L$$

Power delivered to the load is maximum when, $\frac{dP}{dR_L} = 0$

$$\frac{dP}{dR_L} = \frac{(R_0+R_L)^2 \times V_0^2 - V_0^2 R_L \times 2(R_0+R_L)}{[(R_0+R_L)^2]^2} = 0$$

$$\Rightarrow (R_0+R_L)^2 V_0^2 - V_0^2 R_L \times 2(R_0+R_L) = 0$$

$$\Rightarrow (R_0^2+R_L^2+2R_0R_L)V_0^2 - V_0^2[2R_0R_L+2R_L^2] = 0$$

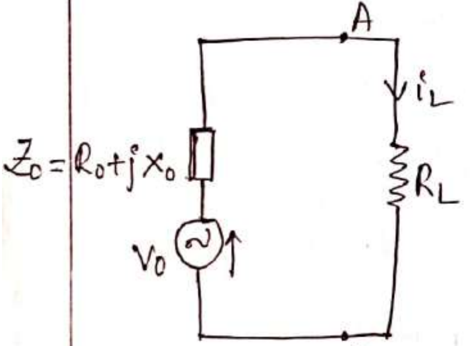
$$\Rightarrow (R_0^2+R_L^2+2R_0R_L)\cancel{V_0^2} = \cancel{V_0^2}(2R_0R_L+2R_L^2)$$

$$R_0^2+R_L^2 = 2R_L^2$$

$$R_0^2 = 2R_L^2 - R_L^2$$

$$\boxed{R_0 = R_L}$$

Case ii) When source has impedance and load has resistance.



where,

$V_0 \rightarrow$ Source voltage.

$Z_0 \rightarrow$ Source impedance.

$R_L \rightarrow$ load resistance.

The current flowing through load is given by,

$$I_L = \frac{V_0}{Z_0+R_L} = \frac{V_0}{R_0+jX_0+R_L}$$

$$I_L = \frac{V_0}{(R_0+R_L)+jX_0}$$

$$I_L = \frac{V_0}{\sqrt{(R_0+R_L)^2+X_0^2}} \quad \text{—— ①}$$

The power delivered to the load is given by

$$P = I_L^2 R_L \quad \text{—— ②}$$

$$\therefore P = \frac{V_0^2 R_L}{(R_0+R_L)^2+X_0^2}$$

The power transformed to the load is max. when

$$\frac{dP}{dR_L} = 0$$

$$\frac{dP}{dR_L} = \frac{[(R_0+R_L)^2+X_0^2]\times V_0^2 - V_0^2 R_L \times 2(R_0+R_L)}{[(R_0+R_L)^2+X_0^2]^2} = 0$$

$$\Rightarrow [(R_0+R_L)^2+X_0^2]\cancel{V_0^2} = 2\cancel{V_0^2}R_L(R_0+R_L)$$

$$\Rightarrow R_0^2+R_L^2+\cancel{2R_0R_L}+X_0^2 = \cancel{2R_LR_0}+2R_L^2$$

$$\Rightarrow R_0^2+X_0^2 = 2R_L^2-R_L^2$$

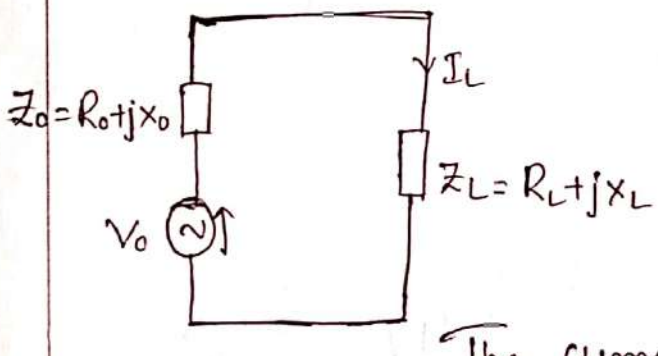
$$\Rightarrow R_0^2+X_0^2 = R_L^2$$

$$\therefore R_L = \sqrt{R_0^2+X_0^2}$$

$$R_L = R_0+jX_0 \quad \Rightarrow \boxed{R_L = |Z_0|}$$

Hence, the load resistance is equal to magnitude of src impedance is proved.

case iii) Both Source & load has impedances (AC circuits):-



where, $Z_0 \rightarrow$ Source impedance

$V_0 \rightarrow$ Src voltage.

$Z_L \rightarrow$ Load impedance.

The current flowing through the load is

$$I_L = \frac{V_0}{Z_0+Z_L} = \frac{V_0}{R_0+jX_0+R_L+jX_L}$$

$$I_L = \frac{V_0}{R_0+R_L+j(X_0+X_L)} = \frac{V_0}{\sqrt{(R_0+R_L)^2+(X_0+X_L)^2}} \quad \text{—①}$$

The power delivered to the load is,

$$P = I_L^2 Z_L$$

$$P = I_L^2 \times (R_L + \cancel{jX_L})$$ (Since power consumed in inductor is zero)

$$P = I_L^2 R_L \quad \text{——} ②$$

Substitute ① in ②, we get-

$$P = \left[\frac{V_0^2}{\sqrt{(R_0+R_L)^2+(X_0+X_L)^2}}\right]^2 \times R_L$$

$$P = \frac{V_0^2 R_L}{(R_0+R_L)^2+(X_0+X_L)^2}$$

Power delivered to the load is max when $\frac{dP}{dR_L} = 0$

$$\therefore \frac{dP}{dR_L} = \frac{[(R_0+R_L)^2+(X_0+X_L)^2]V_0^2 - V_0^2 R_L \times 2(R_0+R_L)}{[(R_0+R_L)^2+(X_0+X_L)^2]^2} = 0$$

$$\Rightarrow [(R_0+R_L)^2+(X_0+X_L)^2]\cancel{V_0^2} = 2\cancel{V_0^2} R_L(R_0+R_L)$$

$$\Rightarrow R_0^2+R_L^2+\cancel{2R_0R_L}+(X_0+X_L)^2 = \cancel{2R_LR_0}+2R_L^2$$

$$\Rightarrow R_0^2+(X_0+X_L)^2 = 2R_L^2-R_L^2$$

$$\Rightarrow R_0^2+(X_0+X_L)^2 = R_L^2$$

$$\therefore R_L = \sqrt{R_0^2+(X_0+X_L)^2}$$

$$R_L = R_0 + j(X_0+X_L)$$

$$R_L = R_0 + jX_0 + jX_L$$

$$R_L - jX_L = R_0 + jX_0$$

$$Z_L^* = Z_0$$

$$\left\{\begin{array}{l} x+jy = \sqrt{x^2+y^2} \\ Z_0 = R_0 + jX_0 \\ Z_L = R + jX_L \\ Z_L^* = R - jX_L \end{array}\right.$$

$$\therefore \boxed{Z_L = Z_0^*}$$

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Norton's Theorem :-

Statement :- "In any linear bilateral complicated n/w connected to load may be replaced by a simple network containing a current source & an impedance in parallel with it. The current source 'I_{sc}' is the short circuit current in load terminals & Z_{th} is the value of impedance looking from the load terminals replacing all the voltage sources by short circuit & all the current sources by open circuit."

Explanation :-

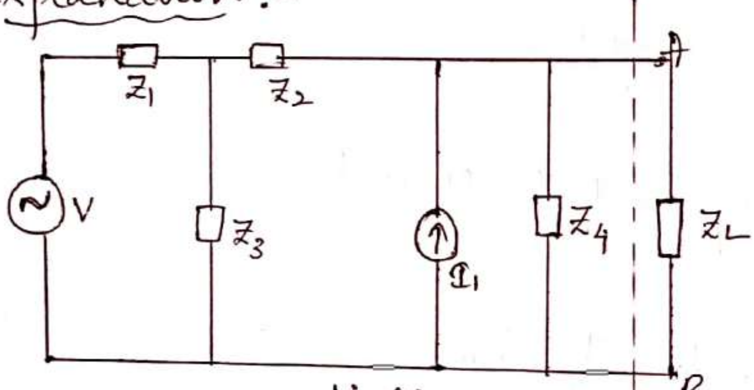
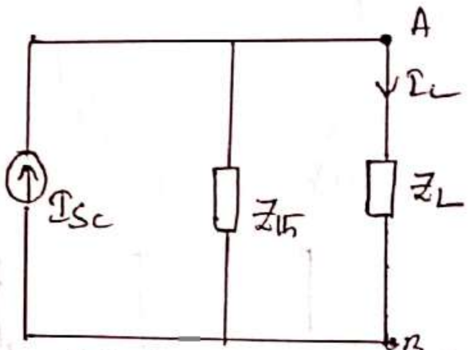


fig (1)



Norton's Equivalent circuit (fig 2)

Consider a linear bilateral n/w as shown in fig(1)

According to Norton's theorem. The above complicated network can be reduced into a simple n/w as shown in fig (2)

The load current is calculated by using

$$I_L = \frac{I_{sc} \times Z_{th}}{Z_{th} + Z_L}$$

Where $I_{sc} \rightarrow$ Short circuit current or Norton's current

$Z_{th} \rightarrow$ Norton's equivalent imp. &

$Z_L \rightarrow$ load impedances.

Procedure :- 1) Remove the load impedance & short circuit the load terminals A & B.

OC → open circuit   SC → Short circuit

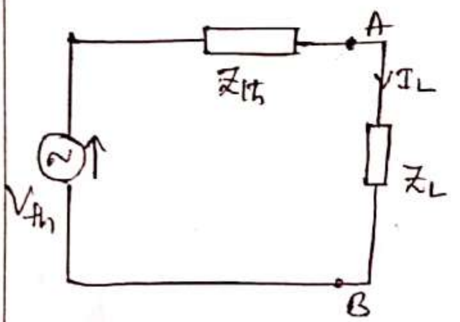
2) Calculate the short ckt current I_{sc} through the load terminal

3) Replace all the vtg sources by SC & all the current sources by OC.

4) Find the equivalent impedance Z_{th} (Z_N) as looking from the load terminals

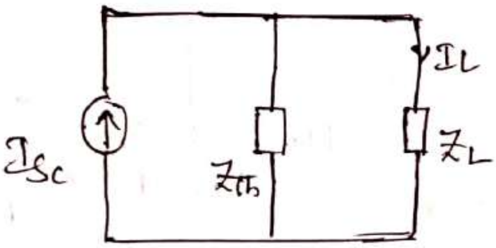
"Thevenin's equivalent is the dual of Norton's equivalent" Comment on the above statement

Soln Consider the Thevenin's equivalent circuit



$$I_L = \frac{V_{th}}{Z_{th} + Z_L} \quad \text{——— (1)}$$

Consider the Norton's equivalent circuit,



$$I_L = \frac{I_{sc}\, Z_{th}}{Z_{th} + Z_L} \quad \text{——— (2)}$$

from (1) & (2)

$$\frac{V_{th}}{Z_{th} + Z_L} = \frac{I_{sc}\, Z_{th}}{Z_{th} + Z_L}$$

$$\Rightarrow \boxed{V_{th} = I_{sc} \cdot Z_{th}} \quad \text{——— (3)}$$

$$\text{or} \quad \boxed{I_{sc} = \frac{V_{th}}{Z_{th}}} \quad \text{——— (4)}$$

where,
V_{th} → Thevenin's vtg
I_{sc} → Norton's current
Z_{th} → Thevenin's equivalent impedance

∴ Norton's equivalent circuit can be converted into thevenin's equivalent circuit using equation (3) & the Thevenin's equivalent circuit can be converted into Norton's equivalent circuit by using eqn (4).

Nortons theorem :

Statement :

Any Linear, bilateral Complicated N/w. Connected to a load impedance Can be replaced by a Simple equivalent CKt Containing a Current Source of Current I_{SC} in parallel with impedance Zth.

Where, I_{SC} → Short CKt Current in the Load terminals.

Zth → Equivalent impedance of the N/w as looking from the load terminals, replacing all the voltage Sources by Short CKt & all Current Sources by open CKt.

Explanation :

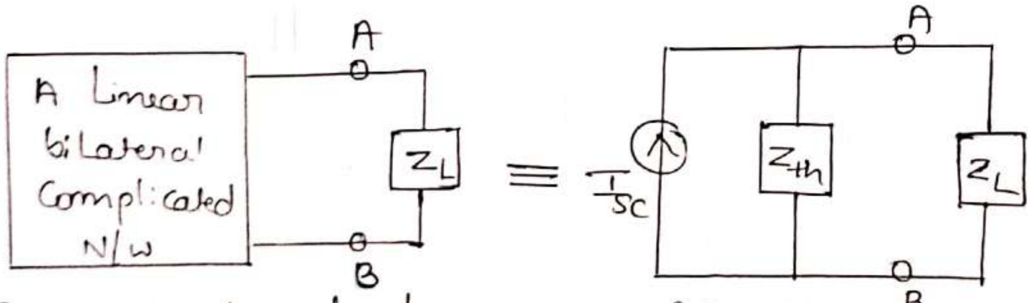


Fig (a) Complicated N/w   Fig(b). ~~Thevenins~~ Norton's N/w.

Consider a linear, bilateral, Complicated N/w as shown in fig (a). According to ~~thevenins~~ Norton's theorem the Complicated N/w reduced to a Simple as shown in fig (b).

The load Current is $I_L = \frac{I_{SC} \times Z_{th}}{Z_{th} + Z_L}$

where, $I_{SC} \rightarrow$ Short ckt current or Nortons current.

$Z_{th} \rightarrow$ Equivalent impedance b/w A & B

$Z_L \rightarrow$ Load impedance.

Procedure :-

1) Remove the Load impedance & short the load terminals A & B.

2) Calculate the short ckt current $[I_{SC}]$ through the load terminals.

3) Replace all the independent voltage sources by short ckt & all the independent current sources by open ckt.

4) Find the equivalent impedance b/w A & B.

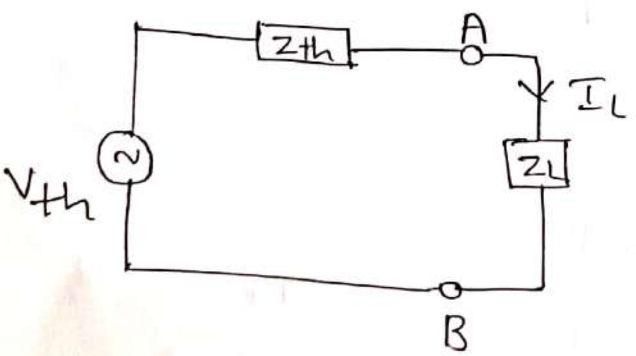
5) Write the Nortons equivalent ckt.

6) Calculate the load current $I_L = \frac{I_{SC} \times Z_{th}}{Z_{th} + Z_L}$

Jan SMK

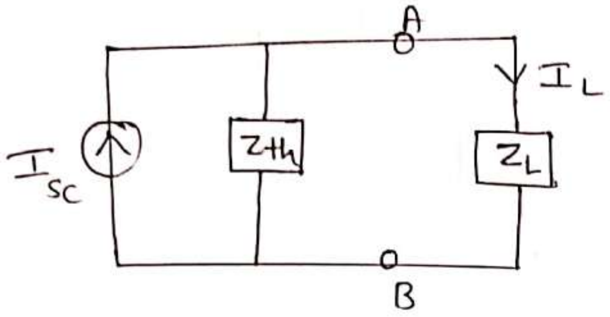
* "Thevenins equivalent is the dual of Nortons equivalent". Comment on the above statement & substantiate the same.

Thevenin's equivalent ckt is



$$I_L = \frac{V_{th}}{Z_{th} + Z_L} \longrightarrow (1)$$

Nortons equivalent ckt is



$$I_L = \frac{I_{SC} \times Z_{th}}{Z_{th} + Z_L} \longrightarrow (2)$$

From (1) & (2)

$$\frac{V_{th}}{Z_{th} + Z_L} = \frac{I_{SC} \cdot Z_{th}}{Z_{th} + Z_L}$$

$$V_{th} = I_{SC} \cdot Z_{th} \quad \text{——— (3)}$$

$$I_{SC} = \frac{V_{th}}{Z_{th}} \quad \text{——— (4)}$$

Where $V_{th} \longrightarrow$ Thevenins Voltage

$I_{SC} \longrightarrow$ Nortons Current

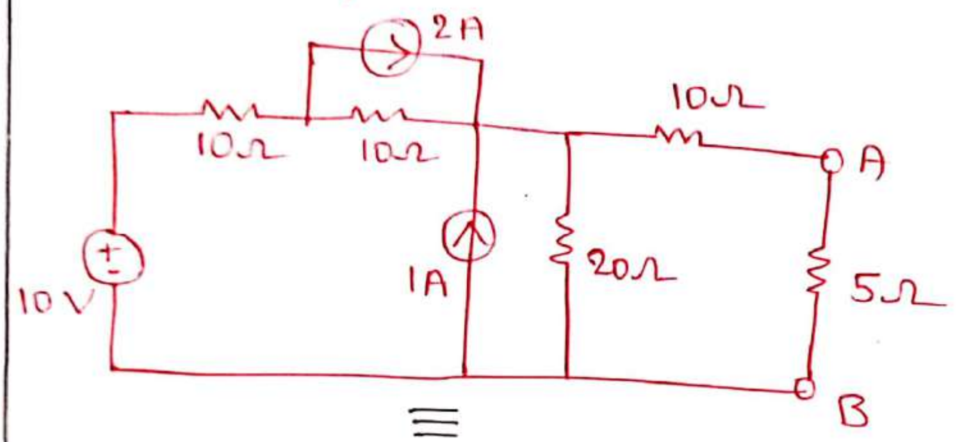
$Z_{th} \longrightarrow$ Equivalent impedance

* Nortons equivalent ckt can be converted into thevenins equivalent ckt by eqn (3)

* Thevenins equivalent ckt can be converted into Nortons equivalent ckt by eqn (4)

Problems :

1) Draw the thevenins equivalent N/W & Nortons equivalent N/W for the N/W shown & also find current flowing through 5 Ω resistor connected b/w A & B.



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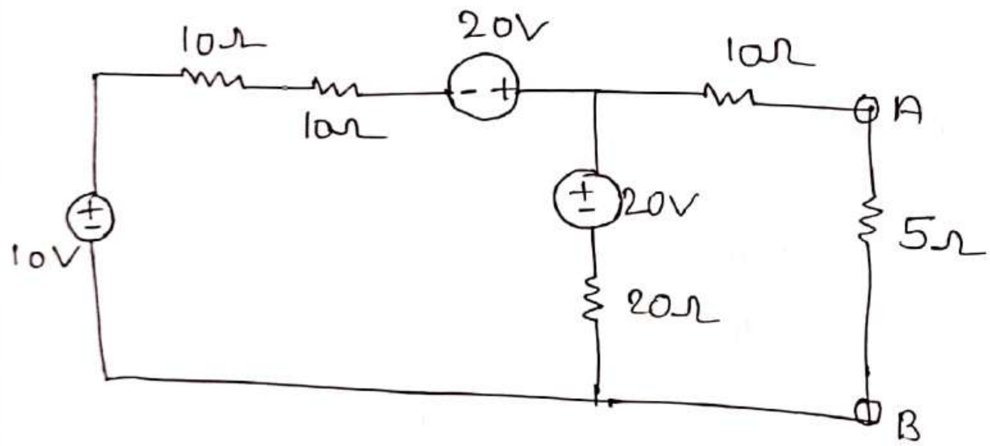
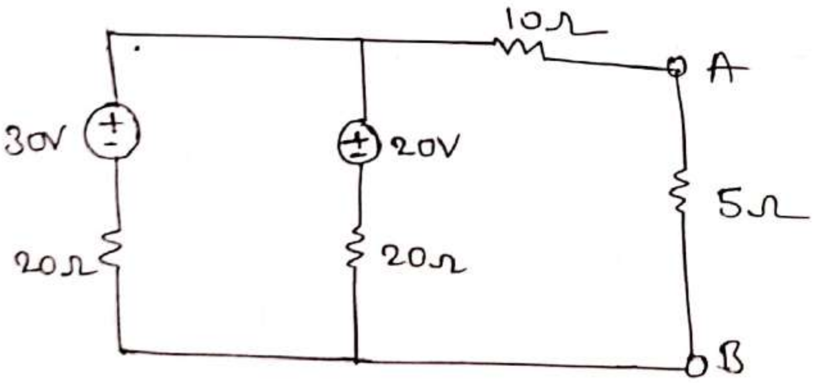
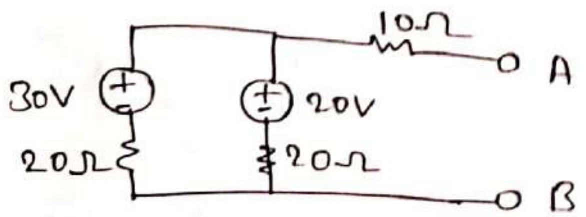
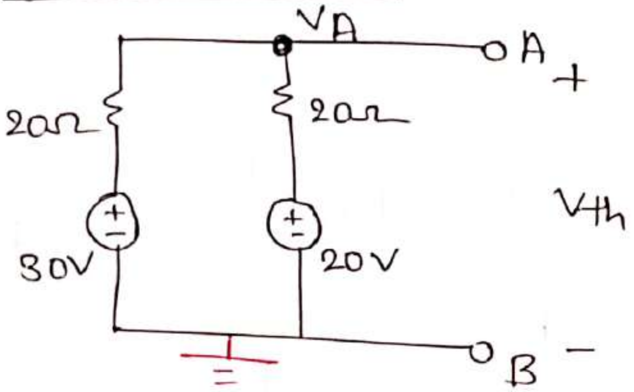




Remove the Load & create open CKt b/w A & B



To find Vth :



Apply KCL at node V_A

$$\frac{V_A - 30}{20} + \frac{V_A - 20}{20} = 0$$

$$V_A - 30 + V_A - 20 = 0$$

$$2V_A - 50 = 0$$

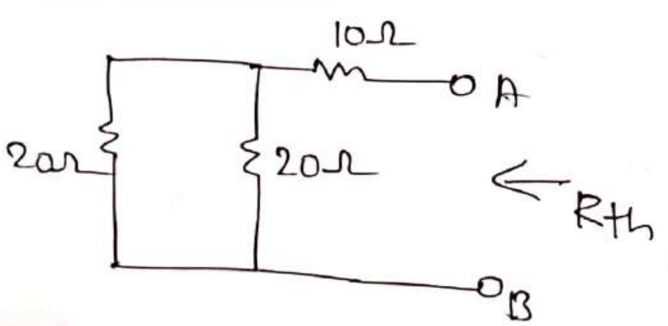
$$V_A = \frac{50}{2} = 25\,V$$

$$\therefore V_{th} = V_{AB} = V_A - V_B$$

$$= 25 - 0$$

$$= \underline{\underline{25\,V}}$$

To find Rth :

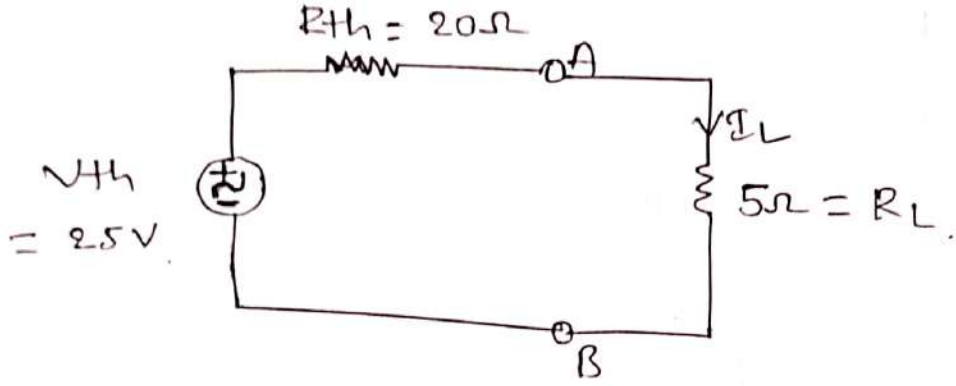


$$R_{th} = (20 \parallel 20) + 10$$

$$= 10 + 10$$

$$= 20\,\Omega$$

Thevenins equivalent N/w :-



$$I_L = \frac{V_{th}}{R_{th} + R_L}$$

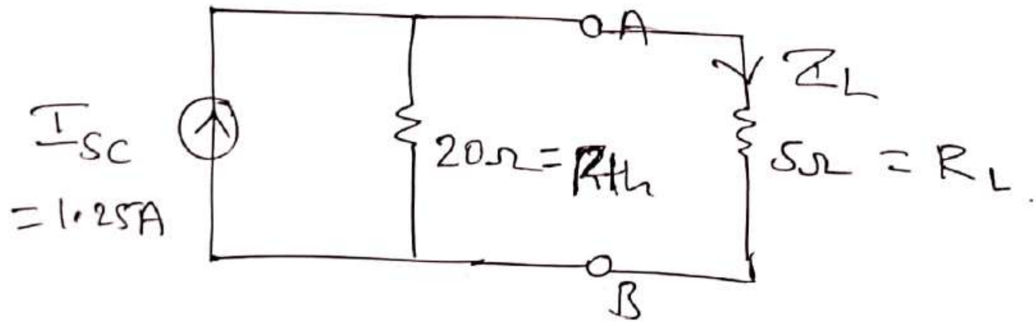
$$I_L = \frac{25}{20+5}$$

$$\boxed{I_L = 1A}$$

Nortons equivalent N/w :-

W.K.T

$$I_{SC} = \frac{V_{th}}{Z_{th}} = \frac{25}{20} = 1.25\,A.$$

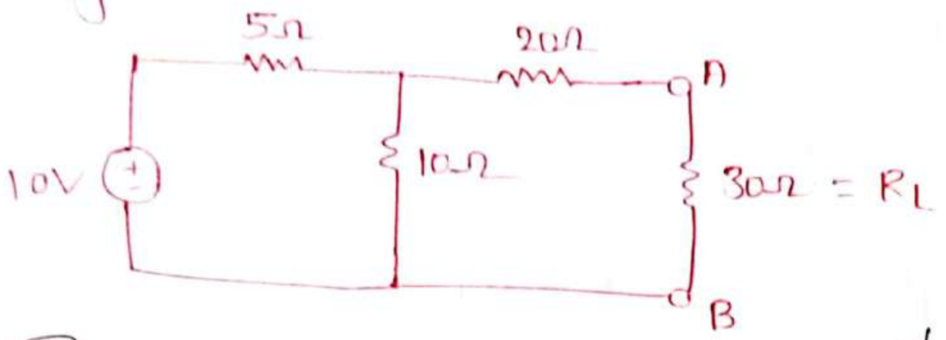


$$I_L = \frac{I_{SC}\,R_{th}}{R_{th} + R_L}$$

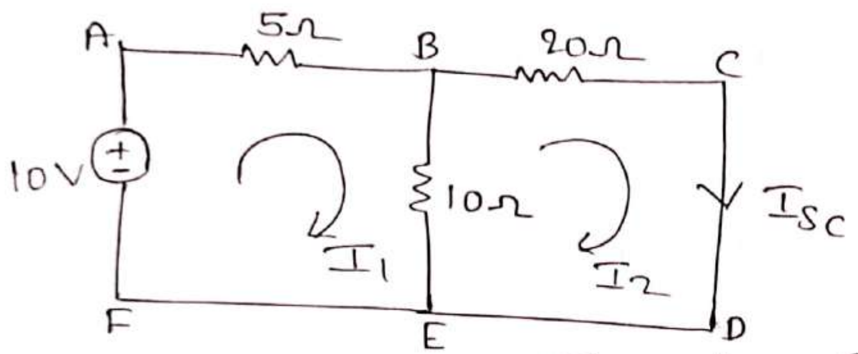
$$= \frac{1.25 \times 20}{20 + 5}$$

$$\boxed{I_L = 1A}$$

2) Find the Current through 30Ω load resistor using Nortons theorem.



Remove the load & Creat the short ckt.



From the ckt

$\therefore I_{SC} = ?$

$I_{SC} = I_2$

KVL to the 1st Loop :

$$10 - 5I_1 - 10[I_1 - I_2] = 0$$

$$10 - 5I_1 - 10I_1 + 10I_2 = 0$$

$$-15I_1 + 10I_2 = -10 \longrightarrow (1)$$

KVL to the 2nd Loop :

$$-20I_2 - 10[I_2 - I_1] = 0$$

$$-20I_2 - 10I_2 + 10I_1 = 0$$

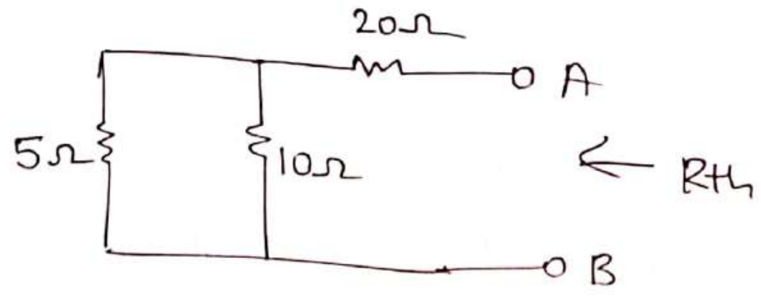
$$10I_1 - 40I_2 = 0 \longrightarrow (2)$$

Solving (1) & (2)

$I_1 = 0.857A \qquad I_2 = 0.2857A$

$\therefore \quad I_{SC} = I_2 = 0.2857A$

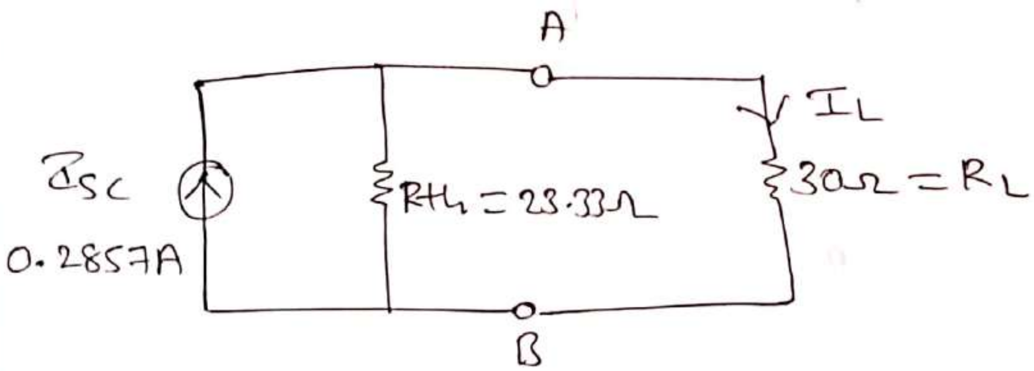
To find Rth :



$$R_{th} = (5 \parallel 10) + 20$$

$$= 23.33\ \Omega$$

Nortons equivalent N/W :-

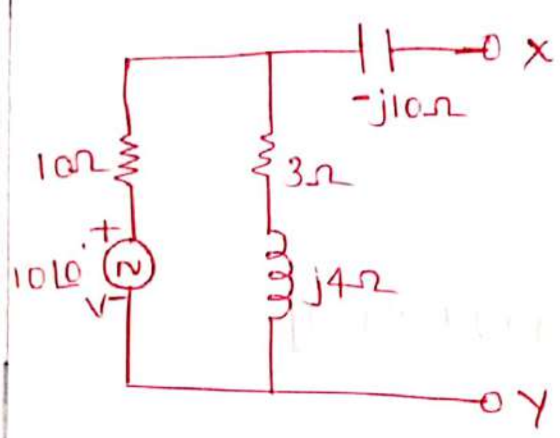


$$I_L = \frac{I_{SC} \times R_{th}}{R_{th} + R_L}$$

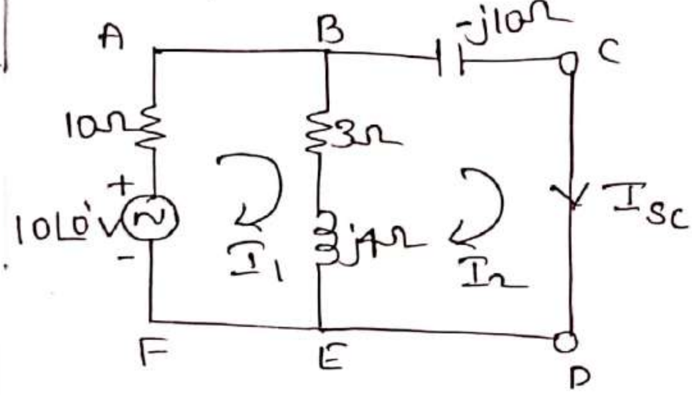
$$= \frac{0.2857 \times 23.33}{23.33 + 30}$$

$$I_L = 0.125\ A$$

3. obtain the Nortons equivalent ckt for the N/w shown



To find I_{sc} :



$$I_{sc} = I_2$$

Apply KVL to the 1st Loop

$$10\angle 0 - 10I_1 - 3[I_1 - I_2] - j4[I_1 - I_2] = 0$$

$$10\angle 0 - 10I_1 - 3I_1 + 3I_2 - j4I_1 + j4I_2 = 0$$

$$-13I_1 - j4I_1 + 3I_2 + j4I_2 = -10\angle 0$$

$$(-13 - j4)I_1 + (3 + j4)I_2 = -10\angle 0 \rightarrow (1)$$

Apply KVL to the 2nd Loop..

$$+j10\Omega I_2 - (3 + j4)(I_2 - I_1) = 0$$

$$j10\Omega I_2 - (3 + j4)I_2 + (3 + j4)I_1 = 0$$

$$(3 + j4)I_1 + (-3 + j6)I_2 = 0 \rightarrow (2)$$

$$\Delta = \begin{vmatrix} -13-j4 & 3+j4 \\ 3+j4 & -3+j6 \end{vmatrix}$$

$$= \left[(-13-j4)(-3+j6) - (3+j4)(3+j4)\right]$$

$$= 70 - 90j$$

$$\Delta_2 = \begin{vmatrix} -13-j4 & -10\angle 0 \\ 3+j4 & 0 \end{vmatrix}$$

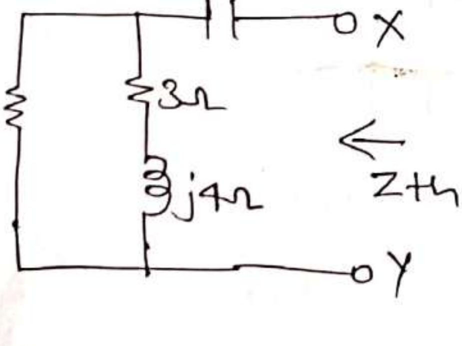
$$= +(3+j4)(10\angle 0)$$

$$= 30 + 40j$$

$$\therefore I_{SC} = I_2 = \frac{\Delta_2}{\Delta} = \frac{30+40j}{70-90j} = -0.115 + 0.42j$$

$$= 0.439\angle 105.3^\circ \text{ A}$$

<u>To find Z_{th}:</u>

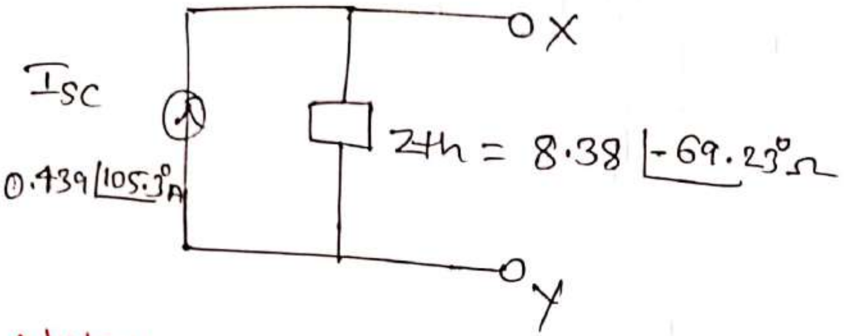


$$Z_{th} = \frac{10 * (3+j4)}{10+3+j4} - j10$$

$$= 2.97 - 7.84j$$

$$= 8.38\angle -69.23^\circ \ \Omega$$

Nortons equivalent N/w:



Note: If the given N/w Consists of some dependent source, then there dependent source must be kept as it is while Calculating Z_{th} & should not be shorted or open ckted wether it is Voltage or Current source.

In such cases, Z_{th} is given by

$$Z_{th} = \frac{V_{th}}{I_{SC}}$$

Where $I_{SC} \rightarrow$ Nortons Current

$V_{th} \rightarrow$ thevenins voltage.

Jan 08
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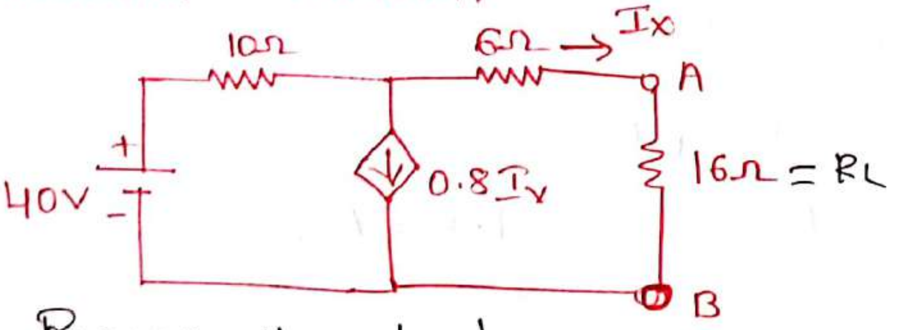
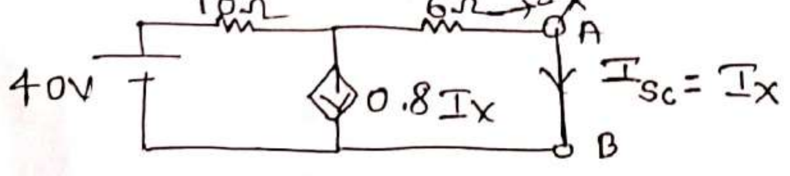
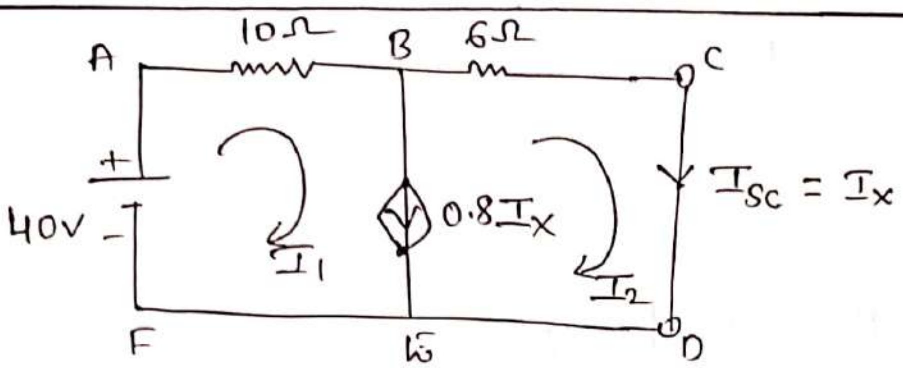
4) Find the Current through 16 Ω resistor using Nortons theorem.



Remove the Load





$$I_{SC} = I_x = I_2$$

$0.8 I_x$ is in b/w two meshes ∴ it forms supermesh ABCDEFA.

$$I_1 - I_2 = 0.8\ I_x$$

$$I_1 - I_2 = 0.8\ I_2$$

$$I_1 - I_2 - 0.8 I_2 = 0$$

$$I_1 - 1.8 I_2 = 0 \longrightarrow (1)$$

Apply KVL to the supermesh

$$-10I_1 - 6I_2 + 40 = 0$$

$$-10I_1 - 6I_2 = -40 \longrightarrow (2)$$

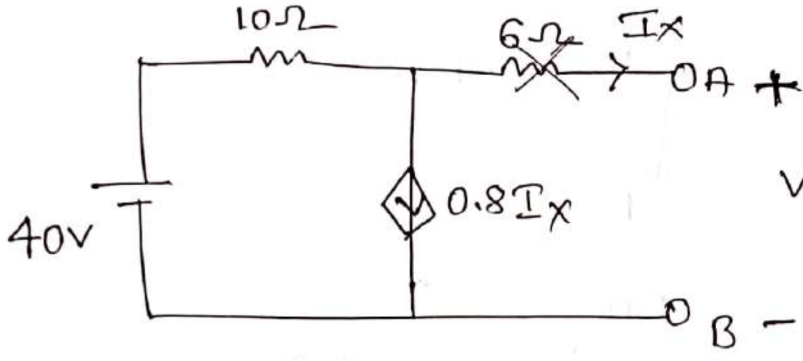
Solving (1) & (2)

$I_1 = 3A \qquad I_2 = 1.67\ A.$

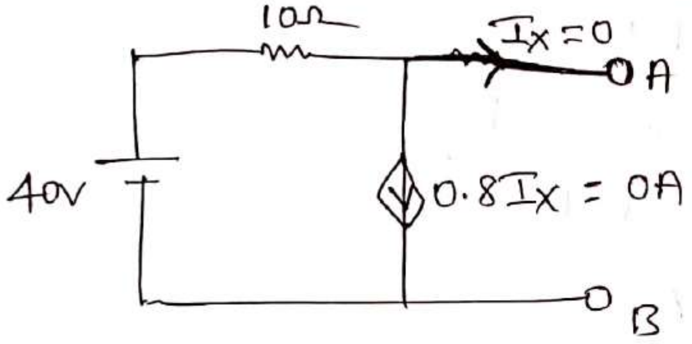
$$\therefore\ I_{SC} = I_2 = 1.67A.$$

To find Zth :

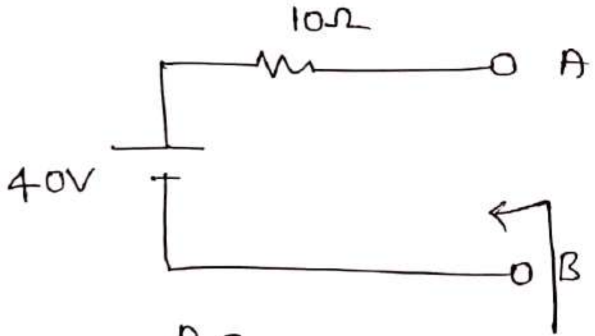
Creat open CKt b/w A & B



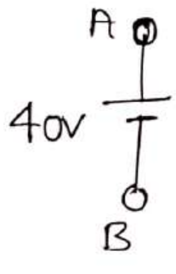
$V_{th} = V_{oc}$



No current flows through 6Ω



No current flows through 10Ω

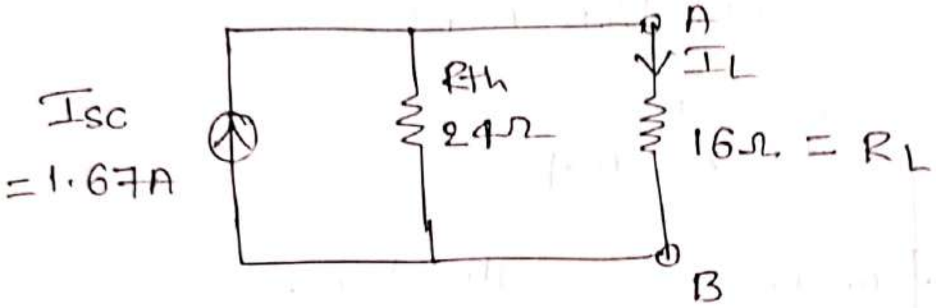


$\therefore V_{th} = V_{AB} = 40V$

$$\therefore Z_{th} = \frac{V_{th}}{I_{sc}}$$

$$= \frac{40}{1.67} = 24\Omega = R_{th}$$

∴ Nortons Equivalent CKt



$$\therefore \quad I_L = \frac{I_{sc} \times R_{th}}{R_{th} + R_L}$$

$$= \frac{1.67 \times 24}{24 + 16}$$

$$\underline{I_L = 1\ A}.$$

Maximum power transfer theorem :

Statement :

In any linear bilateral N/w, the Maximum power is transferred from source to load when

1) Load resistance = Source resistance ie $R_L = R_S$

2) Load resistance = Magnitude of source impedance

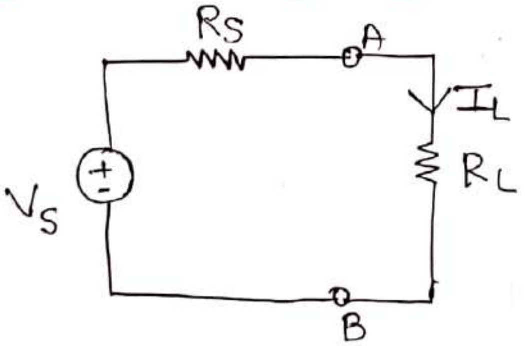
ie $R_L = |Z_S|$

3) Load impedance = Complex Conjugate of Source impedance

ie $Z_L = Z_S^*$

Proof :

Case (1) : P.T $R_L = R_S$



$V_S \rightarrow$ Source Voltage

$R_S \rightarrow$ Source resistance

$R_L \rightarrow$ load resistance

The power delivered to the load is

$$P = I_L^2 R_L \longrightarrow (1)$$

But $$I_L = \frac{V_S}{R_S + R_L} \longrightarrow (2)$$

Substitute (2) in (1)

$$P = \frac{V_S^2}{(R_S + R_L)^2} \cdot R_L \longrightarrow (3)$$

The power delivered to the load is maximum when $\frac{dp}{dR_L} = 0 \rightarrow$ Maxima theorem.

$$\frac{dp}{dR_L} = 0$$

$$\frac{d}{dR_L}\left[\frac{V_S^2}{(R_S+R_L)^2} R_L\right] = 0$$

$$\frac{(R_S+R_L)^2 V_S^2 - V_S^2 R_L \, 2[R_S+R_L]}{(R_S+R_L)^4} = 0$$

$$(R_S+R_L)^2 V_S^2 - 2V_S^2 R_S R_L - 2V_S^2 R_L^2 = 0$$

$$(2R_S R_L + R_S^2 + R_L^2) V_S^2 - 2V_S^2 R_S R_L - 2V_S^2 R_L^2 = 0$$

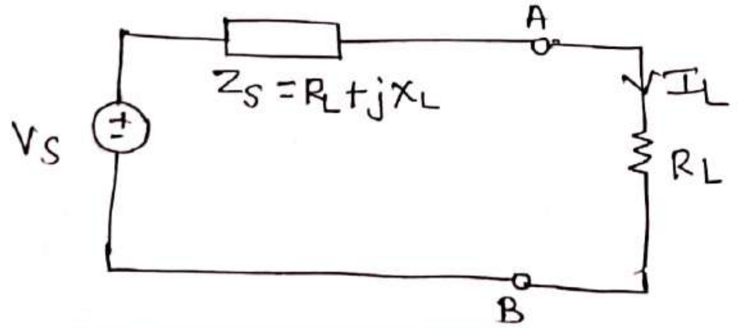
$$\cancel{2R_S R_L V_S^2} + R_S^2 V_S^2 + R_L^2 V_S^2 - \cancel{2V_S^2 R_S R_L} - 2V_S^2 R_L^2 = 0$$

$$R_S^2 V_S^2 - R_L^2 V_S^2 = 0$$

$$R_S^2 \cancel{V_S^2} = R_L^2 \cancel{V_S^2}$$

$$\therefore \boxed{R_L = R_S}$$

Case (2) : P.T $R_L = |Z_g|$



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The power delivered to the load is

$$P = I_L^2 R_L \longrightarrow (1)$$

The load current is given by

$$I_L = \frac{V_S}{Z_S + R_L}$$

$$= \frac{V_S}{R_S + jX_S + R_L}$$

$$= \frac{V_S}{(R_S + R_L) + jX_S}$$

$$I_L = \frac{V_S}{\sqrt{(R_S+R_L)^2 + X_S^2}} \longrightarrow (2)$$

Substitute (2) in (1)

$$P = \frac{V_S^2 R_L}{(R_S+R_L)^2 + X_S^2}$$

The power delivered to the load is Maximum

When

$$\frac{dP}{dR_L} = 0 \longrightarrow \text{Maxima theorem}$$

$$\frac{d}{dR_L}\left[\frac{V_S^2 R_L}{(R_S+R_L)^2 + X_S^2}\right] = 0$$

$$\frac{\left[(R_S+R_L)^2 + X_S^2\right] V_S^2 - V_S^2 R_L\, 2\left[R_S + R_L\right]}{\left[(R_S+R_L)^2 + X_S^2\right]^2} = 0$$

$$(R_S + R_L)^2 + X_S^2 - 2R_L(R_S + R_L) = 0$$

$$R_S^2 + R_L^2 + \cancel{2R_S R_L} + X_S^2 - \cancel{2R_S R_L} - 2R_L^2 = 0$$

$$R_S^2 + X_S^2 - R_L^2 = 0$$

$$R_L^2 = R_S^2 + X_S^2$$

$$R_L = \sqrt{R_S^2 + X_S^2}$$

$$R_L = |Z_S|$$

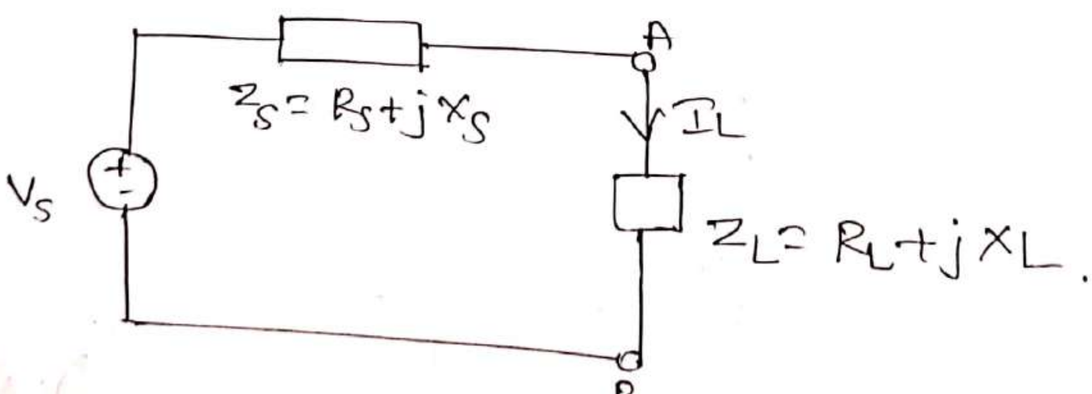
Case 3 : P.T $Z_L = Z_S^*$

or

State & prove maximum power transfer theorem for AC ckt.

or

P.T an alternating voltage source transfer maximum power to the load when the load impedance is equal to complex conjugate of the source impedance.



The power delivered to the load is

$$P = I_L^2 Z_L$$

$$P = I_L^2 \left[R_L + jX_L\right]$$

Power Consumed by the inductor or Capacor is zero

$$\therefore \quad P = I_L^2 R_L \longrightarrow (1)$$

The load current is given by

$$I_L = \frac{V_S}{Z_S + Z_L}$$

$$= \frac{V_S}{(R_S + jX_S) + (R_L + jX_L)}$$

$$= \frac{V_S}{(R_S + R_L) + j(X_S + X_L)}$$

$$I_L = \frac{V_S}{\sqrt{(R_S + R_L)^2 + (X_S + X_L)^2}} \longrightarrow (2)$$

(2) in (1)

$$P = \frac{V_S^2 R_L}{(R_S + R_L)^2 + (X_S + X_L)^2}$$

The power delivered to the load is maximum when $\frac{dP}{dR_L} = 0$.

$$\frac{d}{dR_L}\left[\frac{V_S^2 R_L}{(R_S+R_L)^2+(X_S+X_L)^2}\right] = 0$$

$$\frac{\left[(R_S+R_L)^2+(X_S+X_L)^2\right]V_S^2 - V_S^2 R_L\, 2(R_S+R_L)}{\left[(R_S+R_L)^2+(X_S+X_L)^2\right]^2} = 0$$

$$(R_S+R_L)^2+(X_S+X_L)^2 - 2R_L(R_S+R_L) = 0$$

$$R_S^2+R_L^2+\cancel{2R_SR_L}+X_S^2+X_L^2+2X_SX_L-\cancel{2R_LR_S}-2R_L^2=0$$

$$R_S^2+R_L^2+(X_S+X_L)^2-2R_L^2=0$$

$$R_S^2+(X_S+X_L)^2-R_L^2=0$$

$$R_L^2 = R_S^2+(X_S+X_L)^2$$

$$R_L = \sqrt{R_S^2+(X_S+X_L)^2}$$

$$R_L = R_S + j(X_S+X_L)$$

$$R_L = R_S + jX_S + jX_L$$

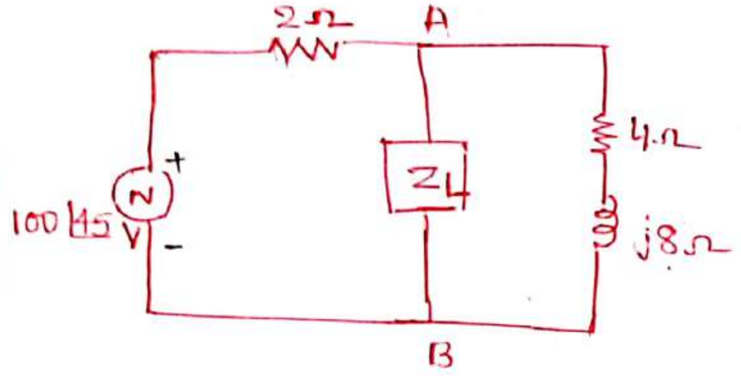
$$R_L - jX_L = R_S + jX_S$$

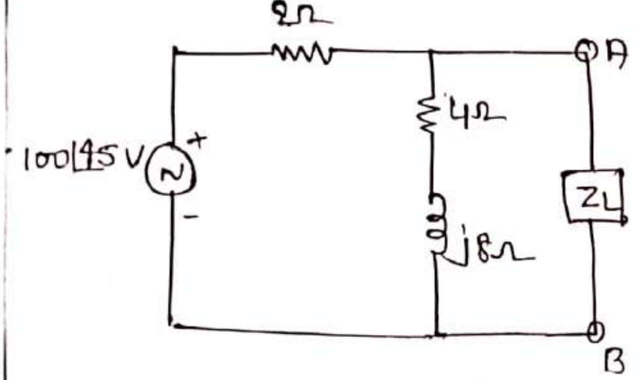
$$Z_L^* = Z_S$$

or $\boxed{Z_L = Z_S^*}$

Solved Problems :-

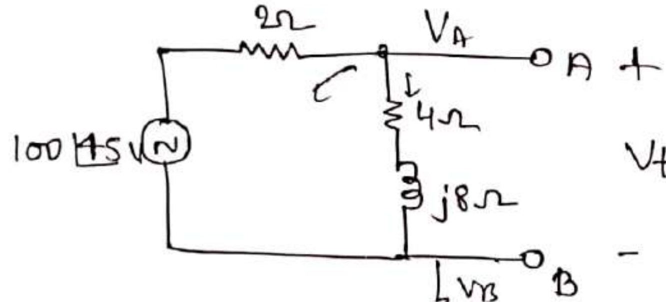
1) The N/W shown in figure determine Z_L for which power transfer is Maximum. Calculate the maximum power transferred to the Load.





Remove the load

$V_{th} = V_A - V_B$ and $\boxed{V_B = 0}$



KCL

$$\frac{V_A - 100\angle 45^\circ}{2} + \frac{V_A}{(4+j8)} = 0$$

$$0.5V_A - 50\angle 45^\circ + \frac{V_A}{8.94\angle 63.43} = 0$$

$$0.5V_A - 50\angle 45^\circ + 0.1118\angle -63.43\, V_A = 0$$

$$\cancel{V_{th} = \frac{100\angle 45 \times (4+j8)}{2+4+j8}}$$

$$\cancel{V_{th} = 89.44\angle 55.3 \text{ V}}$$

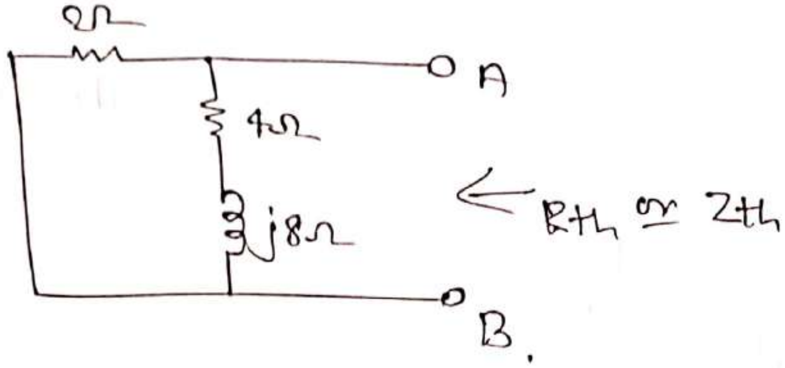
$\rightarrow 0.5V_A + 0.05V_A - j0.099V_A = 50\angle 45^\circ$

$(0.55 - j0.099)V_A = 50\angle 45^\circ$

$$V_A = \frac{50\angle 45^\circ}{0.558\angle -10.2^\circ}$$

$$\boxed{V_A = 89.4\angle 55.3^\circ \text{ volts}}$$

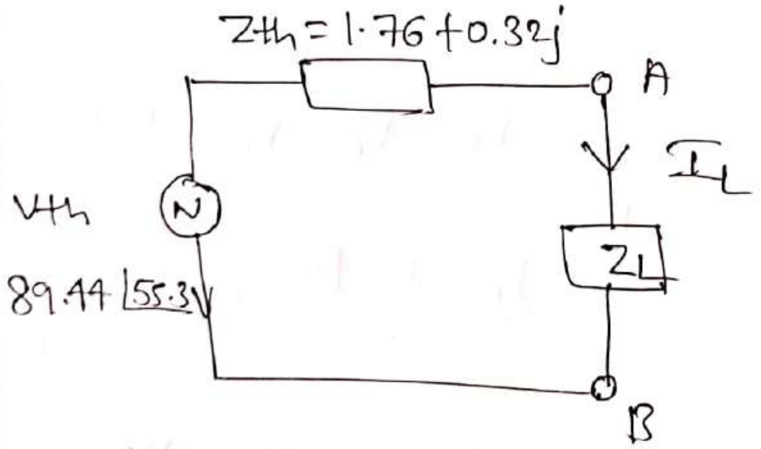
To find Zth :-



$$Z_{th} = \frac{2 \times (4 + j8)}{2 + 4 + j8}$$

$$Z_{th} = 1.76 + 0.32j$$

Thevenins equivalent N/w.



The power is maximum.

when $Z_L = Z_S^*$

$$Z_L = Z_{th}^*$$

$$Z_L = 1.76 - 0.32j \ \Omega$$

$$\therefore I_L = \frac{V_{th}}{Z_{th} + Z_L} = \frac{89.44 \angle 55.3}{1.76 + \cancel{0.32j} + 1.76 - \cancel{0.32j}}$$

$I_L = 25.41 \angle 55.3$ A

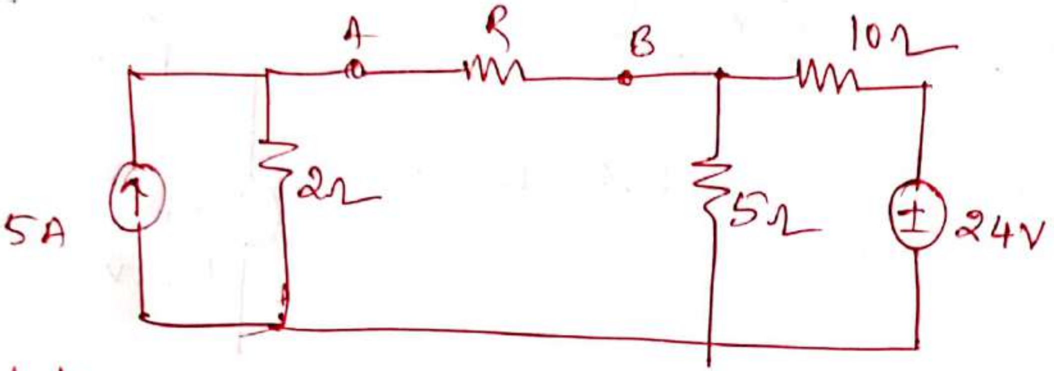
$\therefore$ Maximum power delivered is

$P = I_L^2 \times R_L$

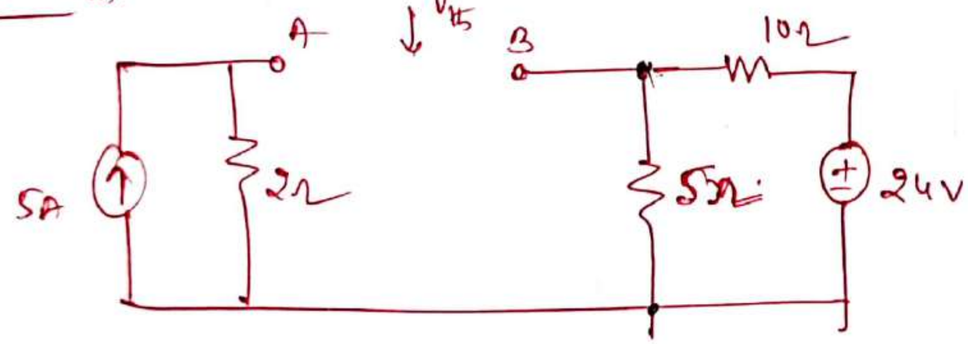
$= 25.41 \angle 55.3 \times 1.76$

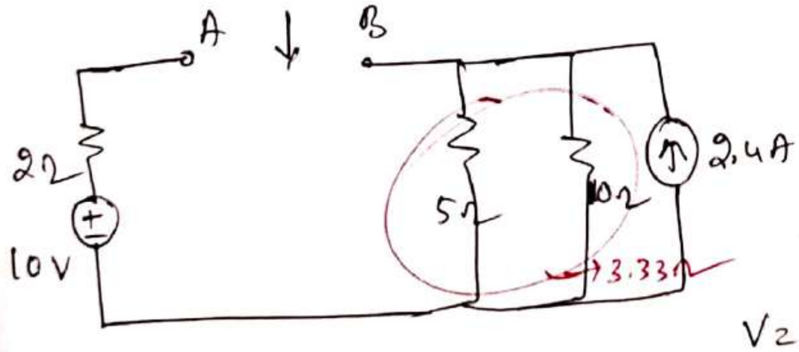
$P = \underline{1.136 \text{ KW}}$

2) What should be the value of R such that max power transfer can take place from the rest of the n/w to R. Obtain the amount of this power.



To find V_{th}:-

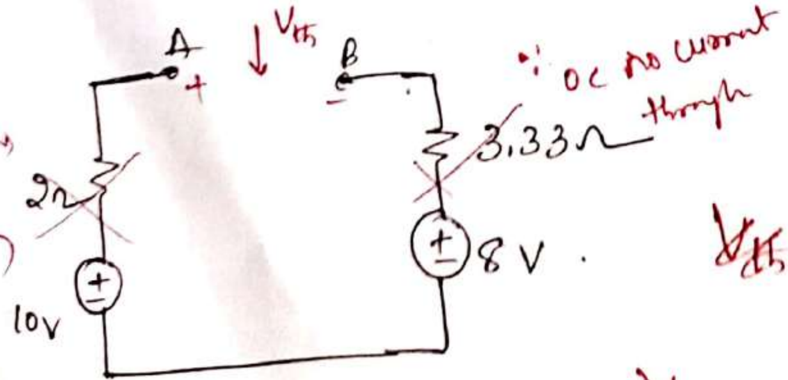




$$\frac{10 \times 5}{10+5} = \frac{50}{15}$$

$V = 2.4 \times 3.33$

OS (current zero)

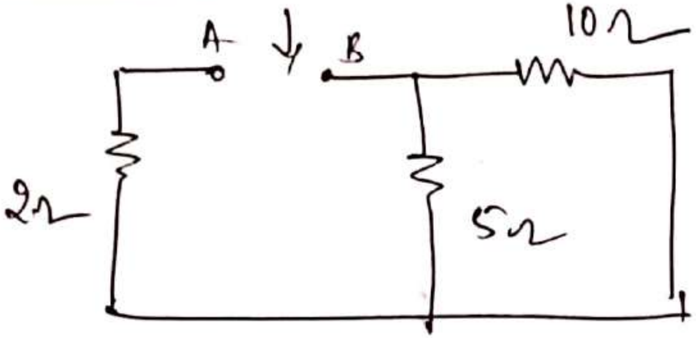


∵ OC no current through

$$V_{th} - 10 + 8 = 0$$

$$\boxed{V_{th} = 2V}$$

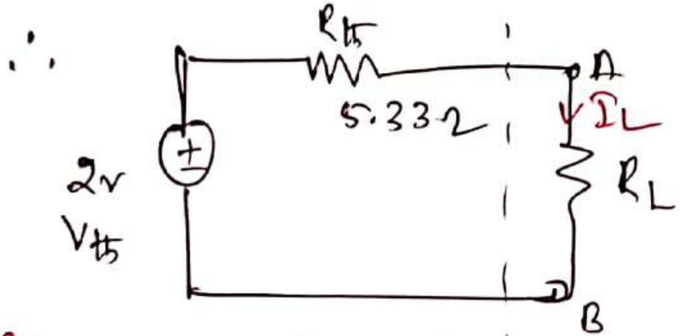
To find R_{th} :



$$R_{th} = 2 + \frac{(10 \times 5)}{10+5}$$

$$\boxed{R_{th} = 5.33\,\Omega}$$

∴



Th Equivalent ckt

Conditions for Max power transfer theorem.

$R_S = R_L$

(Here R_{th} is R_S, V_{th} is V_S)

$\therefore$ $R_L = 5.33\,\Omega$

$$I_L = \frac{V_{th}}{R_{th}+R_L} = \frac{2}{5.33+5.33}$$

$$\boxed{I_L = 0.188\,A}$$

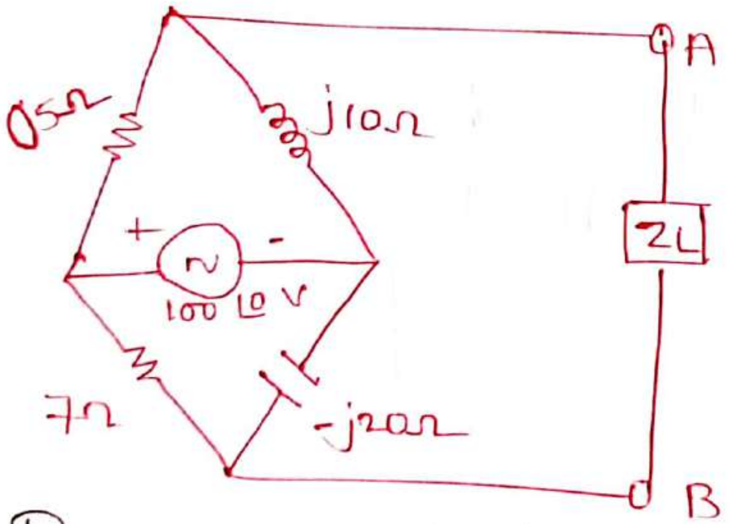
$\therefore$ $P = I_L^2 \times R.$

$P = (0.188)^2 \times 5.33$

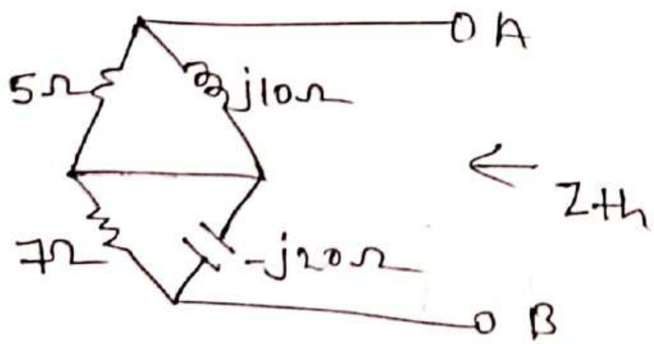
$P = 0.188$ Watts.

Jan 6 Mks

3) Find the value of Z_L for which maximum power is transferred to the load Z_L from the N/w in the below fig.



Remove the load & create open ckt b/w A & B & find out Zth.



$$Z_{th} = \left(\frac{5 \times j10}{5 + j10}\right) + \left(\frac{7 \times -j20}{7 - j20}\right)$$

$$Z_{th} = 10.24 - 0.183j \, \Omega = Z_S$$

Power is maximum.

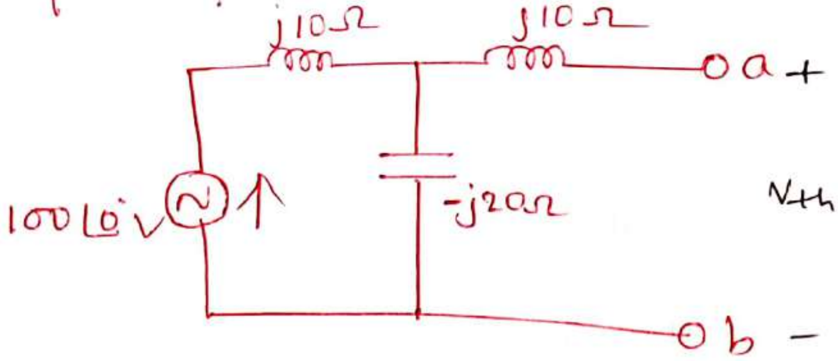
when $Z_L = Z_S^*$

$$Z_L = 10.24 + 0.183j \, \Omega$$

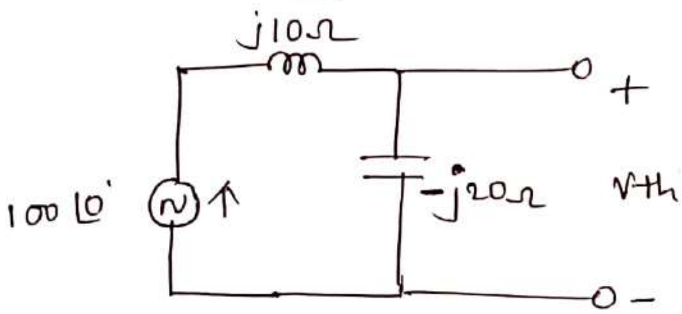
Ref 12/...

March 00
Jan 07 } 10MKS
Jan 10

4) What should be the value of a pure resistance to be connected across the terminals a & b in the ckt of below fig. so that maximum power is transferred to the Load. What is the Max power?



To find Vth:



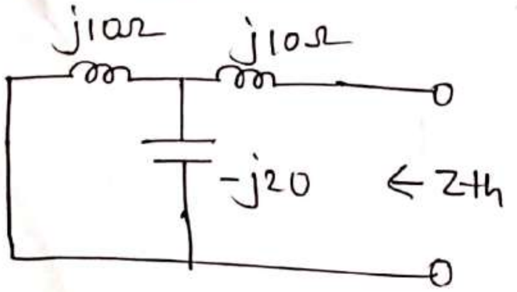
No current flows through j10Ω

$$\therefore V_{th} = \frac{100\angle 0^\circ \times (-j20)}{j10 - j20}$$

$$= 200 + 0j$$

$$= 200\angle 0 \text{ V}$$

To find Zth:

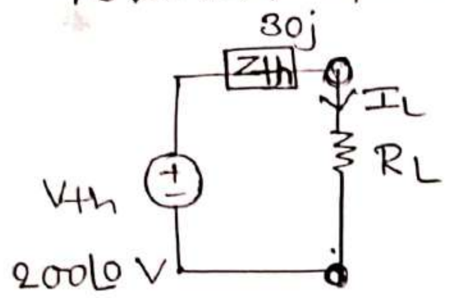


$$Z_{th} = [j10 \parallel -j20] + j10$$

$$= \frac{j10 \times -j20}{j10 - j20} + j10$$

$$= 30j = 30\angle 90^\circ \,\Omega$$

Tevenins equivalent N/W:



Power is maximum

when $R_L = |Z_{th}|$

$= |j30|$

$= 30\,\Omega$

$$I_L = \frac{V_{th}}{Z_{th} + R_L}$$

$$= \frac{200\angle 0}{30j + 30}$$

$$I_L = 4.714\angle -45^\circ \text{ A}$$

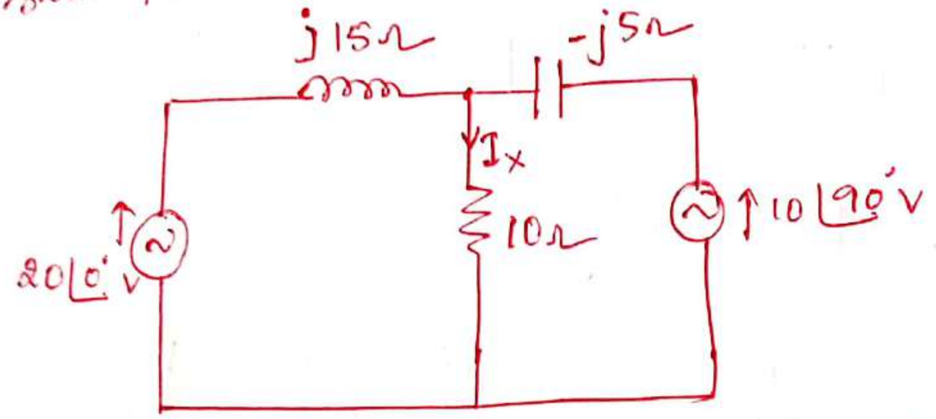
Max. Power is

$$P = I_L^2 R_L$$

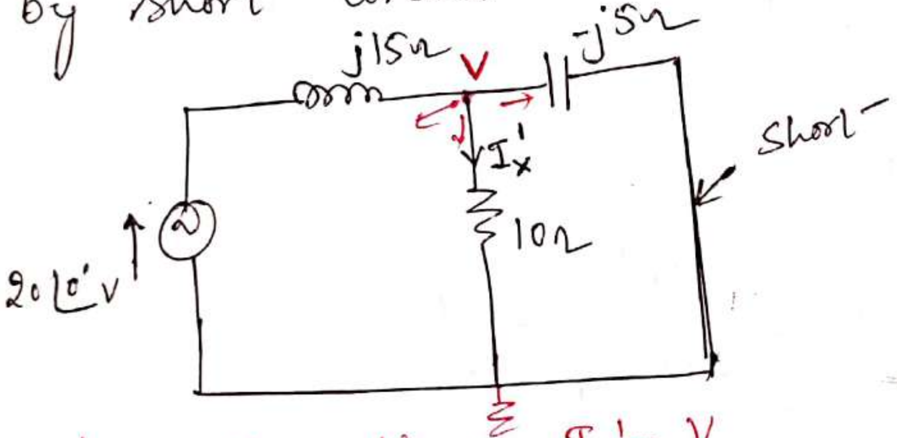
$$= (4.714)^2 (30)$$

$$P = \underline{666.653 \text{ W}}$$

1) Using Superposition theorem determine the current flowing through 10Ω resistance of the n/w shown.



Case 1: Consider only $20\angle 0^\circ$ v & replace $10\angle 90^\circ$ v by short circuit.



from the figure, $I_x' = \frac{V}{10}$

KCL @ node V,

$$\frac{V - 20\angle 0^\circ}{j15} + \frac{V}{10} + \frac{V}{-j5} = 0$$

$$-j0.067V - 1.33\angle -90^\circ + 0.1V + j0.2V = 0$$

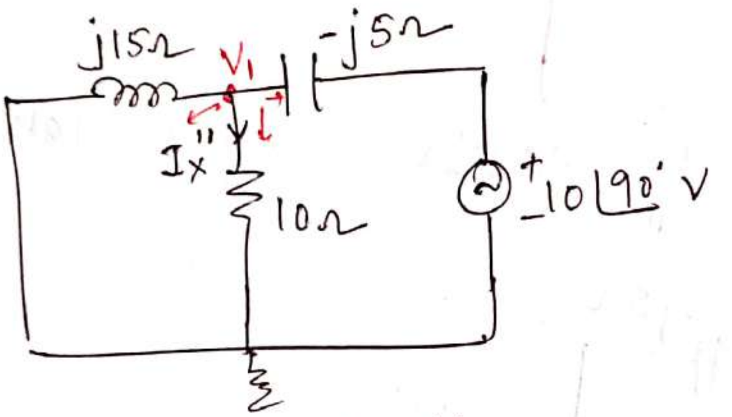
$$(0.1 + j0.133)V = 1.33\angle -90^\circ$$

$$V = \frac{1.33\angle -90^\circ}{0.166\angle 53.06^\circ} = 8.01\angle -143.06^\circ$$

$$I_x' = \frac{8.012 \angle -143.06}{10}$$

$$\boxed{I_x' = 0.8 \angle -143.06 \text{ Amp}} \quad \text{—— (1)}$$

Case 2: Consider $10\angle 90°$ V only.



from the fig

$$I_x'' = \frac{V_1}{10}$$

KCL @ node V_1

$$\frac{V_1}{j15} + \frac{V_1}{10} + \frac{V_1 - 10\angle 90°}{-j5 \rightarrow 5\angle -90°} = 0$$

$$-j0.067 V_1 + 0.1 V_1 + j0.2 V_1 - 2\angle 180° = 0$$

$$(0.1 + 0.133j) V_1 = 2\angle 180°$$

$$V_1 = \frac{2\angle 180°}{0.166\angle 53.13} = 12\angle 126.93$$

$$I_x'' = \frac{V_1}{10} = 1.2\angle 126.93 \text{ Amp} \quad \text{—— (2)}$$

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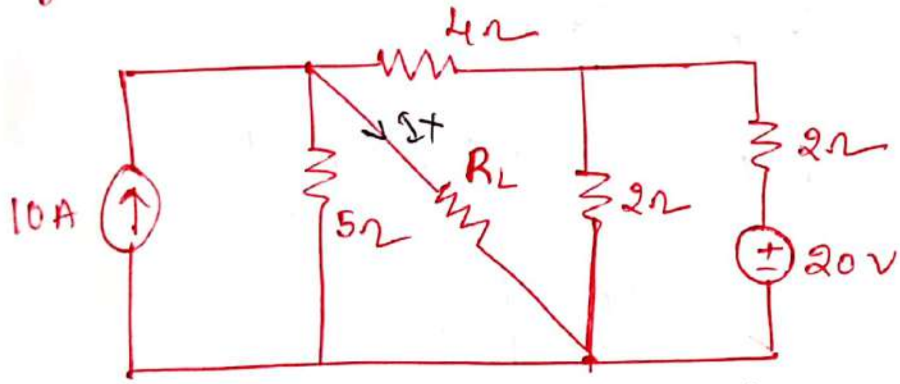
$I_x = I_x' + I_x''$

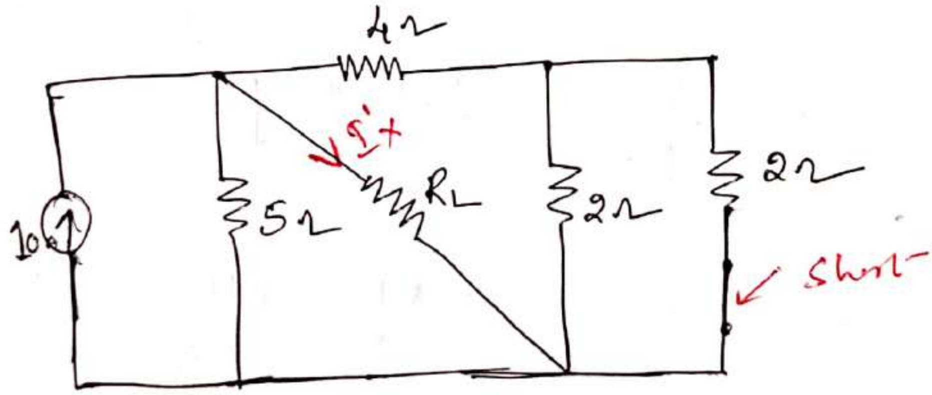
$I_x = 0.8 \angle -143.17 + 1.2 \angle 126.93$

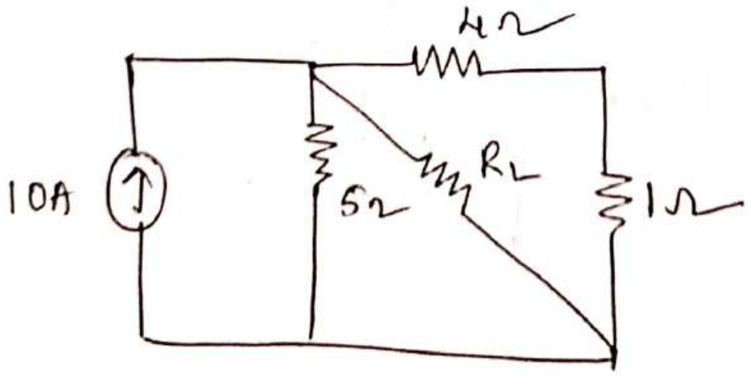
$\boxed{I_x = 1.43 \angle 160^\circ \text{ Amp.}}$

2) Using Superposition theorem, find the current through $R_L = 7.5\Omega$



Consider 10A source alone, short 20V source.





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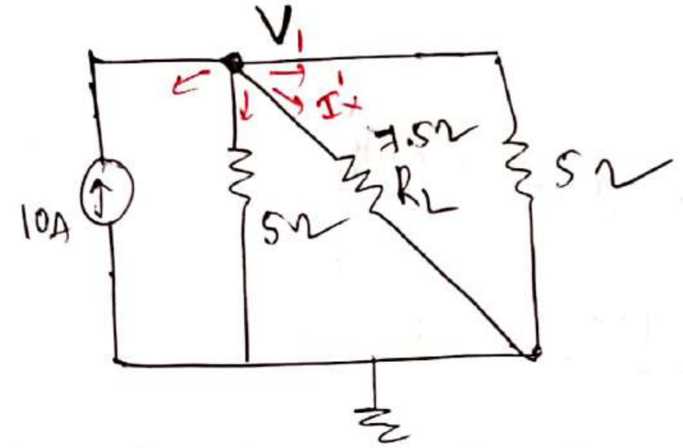


from the figure

$$I_x' = \frac{V_1}{7.5}$$

Apply KCL @ node V

$$-10 + \frac{V_1}{5} + \frac{V_1}{7.5} + \frac{V_1}{5} = 0$$

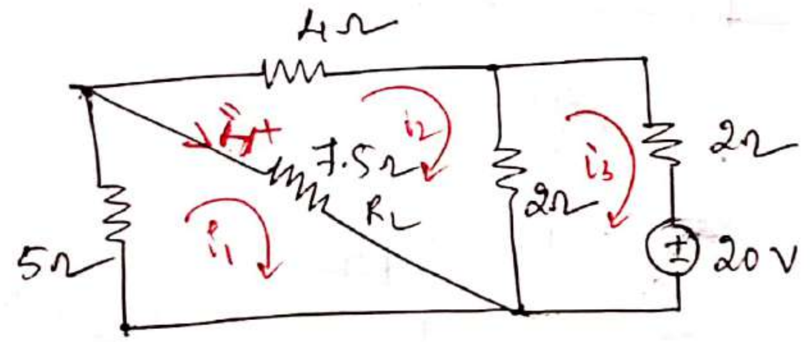
$$-10 + 0.2V_1 + 0.133V_1 + 0.2V_1 = 0$$

$$0.533V_1 = 10$$

$$V_1 = 18.76 \text{ volts}$$

$$\boxed{I_x' = \frac{V_1}{7.5} = 2.5 \text{ Amp}} \quad \text{—— (1)}$$

Consider 20V src & open current source.



loop 1 $\longrightarrow$ $-7.5(i_1 - i_2) - 5i_1 = 0$

$-12.5 i_1 + 7.5 i_2 + 0 i_3 = 0$ —— (a)

loop 2 $\longrightarrow$ $-4i_2 - 2(i_2 - i_3) - 7.5(i_2 - i_1) = 0$

$-4i_2 - 2i_2 + 2i_3 - 7.5 i_2 + 7.5 i_1 = 0$

$7.5 i_1 - 13.5 i_2 + 2 i_3 = 0$ —— (b)

KVL to loop 3

$-2i_3 - 20 - 2(i_3 - i_2) = 0$

$-2i_3 - 20 - 2i_3 + 2i_2 = 0$

$0 i_1 + 2i_2 - 4i_3 = 20$ —— (c)

$i_1 = -0.75A$ $i_2 = -1.25A$ $i_3 = -5.62$ amp

current through 7.5Ω $I_x'' = I_1 - i_2$

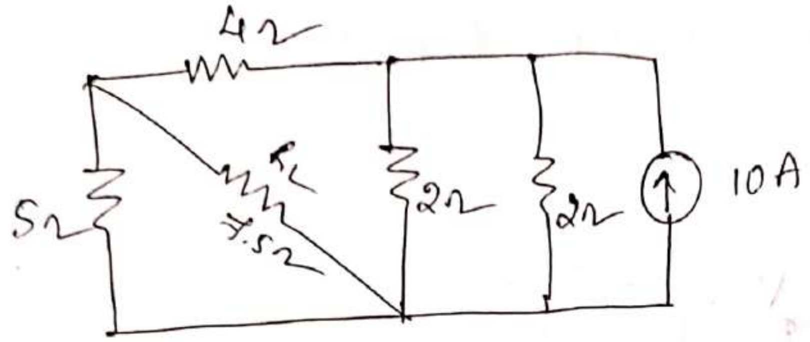
$I_x'' = -0.75 - (-1.25)$

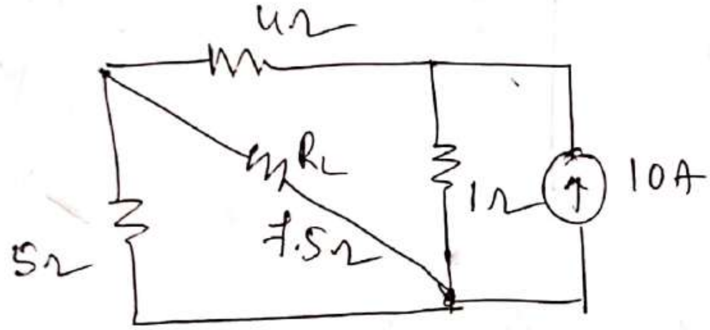
$\boxed{I_x'' = 0.5 \text{ Amp}}$ —— (2)

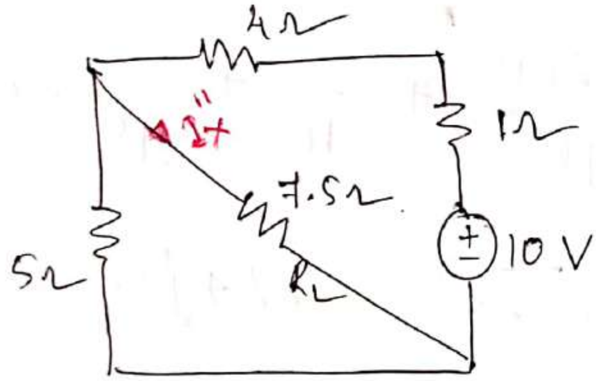
$\therefore$ $I_x = I_x' + I_x''$

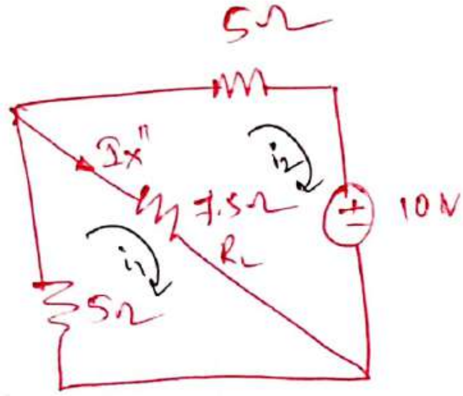
$\hookrightarrow = 2.5 + 0.5$

$\boxed{I_x = 3 \text{ Amp}}$









$$-7.5(i_1 - i_2) - 5i_1 = 0$$

$$-12.5i_1 + 7.5i_2 = 0 \quad \text{——} (1)$$

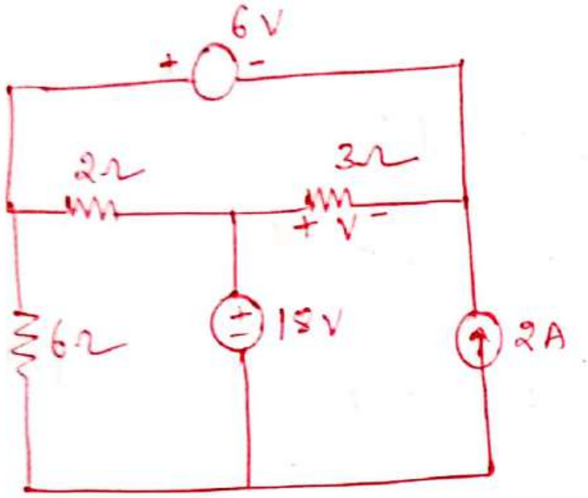
$$-5i_2 - 10 - 7.5(i_2 - i_1) = 0$$

$$7.5i_1 - 12.5i_2 = 10 \quad \text{——} (2)$$

$i_1 = \underline{\underline{-0.75}}$ amp $\quad i_2 = \underline{-1.25}$ amp $\quad \therefore I_x'' = i_1 - i_2$

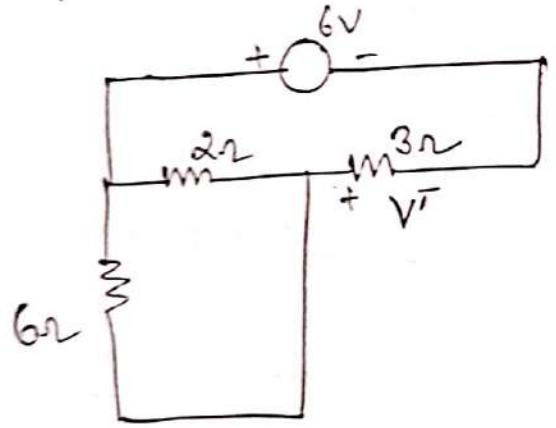
$I_x'' = 0.5$ amp

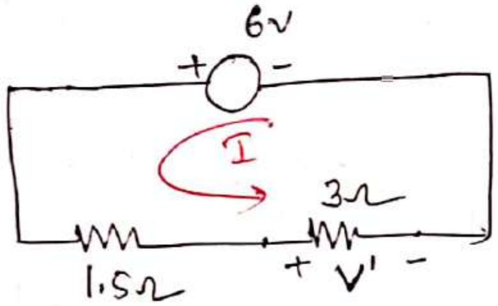
③ Find the voltage V across 3Ω resistor using super position theorem for the ckt shown.



Case 1:

Consider 6V vg src, short ckt 18V src & open ckt 2A src.





$$6 - 1.5I - 3I = 0$$

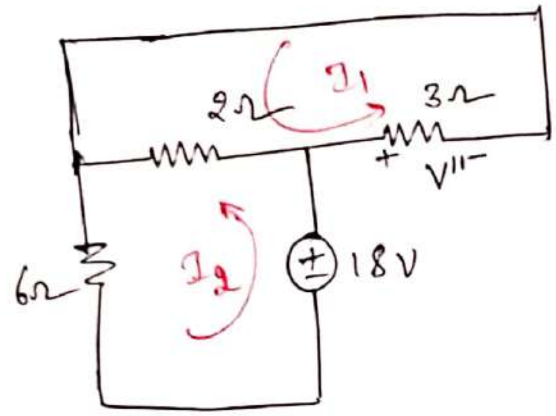
$$4.5I = 6$$

$$I = 1.33\,A$$

$$\therefore \boxed{V' = 3I = 4V} \quad \text{——— } ①$$

Case 2:

Consider 18V vg src



from the ckt

$V'' = 3I_1$

KVL to 1st loop

$-2(I_1 - I_2) - 3I_1 = 0$

$-2I_1 + 2I_2 - 3I_1 = 0$

$-5I_1 + 2I_2 = 0$ —— (a)

KVL to 2nd loop

$-2(i_2 - i_1) - 6i_2 + 18 = 0$

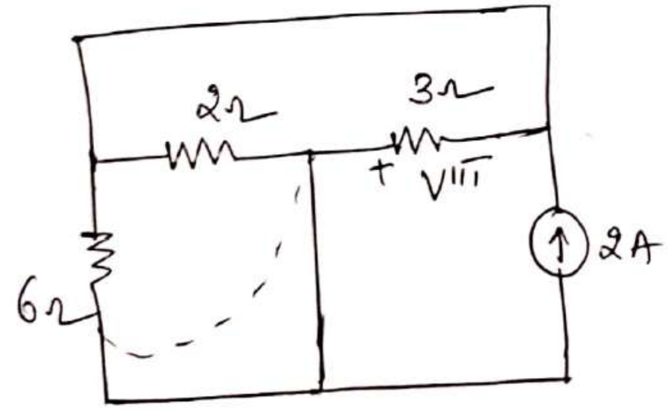
$2i_1 - 8i_2 = -18$ —— (b)

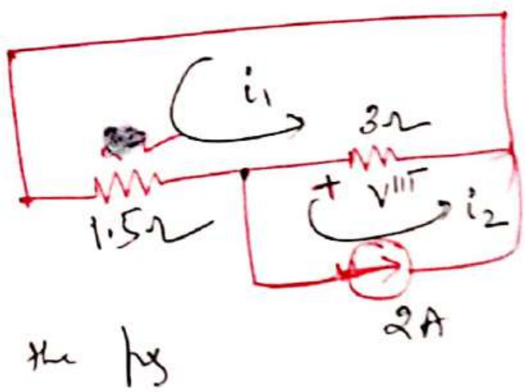
we get

$I_1 = 1A \quad I_2 = 2.5\,A$

$\therefore V'' = 3I_1 \quad \boxed{V'' = 3V}$ —— (2)

Case 3 :- Consider 2A current source





from the fig

$V''' = 3(i_1 - i_2)$

but $\boxed{i_2 = 2A}$

$$-1.5 i_1 - 3(i_1 - i_2) = 0.$$

$$-4.5 i_1 + 3 i_2 = 0$$

$$\cancel{+}4.5 i_1 = \cancel{+}3 \times 2$$

$$i_1 = \frac{6}{4.5} = \cancel{2\ Amp}\ 1.33\ \text{Amp}$$

$$\therefore \cancel{V''' = 3(2-3) =}$$

$$V''' = 3(2 - 1.33)$$

$$\boxed{V''' = -2\ \text{volt}} \quad \text{——— (3)}$$

$$\therefore V = V' + V'' + V''' = 9\ \text{volts}$$

$$V''' = 3(i_2 - i_1) = 3(1.33$$

$$= 3(2 - 1.33)$$

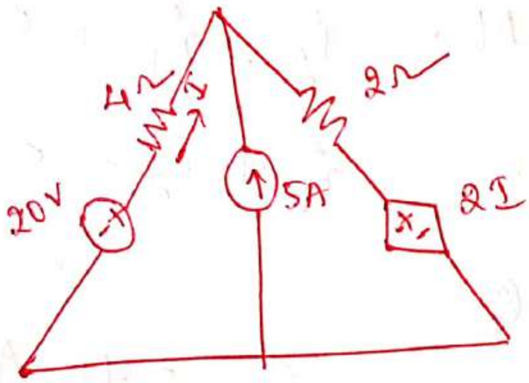
$$= -2\ \text{volts}$$

$\therefore \quad V = V' + V'' + V'''$

$V = 4 + 3 - 2$

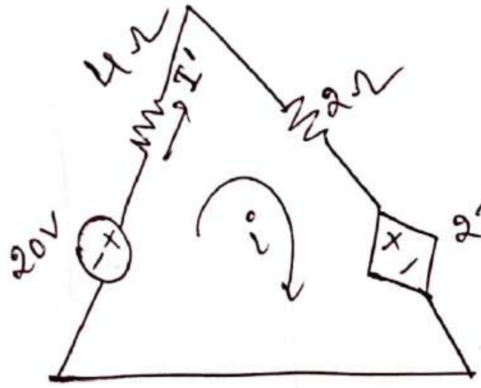
$$\boxed{V = 5 \text{ volts}}$$

5) For the ckt shown in below fig, find the current I using Superposition theorem.



Case i)
Consider 20V src, open ckt 5A current src & keep dependent src as it is,

KVL to loop



$20 - 4i - 2i - 2I' = 0$

from the fig $\boxed{i = I'}$

$20 - 6i - 2i = 0$

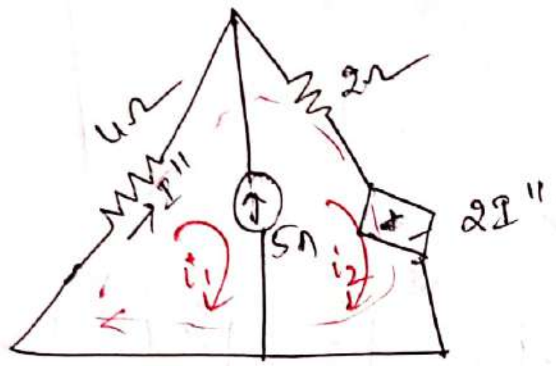
$8i = 20 \quad i = 2.5 \text{ Amp}$

$\therefore \boxed{I' = 2.5 \text{ amp}}$ —— (A)

Case ii)

Consider 5A current src & short 20V vg src

Supermesh



$$-4i_1 - 2i_2 - 2I'' = 0$$

from fig $I'' = i_1$

$$-4i_1 - 2i_2 - 2i_1 = 0$$

5A is b/w 1st & 2nd loop hence Supermesh.

$$-6i_1 - 2i_2 = 0 \quad \text{--- (1)}$$

Also $i_2 - i_1 = 5$

or $-i_1 + i_2 = 5$ --- (2)

Solve (1) & (2),

$I_1 = -1.25A$ & $i_2 = 3.75$ Amp

$\therefore$ $\boxed{I'' = -1.25 \text{ Amp}}$ --- (B)

$\therefore$ from Superposition theorem.

$$I = I' + I''$$

$$I = 2.5 - 1.25$$

$$\boxed{I = 1.25 \text{ Amp}}$$

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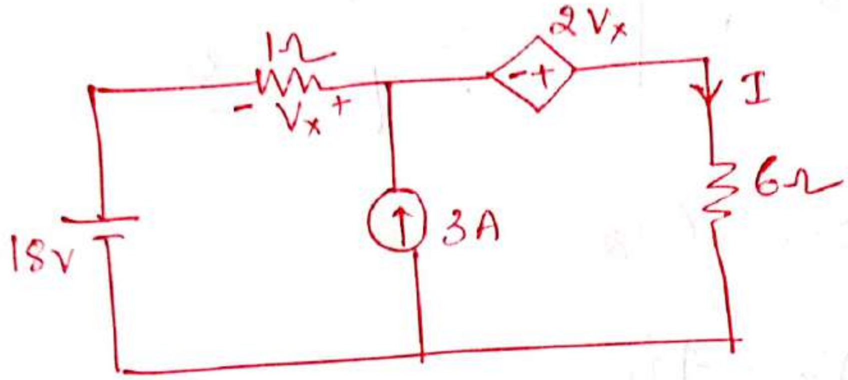
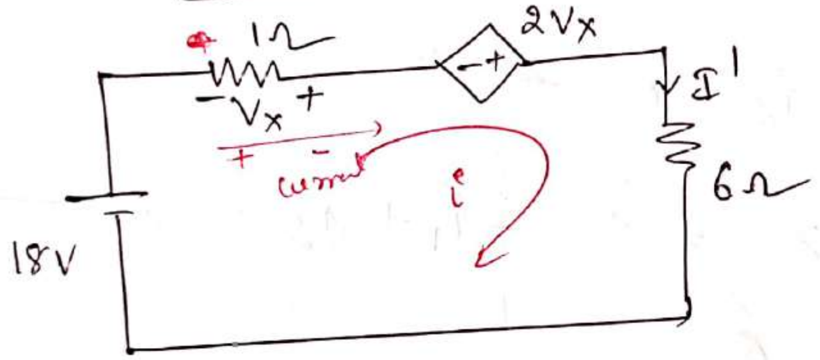
6) Using Superposition theorem find the current in 6Ω resistor in the n/w shown.



case 1) Consider 18V src



$$18 - 1i + 2V_x - 6i = 0$$

from the fig $V_x = -1i$

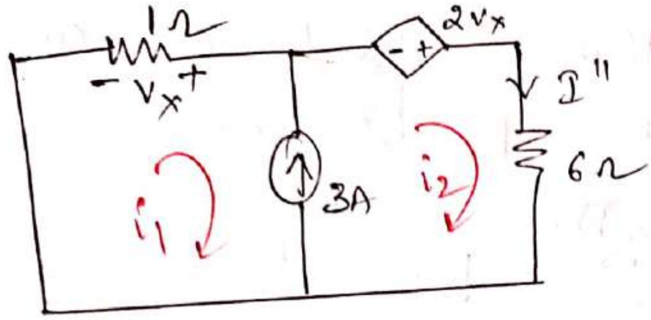
$$18 - i + 2(-1i) - 6i = 0$$

$$-9i = -18$$

$$\boxed{i = 2A}$$

$\therefore$ $\boxed{I' = i = 2\,Amp}$ — (a)

case ii) Consider 3A current src



3A in b/n 1st & 2nd loop hence Supermesh.

$$-1 i_1 + 2V_x - 6 i_2 = 0$$

but $V_x = -1 i_1$

$$-i_1 + 2(-1 i_1) - 6 i_2 = 0$$

$$-3 i_1 - 6 i_2 = 0 \quad \text{—— (1)}$$

& $i_2 - i_1 = 3 \implies -i_1 + i_2 = 3$ —— (2)

solve (1) & (2)

$\boxed{i_1 = -2A}$ $\boxed{i_2 = 1A}$

$\therefore \boxed{I'' = i_2 = 1A}$ —— (b)

from superposition theorem.

$$I = I' + I''$$

$$I = 2 + 1 = 3 \text{ Amp}$$

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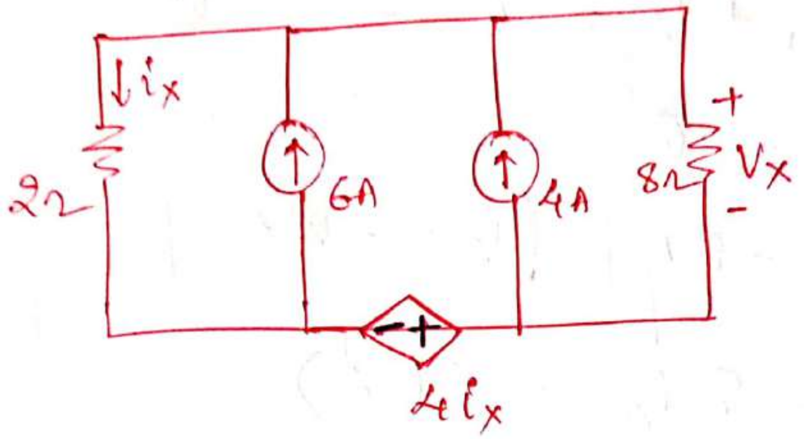
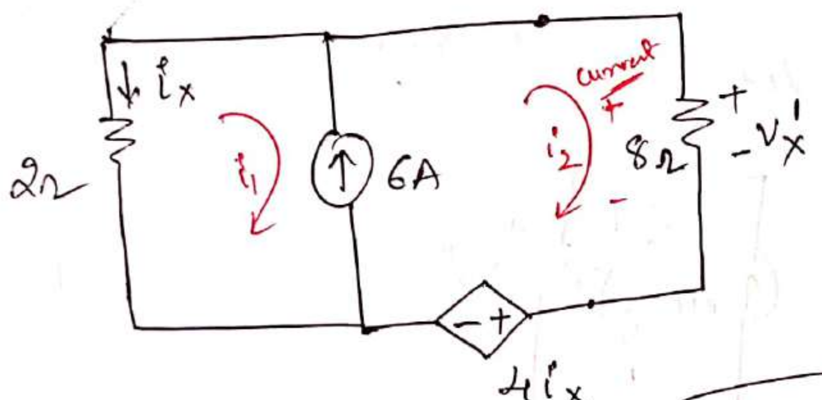
7) Use Superposition theorem to find V_x in the ckt shown below.



Case i) Consider 6A current src. Open ckt 4A src



from the fig $\boxed{i_x = -i_1}$

$$\boxed{V_x' = 8\, i_2}$$

& 6A src is b/w 1st & 2nd loop ∴ Supermesh

$$-2i_1 - 8i_2 - 4i_x = 0$$

$$-2i_1 - 8i_2 - 4(-i_1) = 0$$

$$2i_1 - 8i_2 = 0 \quad \text{——— (1)}$$

& $i_2 - i_1 = 6$

or $-i_1 + i_2 = 6$ —— (2)

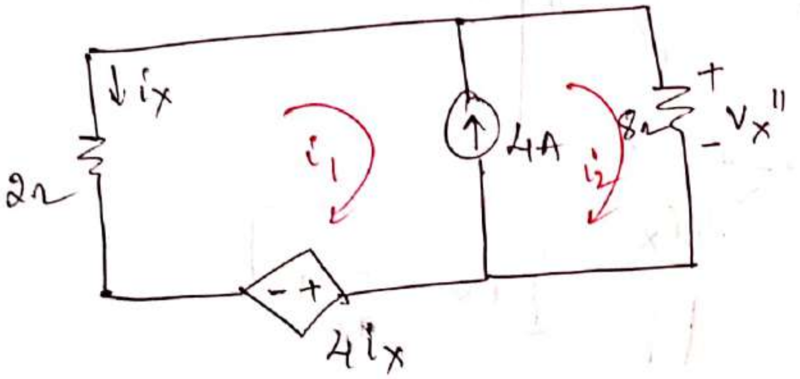
solve (1) & (2)

$\boxed{i_1 = -8A}$ $\boxed{i_2 = -2A}$

$\therefore V_x' = 8\, i_2 = 8(-2)$

$\boxed{V_x' = -16 \text{ volts}}$ —— (a)

Case ii) Consider 4A current src



from the fig $i_1 = -i_x \Rightarrow \boxed{i_x = -i_1}$

& $\boxed{V_x'' = 8\, i_2}$

→ 4A source lies b/w 1st & 2nd loop hence

Super mesh

from 1st fig $i_2 - i_1 = 4 \rightarrow -i_1 + i_2 = 4$ —— (1)

Supermesh (KVL) $-8i_2 - 4i_x - 2i_1 = 0$

$$-8i_2 - 4(-i_1) - 2i_1 = 0$$

$$2i_1 - 8i_2 = 0 \quad \text{—— (5)}$$

Solve (1) & (2) $\boxed{i_1 = -5.33 \text{ Amp}}$.

$$\boxed{i_2 = -1.33 \text{ Amp.}}$$

$\therefore \quad V_x'' = 8 \times -1.33$

$$\boxed{V_x'' = -10.64 \text{ volts}} \quad \text{—— (6)}$$

$\therefore \quad V_x = V_x' + V_x''$

$$V_x = -16 - 10.64$$

$$\boxed{V_x = -26.64 \text{ volts}}$$

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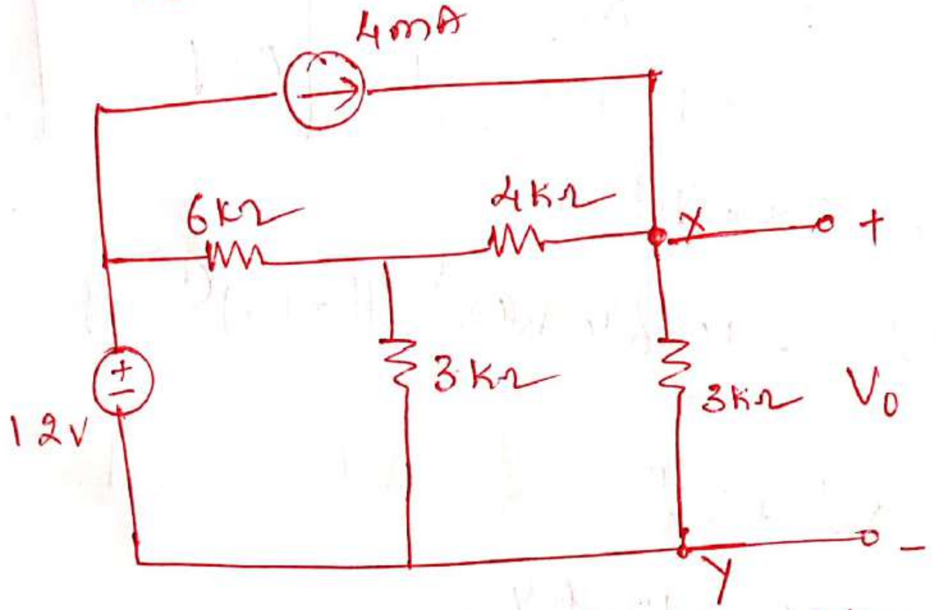
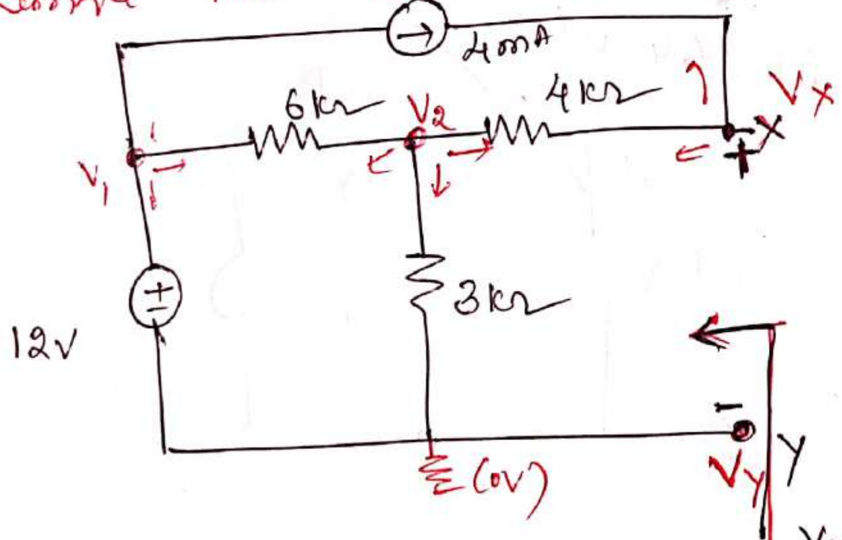
Thevenins theorem :-

1) Obtain the Thevenins equivalent of n/w shown in below fig b/n terminals X & Y. Also find V_o



Remove the load & create open ckt



V_{xy} which is nothing but V_{th}

$$V_{xy} = V_x - V_y$$

$$\boxed{V_{th} = V_{xy}}$$

KCL @ node 1

$$\boxed{V_1 = 12V}$$

KCL @ node 2

$$\frac{V_2 - V_1}{6k} + \frac{V_2}{3k} + \frac{V_2 - V_x}{4k} = 0$$

$$V_2\left[\frac{1}{6k} + \frac{1}{3k} + \frac{1}{4k}\right] - \frac{12}{6k} - \frac{V_x}{4k} = 0$$

$$0.75 \times 10^{-3} V_2 - 0.25 \times 10^{-3} V_x = 2 \times 10^{-3} \quad \text{--- (1)}$$

KCL @ node Vx

$$-4 \times 10^{-3} + \frac{V_x - V_2}{4k} = 0$$

$$-0.25 \times 10^{-3} V_2 + 0.25 \times 10^{-3} V_x = 4 \times 10^{-3} \quad \text{--- (2)}$$

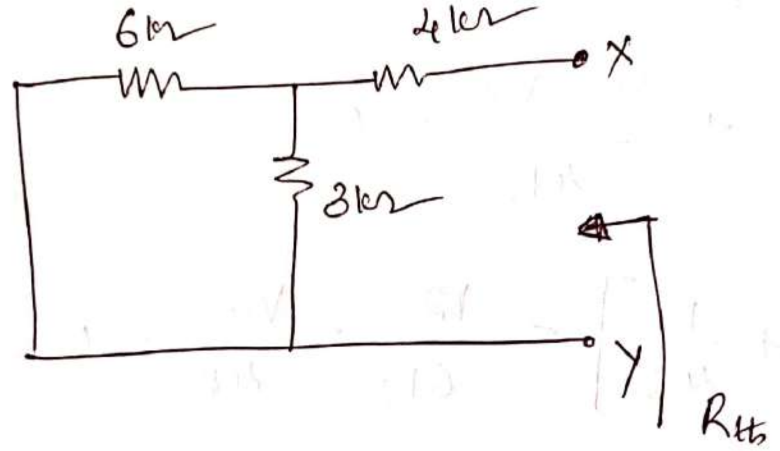
Solve (1) & (2)

$V_2 = 12$ volts $\qquad V_x = 28$ volts

And $\boxed{V_y = 0}$ ∵ bottom node is grounded)

$$V_{th} = V_{xy} = 28 \text{ volts}$$

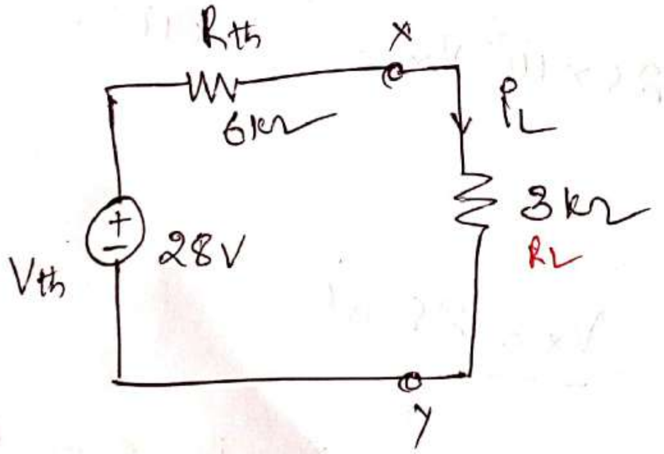
To find R_{th} :-



$$R_{th} = (6k \parallel 3k) + 4k.$$

$$\boxed{R_{th} = 6\,k\Omega}$$

Thevenin's Equivalent ckt



$$i_L = \frac{V_{th}}{R_{th} + R_L}$$

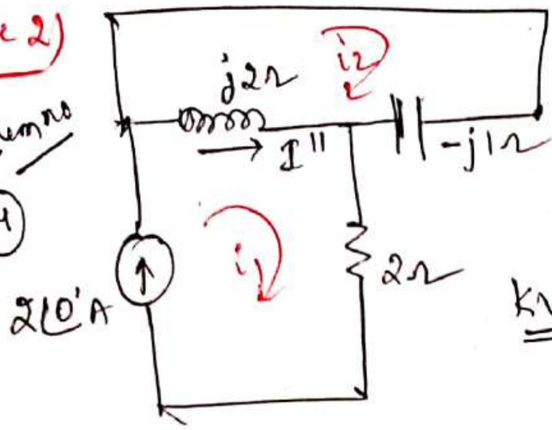
$$i_L = \frac{28}{6k + 3k}$$

$$\boxed{i_L = 3.11\, mA}$$

$$\therefore\ V_0 = I_L \times R_L = 9.33 \text{ volts}$$

Case 2)

Problem no (4)



$$\boxed{i_1 = 2\angle 0^\circ}$$

KVL $j1(i_2) - j2(i_2 - i_1) = 0$

$$j1\, i_2 - j2\, i_2 + j2\, i_1 = 0$$

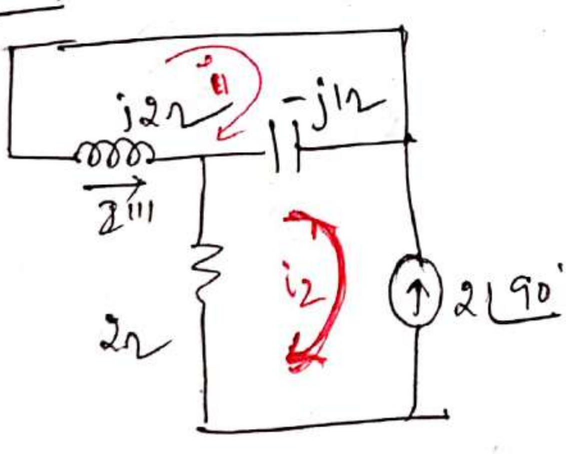
$$-\cancel{j}1\, i_2 = -\cancel{j}2\, i_1$$

$$\cancel{i_2 = 2}$$

$$i_2 = 2 \times 2\angle 0^\circ = 4\angle 0^\circ$$

$$\therefore \boxed{I'' = i_1 - i_2 = 2 - 4 = -2 \text{ Amp}}$$

Case (iii) :-



$$\boxed{i_2 = -2\angle 90^\circ}$$

KVL : $j1(i_1 - i_2) - j2\, i_1 = 0$

$$j1\, i_1 - j1\, i_2 - j2\, i_1 = 0$$

$$-j1\, i_1 = j1\, i_2$$

$$-i_1 = i_2 \qquad i_1 = -i_2 = 2\angle 90^\circ$$

$$\boxed{I''' = -i_1 = -2\angle 90^\circ}$$

$\therefore \quad I = I' + I'' + I'''$

$I = 8\angle{-135^\circ} - 2 - 2\angle{90^\circ}$

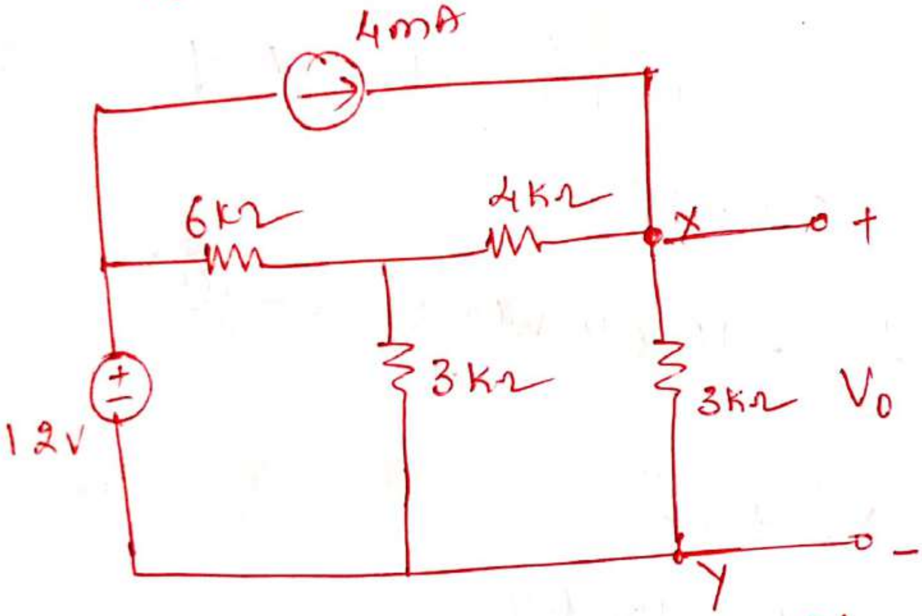
$I = -5.65 - j5.65 - 2 - 2j$

$I = -7.65 - 7.65j$

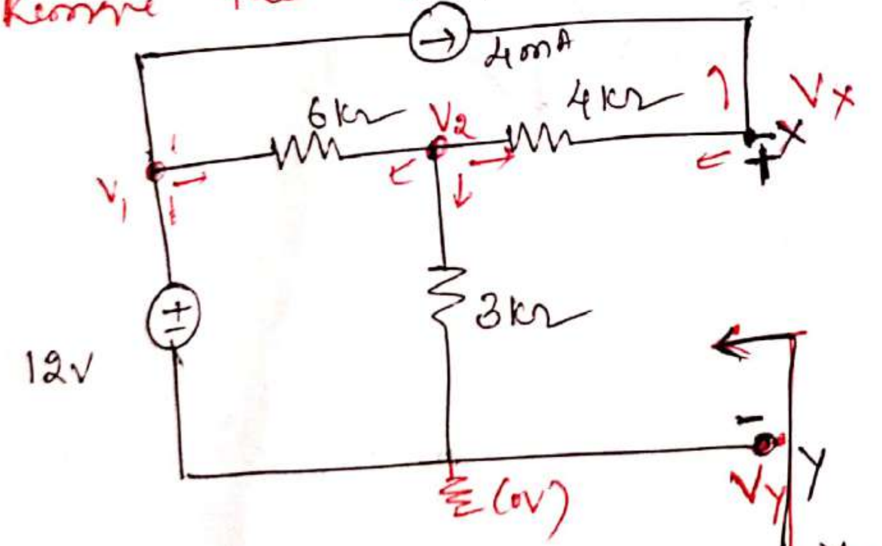
$$\boxed{I = 10.83\angle{-135^\circ} \text{ Amp}}$$

Thevenins theorem :-

1) Obtain the Thevenins equivalent of n/w shown in below fig b/n terminals X & Y. Also find V_0



Remove the load & create open ckt



V_{xy} which is nothing but V_{th}

$$V_{xy} = V_x - V_y$$

$$\boxed{V_{th} = V_{xy}}$$

KCL @ node 1

$\boxed{V_1 = 12V}$

KCL @ node 2

$$\frac{V_2 - V_1}{6K} + \frac{V_2}{3K} + \frac{V_2 - V_x}{4K} = 0$$

$$V_2\left[\frac{1}{6K} + \frac{1}{3K} + \frac{1}{4K}\right] - \frac{12}{6K} - \frac{V_x}{4K} = 0$$

$$0.75 \times 10^{-3} V_2 - 0.25 \times 10^{-3} V_x = 2 \times 10^{-3} \quad \text{—— (1)}$$

KCL @ node Vx

$$-4 \times 10^{-3} + \frac{V_x - V_2}{4K} = 0$$

$$-0.25 \times 10^{-3} V_2 + 0.25 \times 10^{-3} V_x = 4 \times 10^{-3} \quad \text{—— (2)}$$

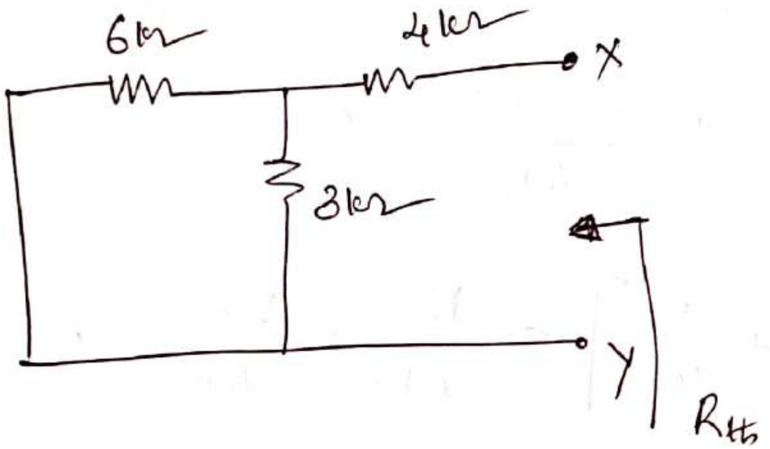
Solve (1) & (2)

$V_2 = 12$ volts $\quad$ $V_x = 28$ volts

And $\boxed{V_y = 0}$ $\because$ bottom node is grounded)

$V_{th} = V_{xy} = 28$ volts

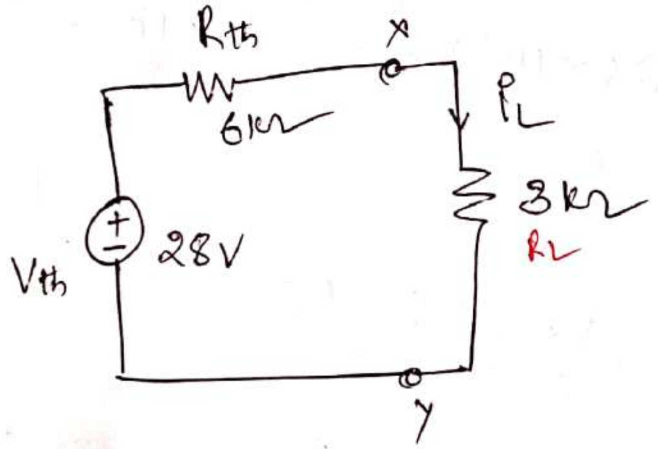
To find R_{th} :-



$$R_{th} = (6k \parallel 3k) + 4k.$$

$$\boxed{R_{th} = 6\,k\Omega}$$

Thevenin's Equivalent ckt



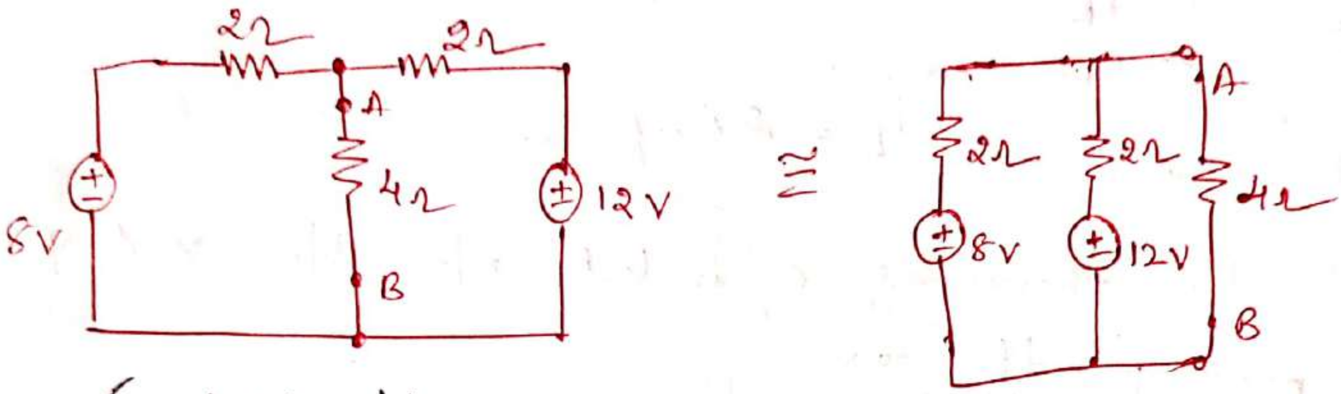
$$i_L = \frac{V_{th}}{R_{th} + R_L}$$

$$i_L = \frac{28}{6k + 3k}$$

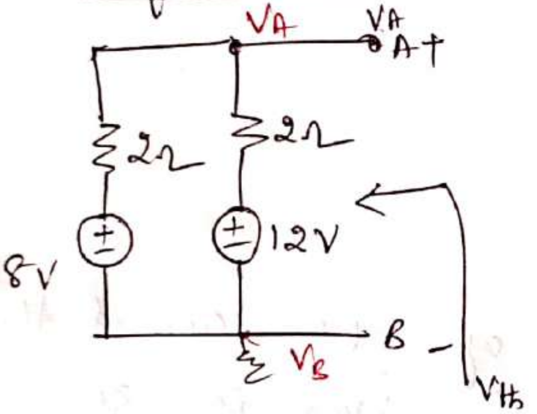
$$\boxed{i_L = 3.11\,mA}$$

$\therefore$ $V_0 = I_L \times R_L = 9.33$ volts

2) Find the Thevenin's equivalent for the n/w at the load terminals A & B. If the load across A & B is 4Ω. Determine the load current.



To find V_{th}



$$V_{th} = V_A - V_B$$

→ KCL @ node A

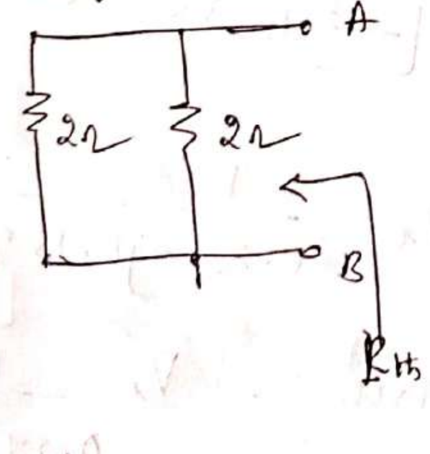
$$\frac{V_A - 8}{2} + \frac{V_A - 12}{2} = 0$$

$$0.5V_A - 4 + 0.5V_A - 6 = 0$$

$\boxed{V_A = 10 \text{ volts}}$ & $\boxed{V_B = 0}$

$\therefore \boxed{V_{th} = 10 \text{ volts}}$

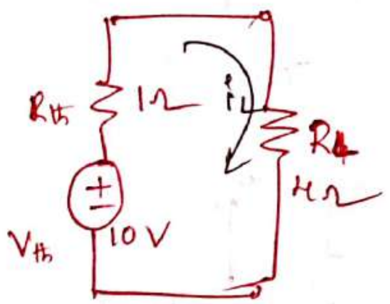
To find R_{th} :-



$$R_{th} = \frac{2 \times 2}{2+2} = 1\Omega$$

$$\boxed{R_{th} = 1\Omega}$$

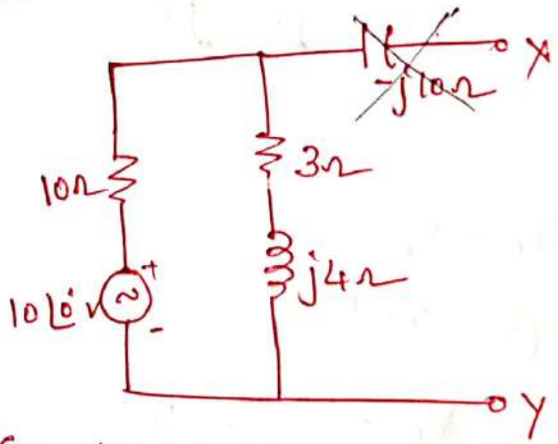
Thevenins ckt :-



$$i_L = \frac{V_{th}}{R_{th} + R_L} = \frac{10}{4+1}$$

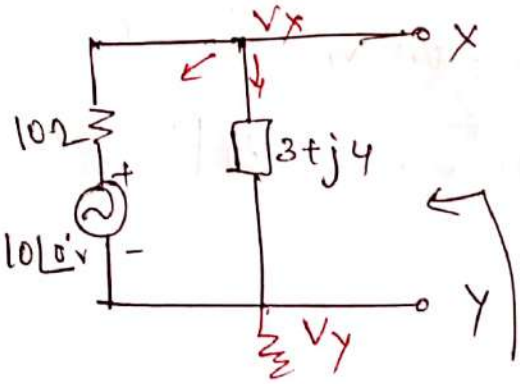
$$\boxed{i_L = 2\,Amp}$$

8) Obtain the thevenins equivalent n/w b/n X & Y



To find V_{th} :-

Since open ckt current through $-j10\Omega$ is zero



$$V_{th} = V_x - V_y$$

V_{th}

KCL

$$\frac{V_x - 10\angle 0°}{10} + \frac{V_x}{3+j4} = 0$$

$$0.1V_x - 1\angle 0° + 0.2\angle -53.13\, V_x = 0.$$

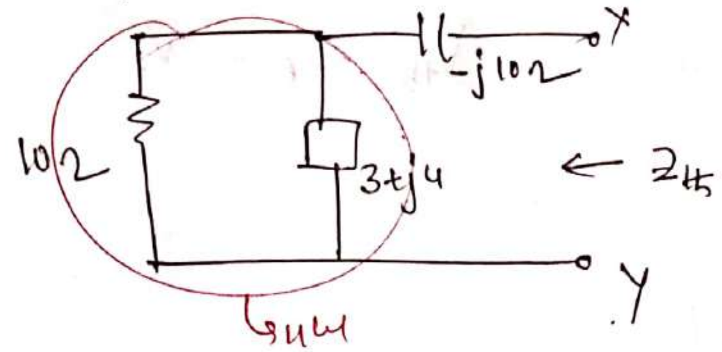
$$0.1V_x + (0.12 - j\,0.159)\,V_x = 1$$

$$(0.22 - j\,0.159)\,V_x = 1 \Rightarrow V_x = \frac{1}{0.22 - j0.159}$$

$$\boxed{V_{th} = 3.676\angle 36.03 \text{ volts}}$$

$$V_x = \frac{1}{0.27\angle -35.8°}$$

To find Z_{th} :-



$$Z_1 = 10 \parallel (3+j4)$$

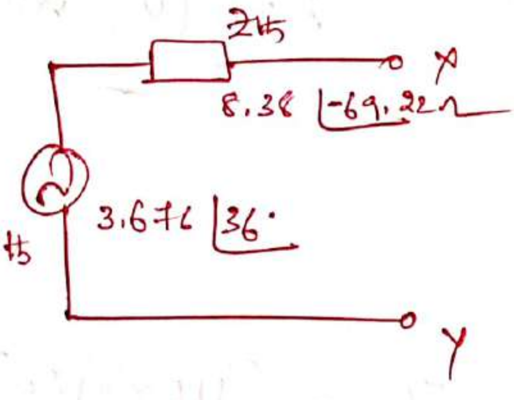
$$Z_1 = \frac{10 \times (3+j4)}{10+3+j4}$$

$$Z_1 = \frac{30+j40}{13+j4} =$$

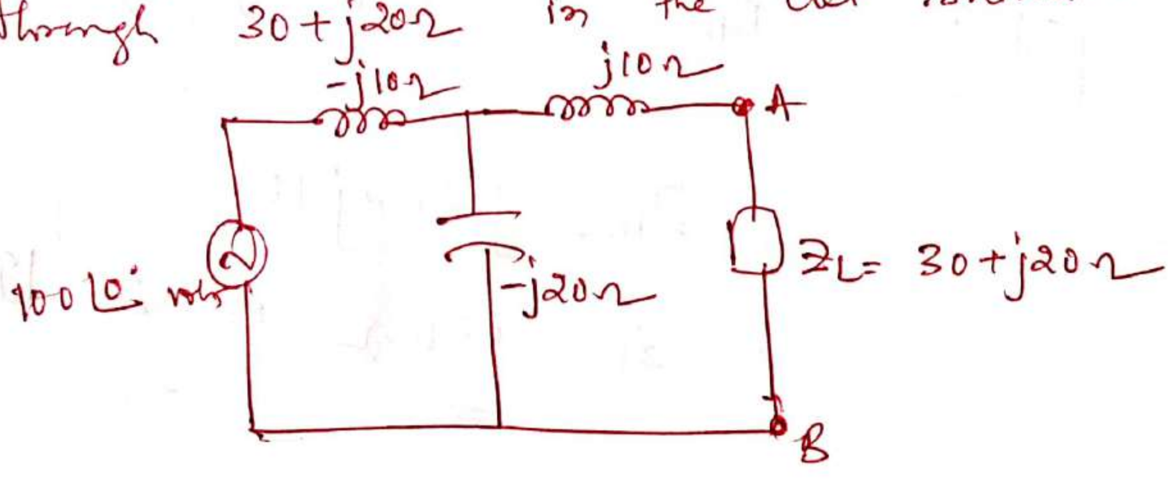
$$Z_{th} = -j10 +$$

$$\boxed{Z_{th} = 8.38 \angle -69.22 \Omega}$$

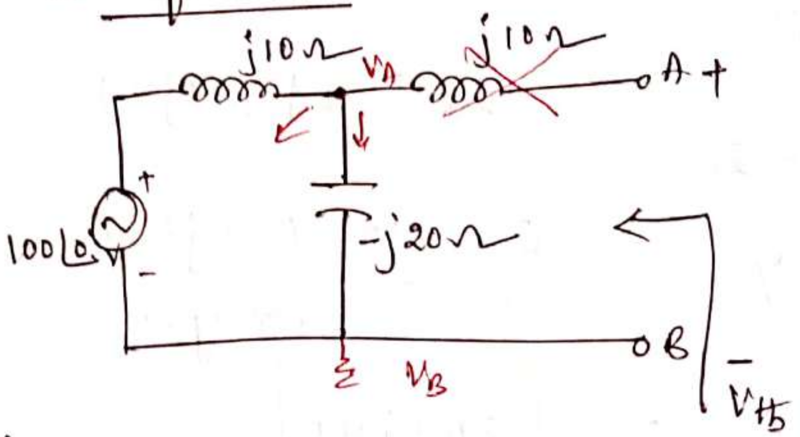
Thevenin's equivalent ckt



4) Using Thevenin's theorem find the current flowing through $30+j20\Omega$ in the ckt shown.



To find V_{th} :



$V_{th} = V_A - V_B$

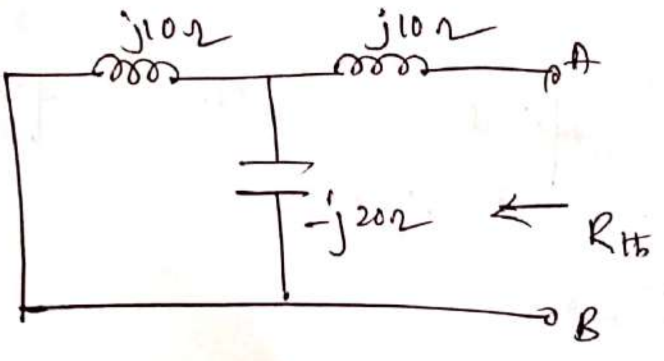
KCL:
@ A
$$\frac{V_A - 100\angle 0°}{j10 \rightarrow 10\angle 90°} + \frac{V_A}{-j20} = 0$$

$$-j0.1 V_A - 10\angle -90° + j0.05 V_A = 0$$

$$-j0.05 V_A = 10\angle -90°$$

$$V_A = \frac{10\angle -90°}{0.05\angle -90°} = 200\angle 0° \text{ volts.}$$

To find R_{th} or Z_{th} :



$$Z_{th} = \left(\frac{j10 \times -j20}{j10 - j20}\right) + j10$$

$$Z_{th} = j20 + j10$$

$$Z_{th} = j30\,\Omega \text{ or } 30\angle 90°\,\Omega$$

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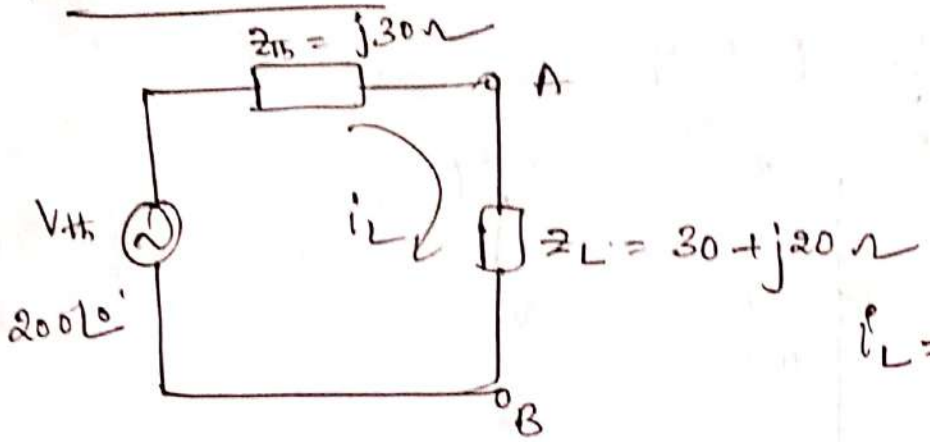
Thevenin's n/w



$$i_L = \frac{V_{th}}{Z_{th} + Z_L}$$

$$i_L = \frac{200\angle 0^\circ}{j30 + 30 + j20}$$

$$\boxed{i_L = 3.43\angle -59^\circ \text{ Amp}}$$

Note :- If the given n/w consists of some dependent sources, then these dependent sources must be kept as it is while calculating Z_{th} & should not be shorted or open ckt'd. whether it is voltage or current source.

In such cases,

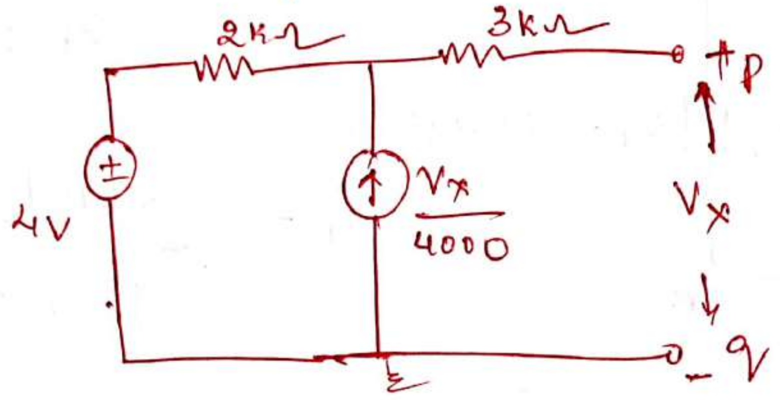
$$\boxed{Z_{th} = \frac{V_{th}}{I_{SC}}}$$

where,

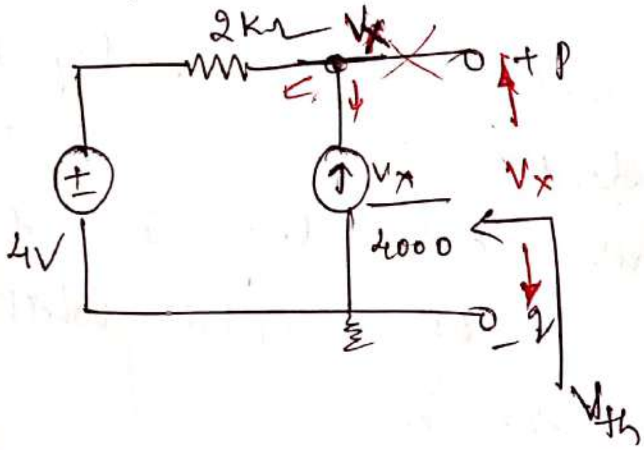
$I_{SC} \rightarrow$ Short ckt current obtained by shorting the load terminals.

$V_{th} \rightarrow$ Thevenin's vg or open ckt vg across load terminals.

1) For the n/w shown, obtain the Thev equivalent across terminals p & q.



To find V_{th} :-



Since no current flows through 3kΩ

$V_{th} = V_x$

$V_x = V_p - V_q$

$V_x = V_p$ ($\because V_q = 0$)

KCL :-

$$\frac{V_x - 4}{2k} + \frac{V_x}{4000} = 0$$

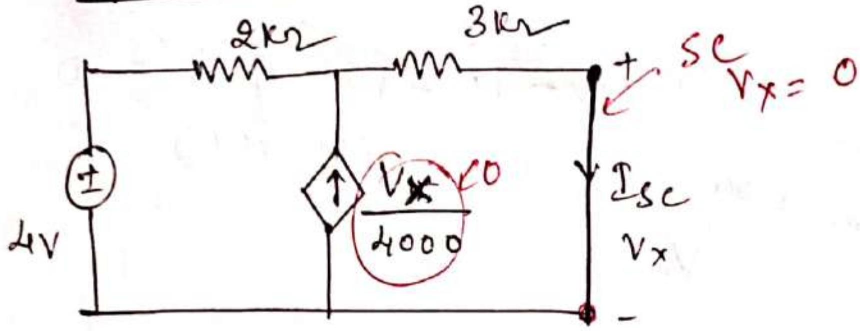
$$\frac{V_x - 4}{2000} = \frac{V_x}{4000}$$

$$4000V_x - 16000 = 2000V_x$$

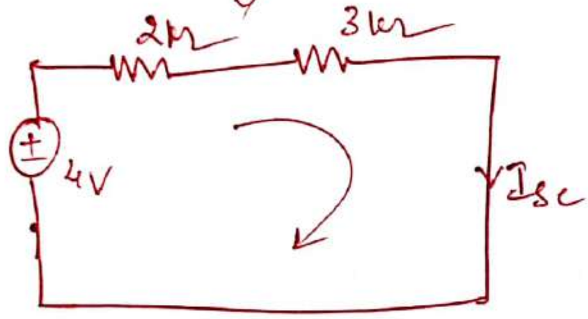
$$\boxed{V_x = 8V}$$

$$\therefore \boxed{V_{th} = 8V}$$

To find Z_{th} :



⇓

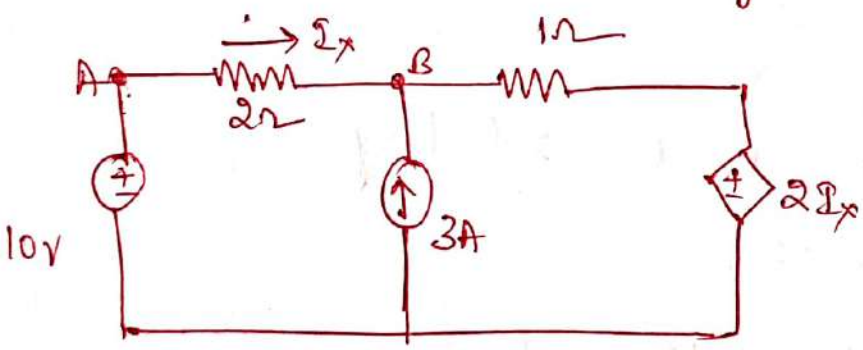


$$I_{sc} = \frac{4}{2k + 3k} = 0.8\,mA$$

$$\therefore\; Z_{th} = \frac{V_{th}}{I_{sc}} = \frac{8}{0.8\,mA}$$

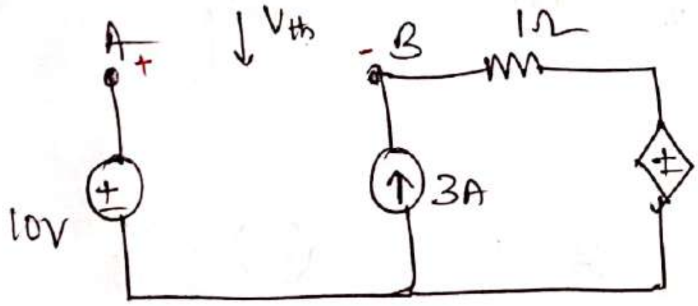
$$Z_{th} = 10\,k\Omega$$

2) Obtain the current I_x by T. theorem.



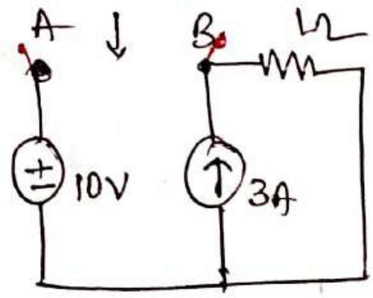
To find V_{th} :-

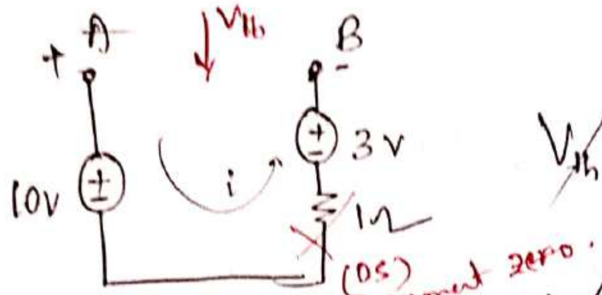
Remove 2Ω resistance. open circuit $I_x = 0$



$2I_x = 2 \times 0$
$= 0V$

≅





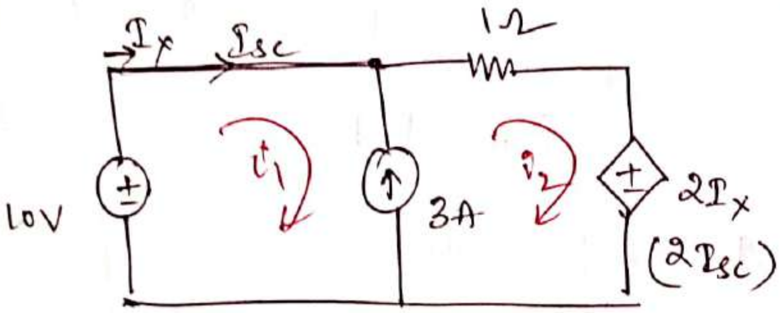
$\cancel{V_{Th} = -10 - 1\cdot i + 3 = 0}$ (open ckt)

$V_{Th} =$

$$V_{Th} - 10 + 3 = 0$$

$$\boxed{V_{Th} = 7V}$$

To find R_{Th} :-



from the fig

$I_x = I_{sc}$.

Also, $I_{sc} = I_1$

→ 3A is in b/w 1st & 2nd loop.

∴ Supermesh.

$$-i_2 - 2I_{sc} + 10 = 0$$

$$-i_2 - 2i_1 + 10 = 0.$$

or $-2i_1 - i_2 = -10$ ——— (1)

And $i_2 - i_1 = 3$

or $-i_1 + i_2 = 3$ ——— (2)

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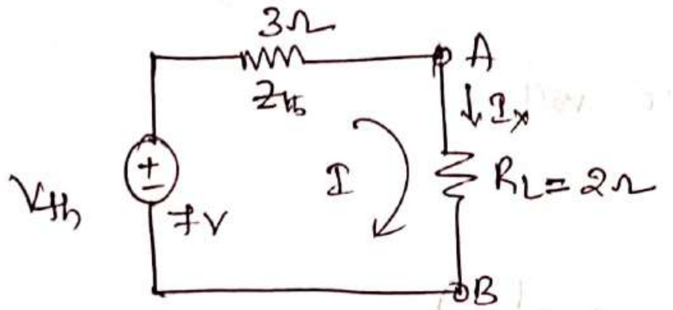
Solve ① & ②

$\boxed{I_1 = 7/3\ A}$ $\boxed{I_2 = 16/3\ \text{Amp}}$

i.e. $I_{SC} = I_1 = 7/3\ A$.

$\therefore\ Z_{th} = \dfrac{V_{th}}{I_{SC}} = \dfrac{7}{7/3} = 3\Omega$

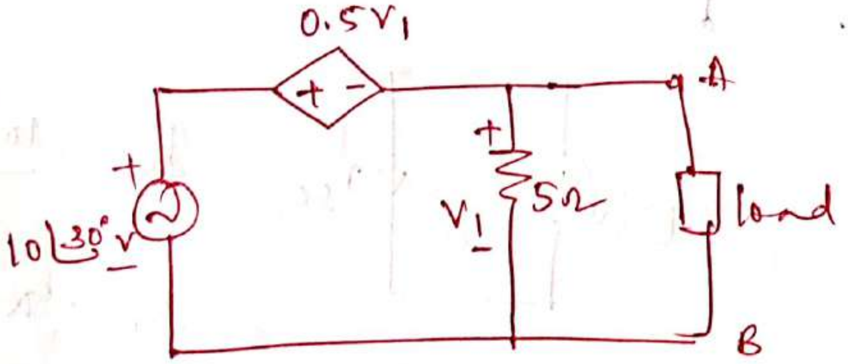


$I = \dfrac{V_{th}}{Z_{th} + R_L}$

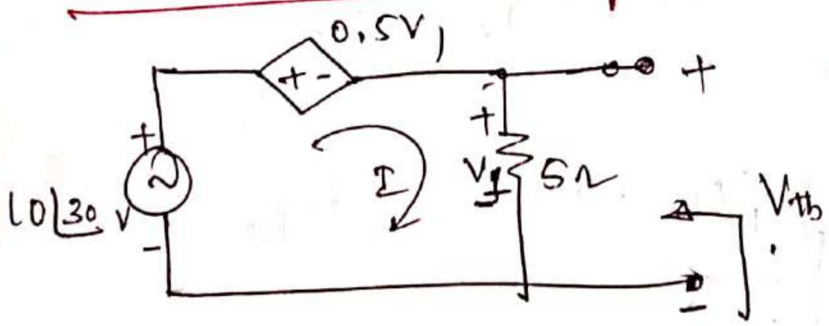
$I = \dfrac{7}{3+2} = 1.4\ \text{Amp}$

$\Rightarrow \boxed{I_x = 1.4\ \text{Amp}}$

3) Find the Th. equivalent ckt across load.



Remove the load to find V_{th} :-



from the fig

$$V_{th} = V_1 = 5I.$$

<u>KVL</u> $-0.5V_1 - V_1 + 10\angle 30 = 0.$

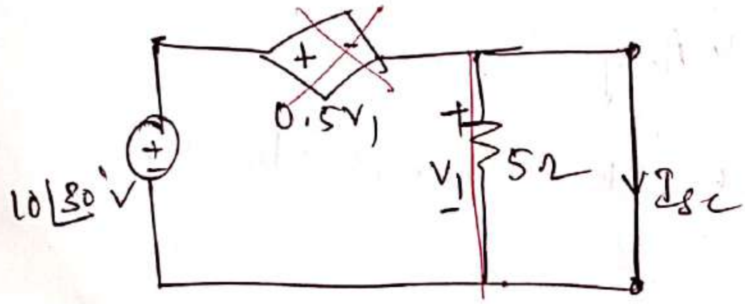
$$-1.5V_1 = -10\angle 30^\circ$$

$$V_1 = 6.67\angle 30^\circ \text{ volts}.$$

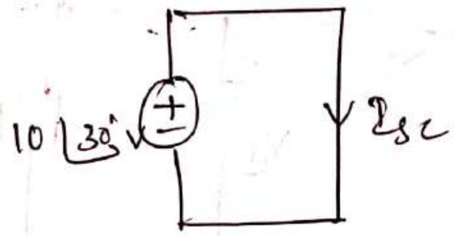
$$\therefore \boxed{V_{th} = 6.67\angle 30^\circ \text{ volts}}$$

<u>To find R_{th}</u>

(S.C the load terminals)



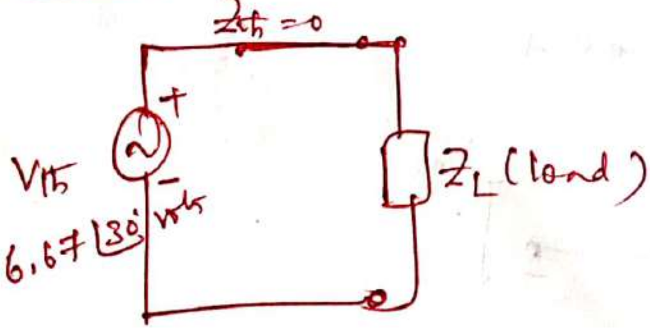
As there is a SC across 5Ω, $V_1 = 0$



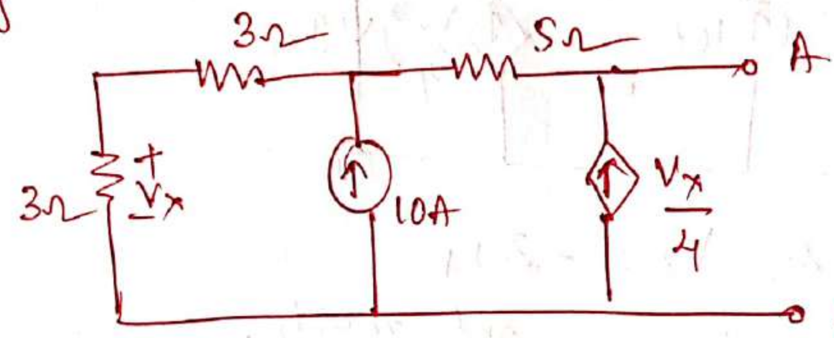
$$I_{sc} = \frac{10\angle 30^\circ}{0}$$

$$I_{sc} = \infty$$

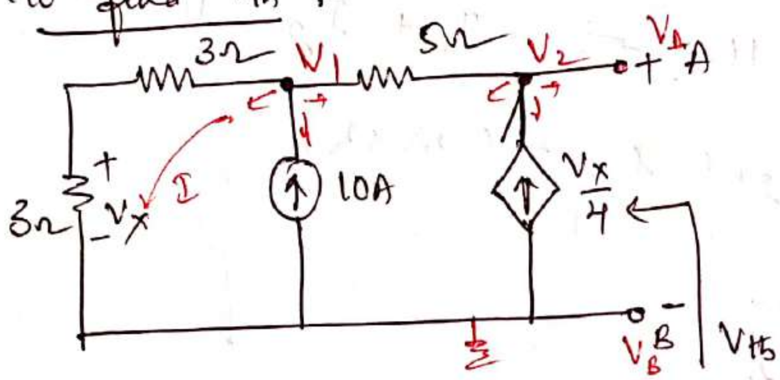
<u>Th. Eq ckt :-</u> $\therefore Z_{th} = \frac{V_{th}}{I_{sc}} = \underline{\underline{0\,\Omega}}$



4) Find the The eq of the n/w shown in fig



To find V_{th} :-



$V_{th} = V_A - V_B$

$\boxed{V_{th} = V_2}$

KCL @ V_1 :- $\frac{V_1}{6} - 10 + \frac{V_1 - V_2}{5} = 0$

$0.367 V_1 - 0.2 V_2 = 10$ —— ①

KCL @ V_2 $\frac{V_2 - V_1}{5} - \frac{V_x}{4} = 0$

But $V_x = 3I$ where $I = \frac{V_1}{6}$

$V_x = 3 \times V_1/6 = V_1/2 = 0.5V_1$

$0.2V_2 - 0.2V_1 - \frac{0.5V_1}{4} = 0$

$-0.325V_1 + 0.2V_2 = 0$ —— ②

$\boxed{V_1 = 238.1V}$ $\boxed{V_2 = 386.9 \text{ volts}}$ $\therefore \boxed{V_{th} = 386.9 \text{ volts}}$

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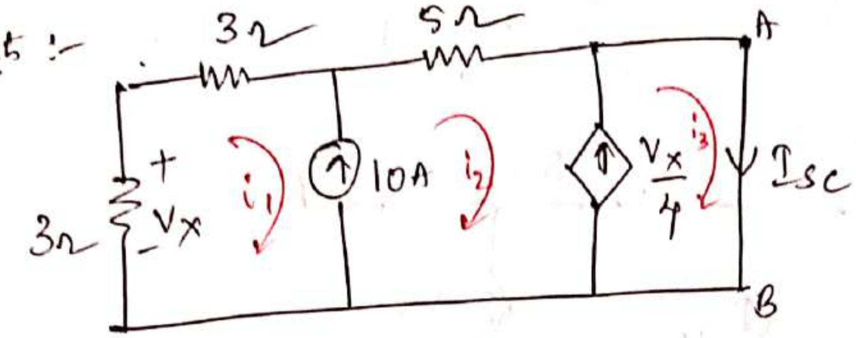
To find R_{th} :-



from the fig $I_{sc} = i_3$ & $V_x = -3I_1$

→ 10A is b/n 1st & 2nd mesh.

$I_2 - I_1 = 10 \Rightarrow -I_1 + I_2 = 10$ —— ①

→ $\frac{V_x}{4}$ is b/n 2nd & 3rd mesh.

$i_3 - i_2 = \frac{V_x}{4}$

$i_3 - i_2 = -3I_1/4$

$0.75 i_1 - i_2 + i_3 = 0$ —— ②

∴ mesh ①, ② & ③ forms supermesh.

$-3I_1 - 5i_2 - 3i_1 = 0$

$-6i_1 - 5i_2 = 0$ —— ③

Solve ①, ② & ③. $\boxed{I_1 = -4.545A}$

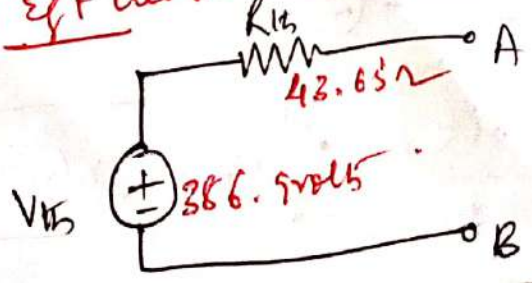
$\boxed{I_2 = 5.45}$ $\boxed{I_3 = 8.864A}$

$\boxed{I_{sc} = 8.864 \text{ Amp}}$

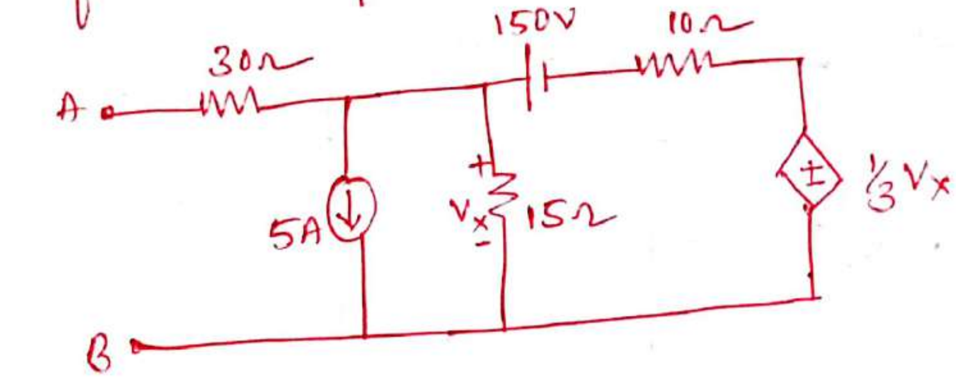
$Z_{th} = \frac{V_{th}}{I_{sc}} = \frac{386.9}{8.864}$

$\boxed{Z_{th} = 43.65\Omega}$

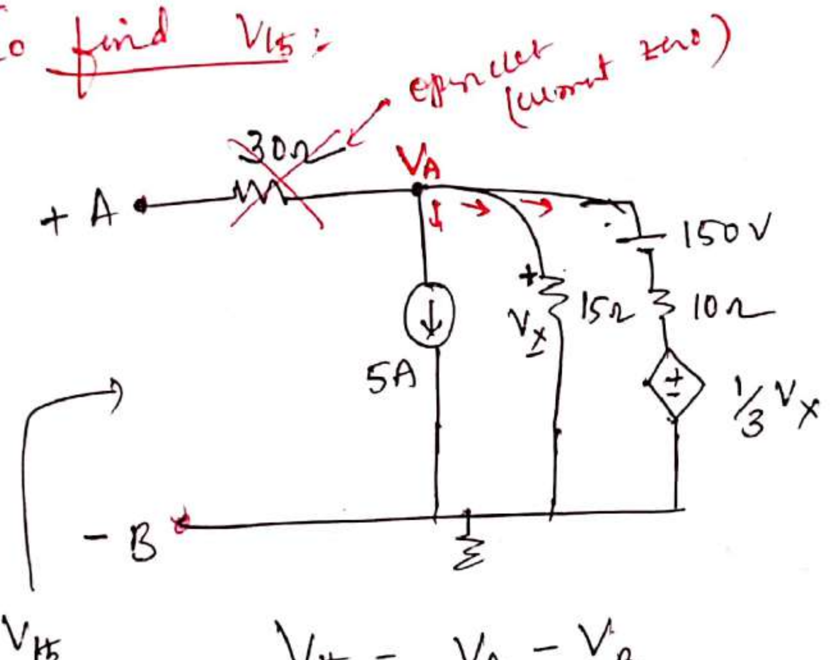
Th Eqt ckt :-



5) Calculate Thevenin's equivalent ckt across AB for the n/w shown below.



To find V_{th}:



$$V_{th} = V_A - V_B$$

KCL @ A:

$$5 + \frac{V_A}{15} + \frac{V_A - 150 - 0.33V_x}{10} = 0$$

from the fig $V_x = V_A$

$$5 + 0.066V_A + 0.1V_A - 15 - 0.033V_A = 0.$$

$$0.133V_A = 10$$

$$V_A = 75.18 \text{ volts}$$

$$V_{th} = 75.18 \text{ volts}$$

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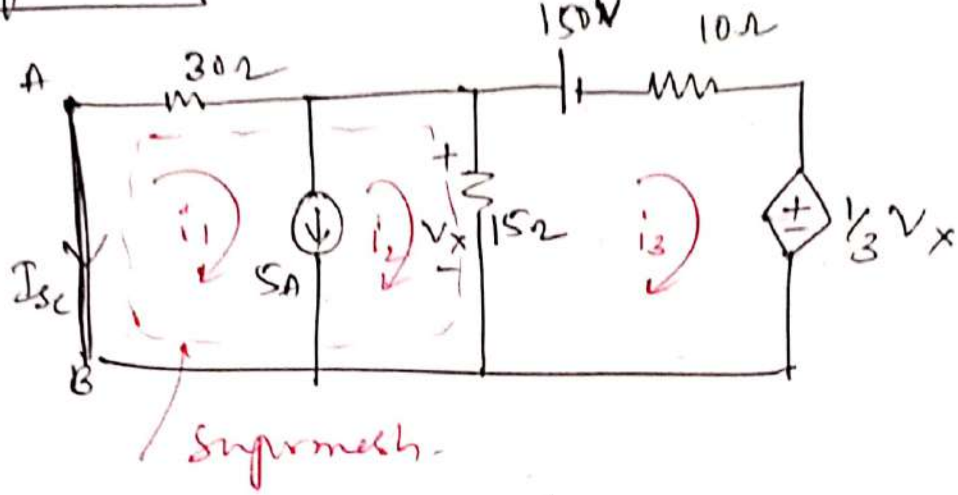
To find R_{th} :



from the supermesh

$$i_1 - i_2 = 5 \quad \text{——— (1)}$$

→ KVL to supermesh

$$-30i_1 - 15(i_2 - i_3) = 0$$

$$-30i_1 - 15i_2 + 15i_3 = 0 \quad \text{——— (2)}$$

→ KVL to 3rd loop.

$$-150 - 10i_3 - 0.33V_x - 15(i_3 - i_2) = 0$$

$$-150 - 10i_3 - 0.33V_x - 15i_3 + 15i_2 = 0$$

from the fig. $V_x = 15(i_2 - i_3)$

$$-150 - 25i_3 - 0.33 \times 15(i_2 - i_3) + 15i_2 = 0.$$

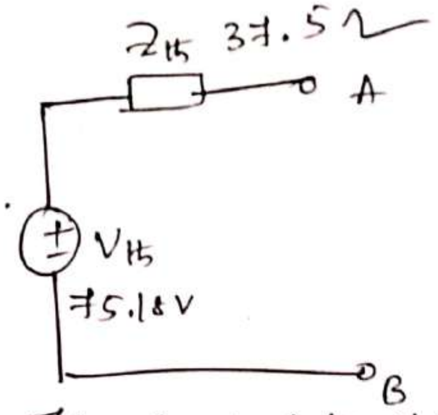
$$10i_2 - 20i_3 = 150 \quad \text{——— (3)}$$

$\boxed{i_1 = -2A}$ $\boxed{i_2 = -7A}$ $\boxed{i_3 = -11A}$

$\therefore I_{sc} = -I_1$

$\boxed{I_{sc} = 2A}$

$\therefore Z_{th} = \frac{V_{th}}{I_{sc}} = 37.5\Omega$.



Th Equivalent ckt.

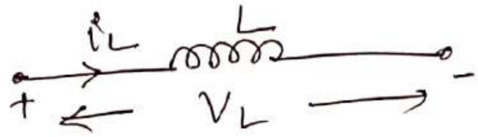
Norton's Theorem :-

Transient Behaviour & Initial Conditions

There are many reasons for studying initial & final conditions. The most important reason is that initial & final conditions evaluate the arbitrary constants in the general solution of differential equation.

* Initial and final conditions in elements :-

1) The Inductor :-



WKT voltage drop across inductor is $V_L = L\frac{di_L}{dt}$

for dc current, $\frac{di_L}{dt}$ becomes zero. Hence voltage across inductor is zero. Thus in steady state inductor acts as a short circuit.

Current through inductor is

$$i_L = \frac{1}{L}\int V_L\, dt$$

$$i_L = \frac{1}{L}\int_{-\infty}^{t} V_L\, dt$$

$$i_L = \frac{1}{L}\int_{-\infty}^{0^-} V_L\, dt + \frac{1}{L}\int_{0^-}^{t} V_L\, dt$$

At $t = 0^+$

$$i_L(0^+) = i_L(0^-) + \cancel{\frac{1}{L}\int_{0^-}^{0^+} V_L\, dt} \rightarrow 0$$

$$\boxed{i_L(0^+) = i_L(0^-)}$$

Thus, current through inductor cannot change instantaneously.

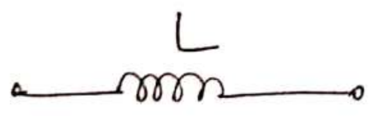
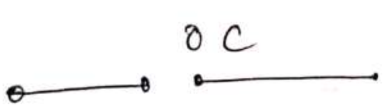
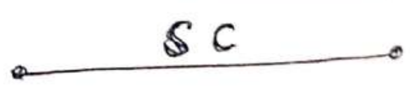
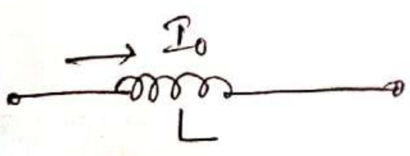
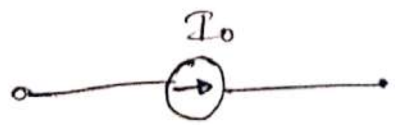
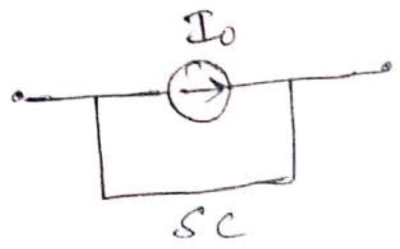
If $i_L(0^-) = 0$, then $i_L(0^+) = 0$. This means that at $t = 0^+$, inductor will act as an open circuit.

If $i_L(0^-) = I_0$, then $i_L(0^+) = I_0$, This means that @ $t = 0^+$, inductor acts as a current source I_0 Amp.

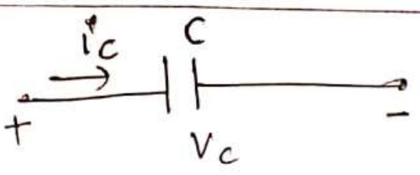
The final condition of the inductor is derived from

$$V_L = L \frac{di_L}{dt}$$

$\frac{di_L}{dt} = 0$ under steady state condn. Thus $V_L = 0$ & hence L acts as short circuit at $t = \infty$

Element	Equivalent ckt at $t=0^+$	Equivalent ckt at $t=\infty$
		
		

2) <u>The Capacitor</u> :-



WKT, $i_c = C \dfrac{dV_c}{dt}$

If dc vg is applied to capr, $\dfrac{dV_c}{dt}$ becomes zero. Thus current through capacitor becomes zero i.e., $\boxed{i_c = 0}$. Thus in <u>steady state</u> (dc) capacitor acts as <u>open circuit</u>.

$$\text{Now, } V_c = \frac{1}{C}\int_{-\infty}^{t} i_c \, dt.$$

$$V_c = \frac{1}{C}\int_{-\infty}^{0^-} i_c \, dt + \frac{1}{C}\int_{0^-}^{t} i_c \, dt$$

$$V_c = V_c(0^-) + \frac{1}{C}\int_{0^-}^{t} i_c \, dt.$$

@ $t = 0^+$

$$V_c(0^+) = V_c(0^-) + \cancel{\frac{1}{C}\int_{0^-}^{0^+} i_c \, dt}^{\,0}$$

$$\therefore \boxed{V_c(0^+) = V_c(0^-)}$$

Thus vg drop across <u>capr</u> cannot change instantaneously.

If $V_c(0^-)=0$, then $V_c(0^+)=0$. This means at $t=0^+$, capacitor C acts as a Short circuit

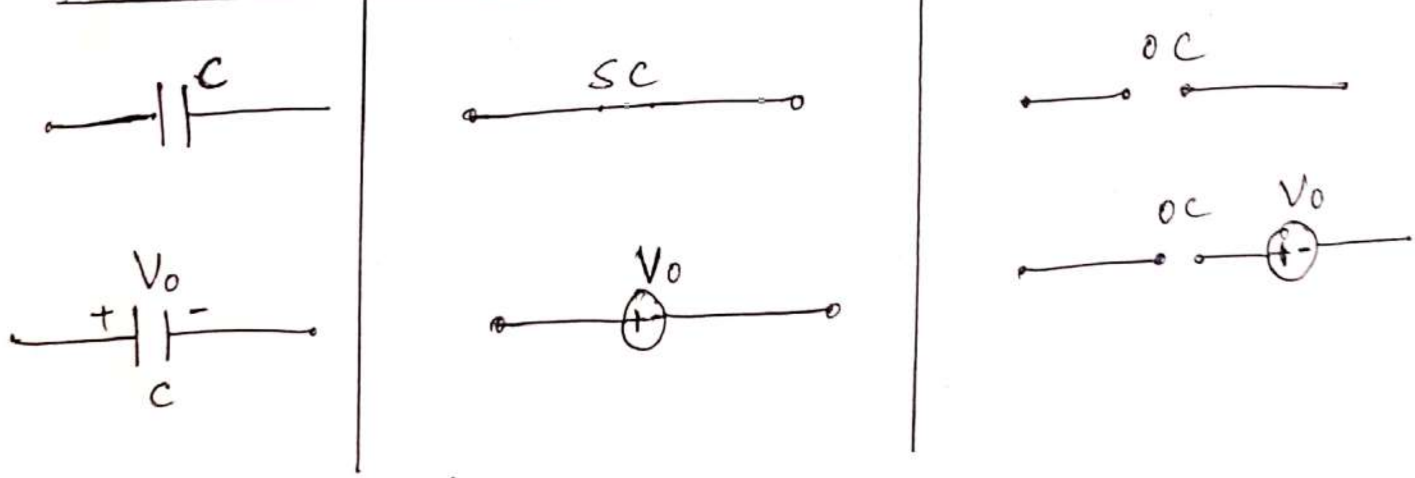
If $V_c(0^-)=V_0$ then $V_c(0^+)=V_0$, then C acts as vg source of V_0 volts.

Under steady state condition (dc) is @ $t=\infty$

$\rightarrow \quad i_c = C\dfrac{dV_c}{dt}$ ← is zero.

$\rightarrow \quad C = \dfrac{i_c}{0} = \infty$ Capacitor acts as open circuit @ $t=\infty$

Element	Equivalent ckt at $t=0^+$	Equivalent circuit at $t=\infty$



3) Resistor :- For a resistor, the relation b/w applied vg & resulting current is given by

$$V = i \cdot R$$

Above eqn is linear & time independent.

The behaviour of R at $t = 0^+$ & also at $t = \infty$ is same.

* <u>Initial Value theorem</u> :-

If $F(s)$ is the Laplace transform of $f(t)$, then, initial value theorem states that,

$$\lim_{t \to 0^+} f(t) = \lim_{s \to \infty} sF(s) \quad \text{——} (1)$$

The Laplace transform is very useful to find the initial value of the time function $f(t)$.

<u>Proof</u> :- WKT, the Laplace transform of the real differentiation,

$$\mathcal{L}\left\{\frac{df(t)}{dt}\right\} = sF(s) - f(0^-) \quad \text{——} (2)$$

Taking limit as $s \to \infty$ on both side,

$$\lim_{s \to \infty} \mathcal{L}\left\{\frac{df(t)}{dt}\right\} = \lim_{s \to \infty} \left[sF(s) - f(0^-)\right] \quad \text{——} (3)$$

By defn of L.T WKT $\mathcal{L}[f(t)] = \int_{0^-}^{\infty} e^{-st} f(t)\, dt$.

$$\lim_{s \to \infty} \mathcal{L}\left\{\frac{df(t)}{dt}\right\} = \lim_{s \to \infty} \int_{0^-}^{\infty} e^{-st} \left[\frac{df(t)}{dt}\right] dt$$

as $s \to \infty$ $e^{-st} = 0$

$\therefore$ LHS becomes zero of eqn (3)

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$$\therefore \quad 0 = \lim_{S\to\infty} \left[SF(s) - f(0^-) \right]$$

$$f(0^-) = \lim_{S\to\infty} SF(s)$$

But $f(0^-) = f(0^+)$ $\quad \therefore \quad f(0^+) = \lim_{S\to\infty} SF(s)$

$$\boxed{\lim_{t\to 0^+} f(t) = f(0^+) = \lim_{S\to\infty} SF(s)}$$

Final value theorem :-

The L.T is also useful to find the final value of the time function f(t). Thus if F(s) is the L.T of f(t) then the final value theorem states that,

$$\boxed{\lim_{t\to\infty} f(t) = \lim_{S\to 0} SF(s)} \qquad \text{--- (1)}$$

Proof :- Consider the L.T of the differentiation

$$L\left[\frac{df(t)}{dt}\right] = SF(s) - f(0^-) \qquad \text{--- (2)}$$

Taking limit as $s\to 0$ on both side.

$$\lim_{S\to 0}\left[L\,\frac{df(t)}{dt}\right] = \lim_{S\to 0}\left[SF(s) - f(0^-)\right] \qquad \text{--- (3)}$$

Consider LHS

$$\lim_{s\to 0} \mathcal{L}\frac{df(t)}{dt} = \lim_{s\to 0}\int_{0^-}^{\infty} e^{-st}\frac{df(t)}{dt}.dt$$

as $s\to 0$ $e^{-st} = 1$

$$= \int_{0^-}^{\infty}\frac{df(t)}{dt}.dt$$

$$= f(t)\Big|_{0^-}^{\infty}$$

$$= \lim_{t\to\infty}[f(t) - f(0^-)]$$

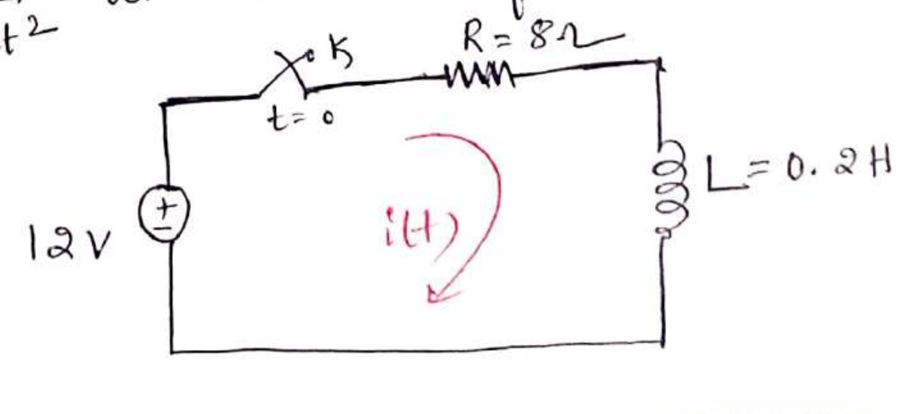
$\therefore$ eqn ③ becomes.

$$\lim_{t\to\infty}[f(t) - f(0^-)] = \lim_{s\to 0}[sF(s) - f(0^-)]$$

$$\boxed{\lim_{t\to\infty} f(t) = \lim_{s\to 0} sF(s)}$$

Problems :-

1) In the n/w, K is closed at t = 0 with zero current in the inductor. Find the values of i, $\frac{di}{dt}$, $\frac{d^2i}{dt^2}$ at $t = 0^+$. If $R = 8\Omega$, $L = 0.2H$.



Soln :- Switch is closed at $t=0$ means $t=0^+$

then Switch opens at $t=0^-$

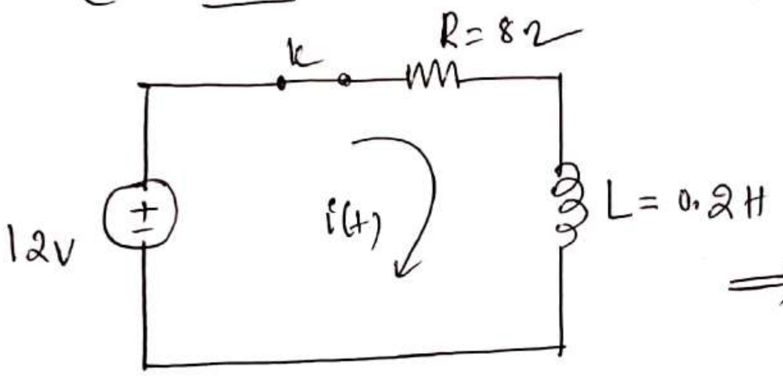
Given @ $t=0$ (i.e $t=0^+$) zero current

in the inductor.

i.e, $\boxed{i(0^+) = i(0^-) = 0}$

$i_L(0)$ means $i(0)$

@ $t=0^+$



KVL to loop

$$12 - 8\,i(t) - L\frac{di(t)}{dt} = 0 \quad \text{—(1)}$$

$$\Rightarrow 8\,i(t) + L\frac{di(t)}{dt} = 12$$

@ $t=0^+$ $i(0^+) = 0$

$$\therefore 0.2\frac{di}{dt} = 12$$

$$\frac{di}{dt} = \frac{12}{0.2} = 60\ A/sec$$

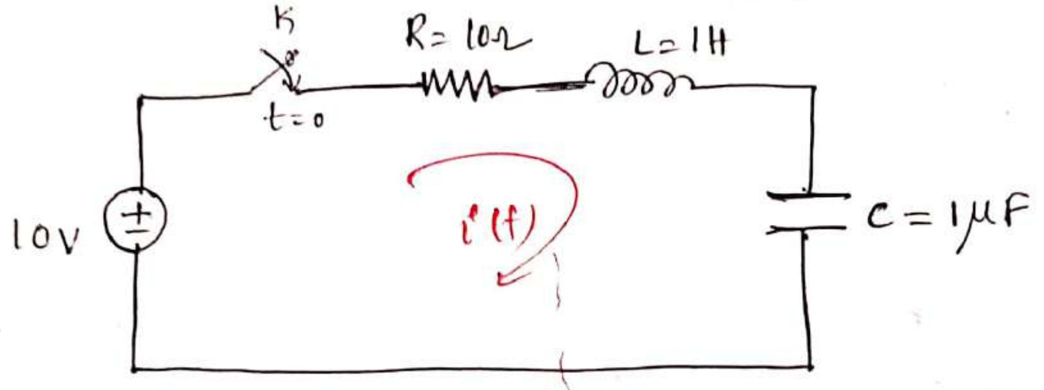
Differentiating Eqn (1)

$$-8\frac{di(t)}{dt} - L\frac{d^2i(t)}{dt^2} = 0$$

$$-8\times 60 - 0.2\frac{d^2i}{dt^2} = 0$$

$$\frac{d^2i}{dt^2} = -2400\ A/sec^2$$

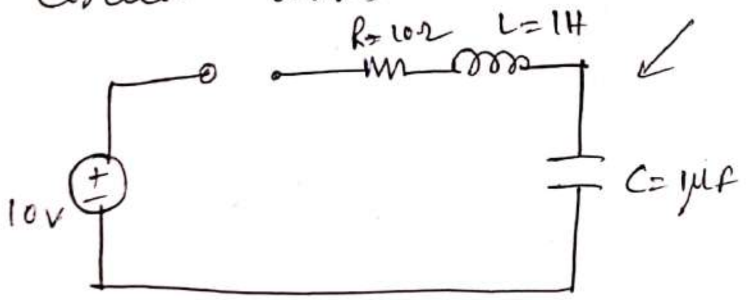
2) In the n/w shown, the switch is closed at $t=0$. Determine i, $\frac{di}{dt}$, $\frac{d^2i}{dt^2}$ at $t=0^+$.



→ In the problem it is not given. we have to indicate.

Given switch is closed at $t=0$
means $\underline{\underline{t=0^+}}$, then switch is opened

@ $\underline{\underline{t=0^-}}$.
When the switch is in opened condition,
Circuit looks like

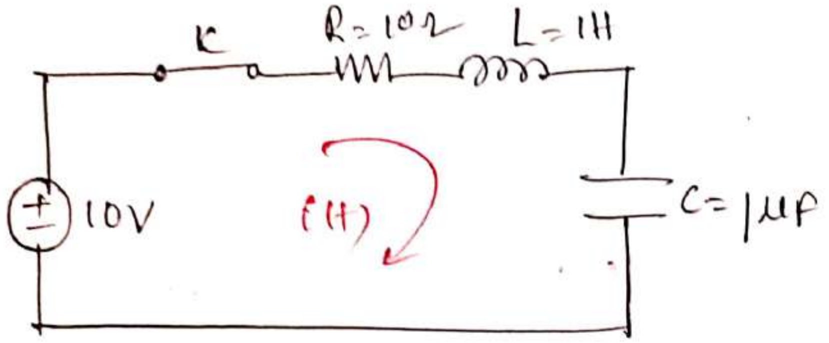


Open loop ∴ no current flows

∴ $\boxed{i(0^-) = i(0^+) = 0}$

& $\boxed{V_c(0^-) = V_c(0^+) = 0}$

@ $\underline{t=0^+}$ (switch is closed)



$V_c = \frac{1}{C}\int i(t)\,dt$

$V_L = L\frac{di}{dt}$

Apply KVL to loop.

$$10 - \underbrace{R\,i(t)}_{V_R} - \underbrace{L\frac{di}{dt}}_{V_L} - \underbrace{\frac{1}{C}\int i(t)\,dt}_{V_C} = 0 \quad \text{—— (1)}$$

or $$10 - R\,i(t) - L\frac{di}{dt} - V_c = 0$$

@ $t = 0^+$ $\quad i(0^+) = 0$ & $V_c(0^+) = 0$

$$\therefore \quad 10 - L\frac{di}{dt} = 0 \implies L\frac{di}{dt} = 10$$

$$\frac{di}{dt} = \frac{10}{L} = \frac{10}{1}.$$

$$\boxed{\frac{di}{dt} = 10\ A/sec}$$

Differentiating eqn (1)

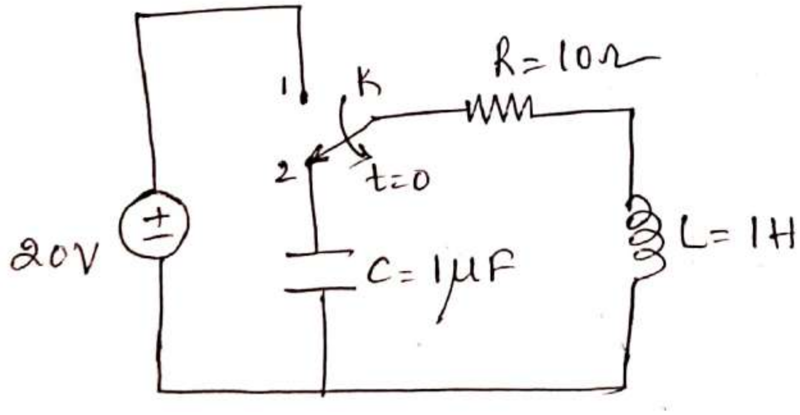
$$-R\frac{di}{dt} - L\frac{d^2i}{dt^2} - \cancel{\frac{i(t)}{C}} = 0$$

@ $t = 0^+$, $i(0^+) = 0$

$$-10 \times 10 - 1\,\frac{d^2i}{dt^2} = 0$$

$$-\frac{d^2i}{dt^2} = 100 \quad \text{or} \quad \boxed{\frac{d^2i}{dt^2} = -100\ A/sec^2}$$

3) The switch K is changed from position 1 to position 2 at $t=0$. Steady state cond^n has been reached in position 1. Find the values of i, $\frac{di}{dt}$ & $\frac{d^2i}{dt^2}$ at $t = 0^+$.

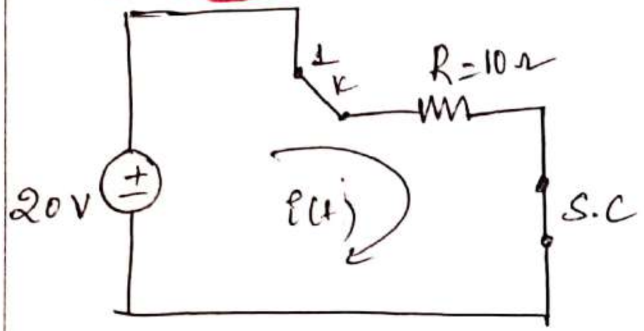


Given switch K is in position 2 at $t=0$ (i.e., $t = 0^+$)

means it is in position 1 at $t=0^-$

* Also in position 1 steady state cond^n is reached. WKT inductor acts as short ckt in this cond^n.

@ $(t=0^-)$



$$20 - 10\, i(t) = 0$$

$$i(t) = \frac{20}{10} = 2\,A$$

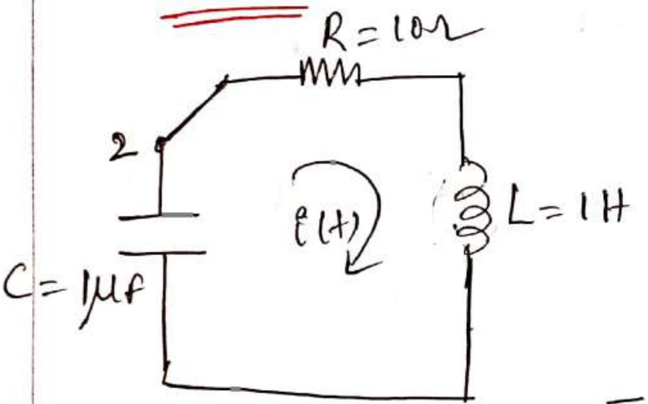
$$i_L \quad \boxed{i(0^-) = 2A}$$

WKT $\quad i(0^+) = i(0^-)$

$$\therefore \boxed{i(0^+) = i(0^-) = 2\,Amp}$$

Also $\boxed{V_c(0^-) = V_c(0^+) = 0}$ $\quad$ ($\because$ no vg across capr)

@ $(t=0^+)$



KVL to loop

$$-R\, i(t) - L\frac{di}{dt} - \underbrace{\frac{1}{C}\int i(t)\, dt}_{V_c} = 0 \quad \text{--- (1)}$$

$$-R\, i(t) - L\frac{di}{dt} - \cancel{V_c}^{\,0} = 0$$

@ $t=0^+$, $\quad i(0^+) = 2 \;\;\&\;\; v_c(0^+) = 0$

$$-10\times 2 - 1\frac{di}{dt} = 0$$

$$\boxed{\frac{di}{dt} = -20\ A/sec}$$

Diff. Eqn (1)

$$-R\frac{di}{dt} - L\frac{d^2 i}{dt^2} - \frac{i(t)}{C} = 0$$

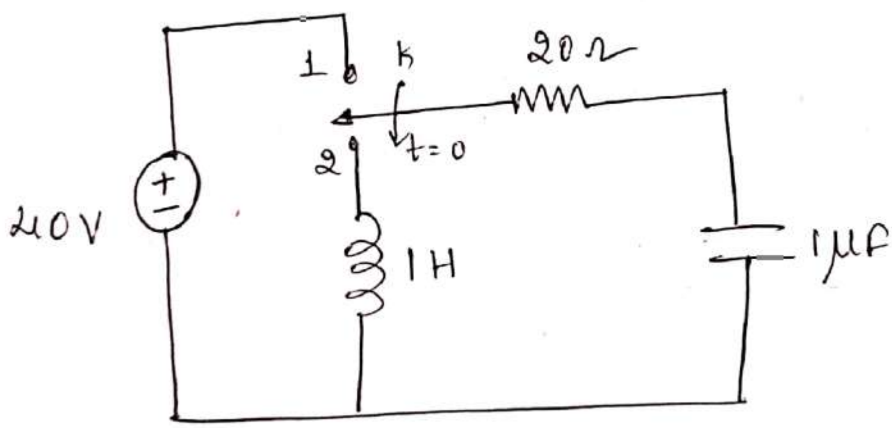
$i(0^+) = 2$

$$-10\times -20 - 1\frac{d^2 i}{dt^2} - \frac{2}{1\times 10^{-6}} = 0.$$

$$\frac{d^2 i}{dt^2} = 200 - 2\times 10^6$$

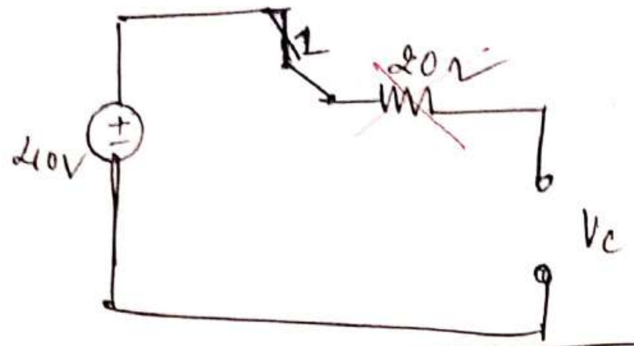
$$\boxed{\frac{d^2 i}{dt^2} \cong -2\times 10^6 \text{ A/sec}^2}$$

4) In the n/w, the switch is moved from position 1 to position 2 at $t=0$. The steady state reached before switching. Calculate i, $\frac{di}{dt}$ & $\frac{d^2 i}{dt^2}$ at $t=0^+$.



Given switch is in position 2 at $t=0$ (i.e. $t=0^+$) means in position 1 at $t=0^-$. Also steady state reached. WKT @ steady state capacitor acts as open circuit

($\because$ DC no current flows)



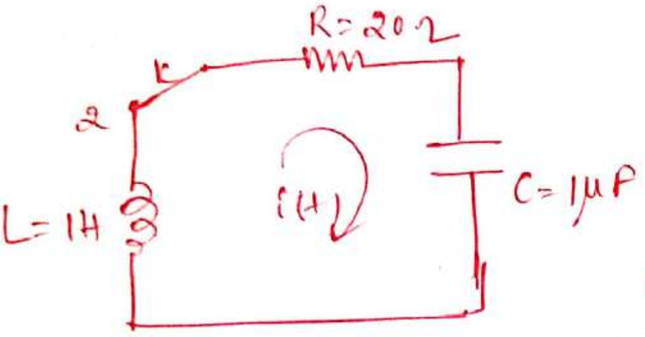
from the fig

$$\boxed{V_c = 40\ V}$$

$$\therefore \boxed{V_c(0^+) = V_c(0^-) = 40\ V}$$

Also $$\boxed{i(0^+) = i(0^-) = 0}$$

@ $t = 0^+$ switch in position 2



KVL to loop

$$-Ri(t) - \underbrace{\frac{1}{C}\int i(t)\,dt}_{V_c} - L\frac{di}{dt} = 0 \quad \text{——— (1)}$$

$$-R\overset{0}{i(t)} - V_c - L\frac{di}{dt} = 0$$

@ $t = 0^+$ $i(0^+) = 0$ & $V_c(0^+) = 40V$

$$-40 - 1\frac{di}{dt} = 0 \Rightarrow \boxed{\frac{di}{dt} = -40\ A/sec}$$

Diff eqn (1)

$$-R\frac{di}{dt} - \cancel{\frac{i(t)}{C}}^{\,0} - L\frac{d^2i}{dt^2} = 0$$

$$-20 \times -40 - 1\frac{d^2i}{dt^2} = 0$$

$$\boxed{\frac{d^2i}{dt^2} = 800\ A/sec^2}$$

-: Resonance :-

Resonance is defined as a phenomenon in which applied voltage & resulting current are in phase.

Resonance occurs in RLC circuit. During resonance phase angle between current & voltage is zero

i.e, $\phi = 0$

WKT Power factor $= \cos\phi$

$$pf = 1$$

$\therefore$ an AC circuit is said to be in resonance when the circuit P.f is Unity.

The resonant condition in ac circuit may be achieved,

1) By varying the frequency & the supply keeping the networks elements constant.

(or)

2) By varying L or C, keeping frequency constant.

Types of Resonance :-

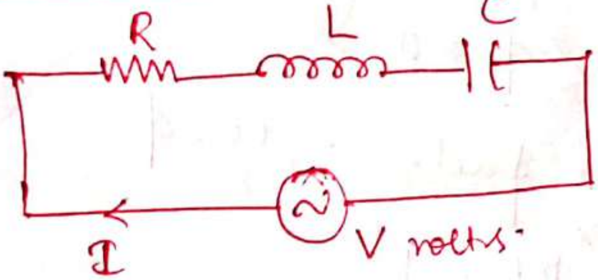
There are two types of resonance

i) Series resonance.

2) Parallel resonance.

Series resonance :-

Expression for resonant frequency in Series resonance :-



Consider a general RLC series circuit energised by a voltage source of V volts as shown in above figure.

The impedance of the circuit is given by

$$Z = R + j(X_L - X_C)$$

Where $X_L = 2\pi f L$ & $X_C = \dfrac{1}{2\pi f C}$

By varying supply frequency X_L is made equal to X_C

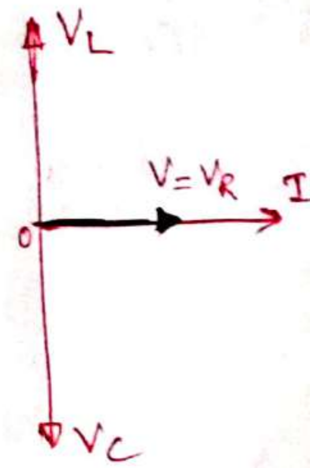
If $X_L = X_C$

Then $Z = R$

Current in phase with voltage.

$\rightarrow \phi = 0$

$\rightarrow Pf = 1$



Now the circuit is at resonance.

$\therefore$ At resonance.

$$X_L = X_C$$

$$2\pi f_0 L = \frac{1}{2\pi f_0 C} \qquad [f_0 = \text{resonant freq}].$$

$$(2\pi)^2 f_0^2 LC = 1$$

$$f_0^2 = \frac{1}{(2\pi)^2 LC}$$

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{LC}}}$$

$$2\pi f_0 = \frac{1}{\sqrt{LC}} \implies \boxed{\omega_0 = \frac{1}{\sqrt{LC}}}$$

Voltage magnification or figure of merit or quality factor or Q-factor :-

The ratio of voltage developed across inductor or capacitor to the applied voltage is called voltage magnification.

i.e, $Q = \frac{V_L \text{ or } V_C}{V}$

$\therefore \quad Q = \frac{V_L}{V} \quad$ or $\quad Q = \frac{V_C}{V}$

$Q = \frac{IX_L}{IR} \qquad Q = \frac{IX_C}{IR}$

$\boxed{Q = \frac{X_L}{R}} \qquad \boxed{Q = \frac{X_C}{R}}$

Q-factor of inductor $\qquad$ Q-factor of capacitor.

Expression for Q-factor in Series resonance $[Q_s]$:-

Q factor of series resonance is nothing but the Q-factor of inductor or Q-factor of capacitor.

Let Q_s be the Q-factor in series resonance, $\therefore Q_s = Q$

$Q_s = \frac{X_L}{R}$

$X_L = 2\pi f_0 L$

$X_L = \omega_0 L$

$$Q_s = \frac{\omega_0 L}{R} = \frac{1}{\sqrt{LC}} \times \frac{L}{R}$$

$$Q_s = \frac{1}{\cancel{\sqrt{L}}\sqrt{C}} \times \frac{\cancel{\sqrt{L}} \times \sqrt{L}}{R}$$

$$\boxed{Q_s = \frac{1}{R}\sqrt{\frac{L}{C}}}$$

Characteristics of Series resonant Circuit :-

At resonance,

1) $X_L = X_C$

2) The impedance of the circuit is minimum. & is equal to the resistance of the circuit

i.e, $\boxed{Z = R}$.

3) The current in the circuit is maximum & it is inphase with voltage.

$$\boxed{I = \frac{V}{R}}$$

4) The power factor is Unity.

i.e, $\boxed{Pf = 1}$.

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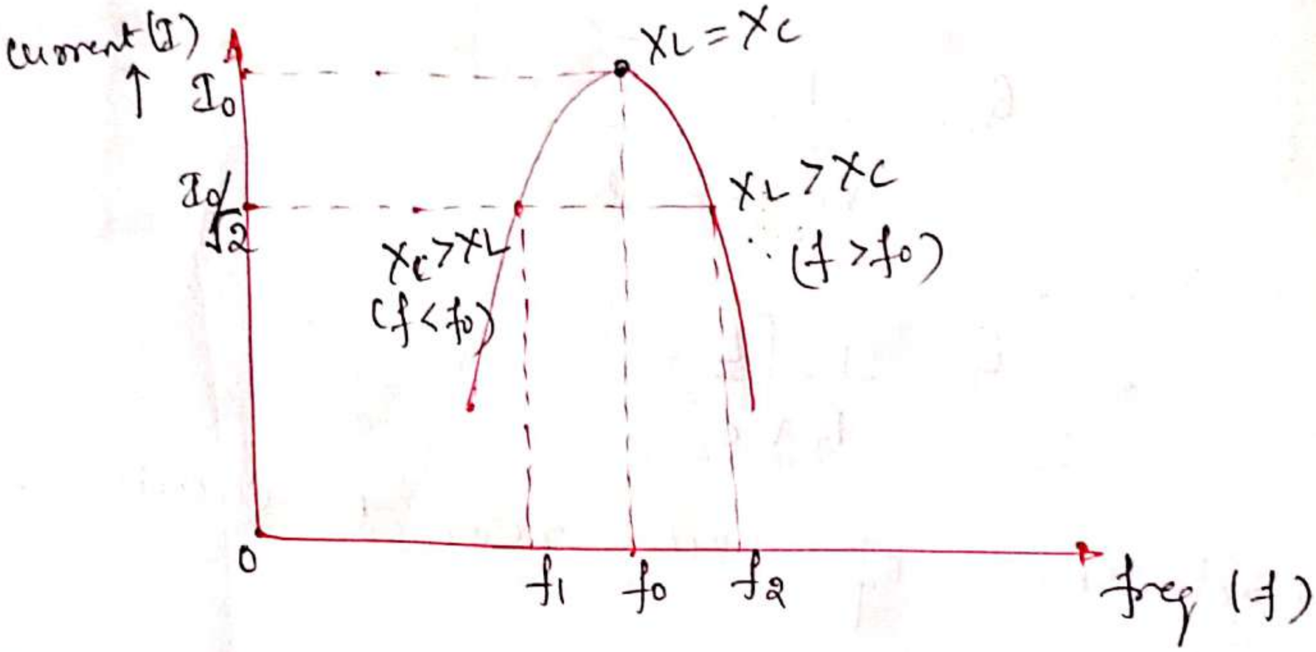
Frequency resonance curve of Series resonant Circuit :-



$I_0 \rightarrow$ maximum current or current @ resonance.

$f_1 \rightarrow$ Lower cut off frequency. }
$f_2 \rightarrow$ Upper cutoff frequency. } Half power frequency.

The power at resonance $= I_0^2 R \rightarrow$ maximum power.

If $I = \frac{I_0}{\sqrt{2}}$

then power $= I^2 R$

$$= \left(\frac{I_0}{\sqrt{2}}\right)^2 R$$

$$= \frac{I_0^2}{2} \times R = \frac{1}{2} \times I_0^2 R$$

$$= \frac{1}{2} \times \text{Maximum power}$$

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∴ The frequencies f_1 & f_2 corresponding to $\frac{I_0}{\sqrt{2}}$ or $0.707 I_0$ are called cut off frequencies or half power frequencies. Because the o/p power is reduced to half of the maximum power.

* Band width :-

The range or band of frequencies b/w f_1 & f_2 is called as Band width.

ie, $\boxed{\text{Band width} = \Delta f = f_2 - f_1}$

* Quality factor :-

Quality factor is defined as the ratio of resonant frequency to the band width.

i.e, $\boxed{Q = \frac{f_0}{B.W}}$

* Selectivity :-

It is the reciprocal of Quality factor.

i.e, $\text{Selectivity} = \frac{1}{Q}$.

$= \frac{1}{(f_0/B.W)} = \frac{B.W}{f_0}$

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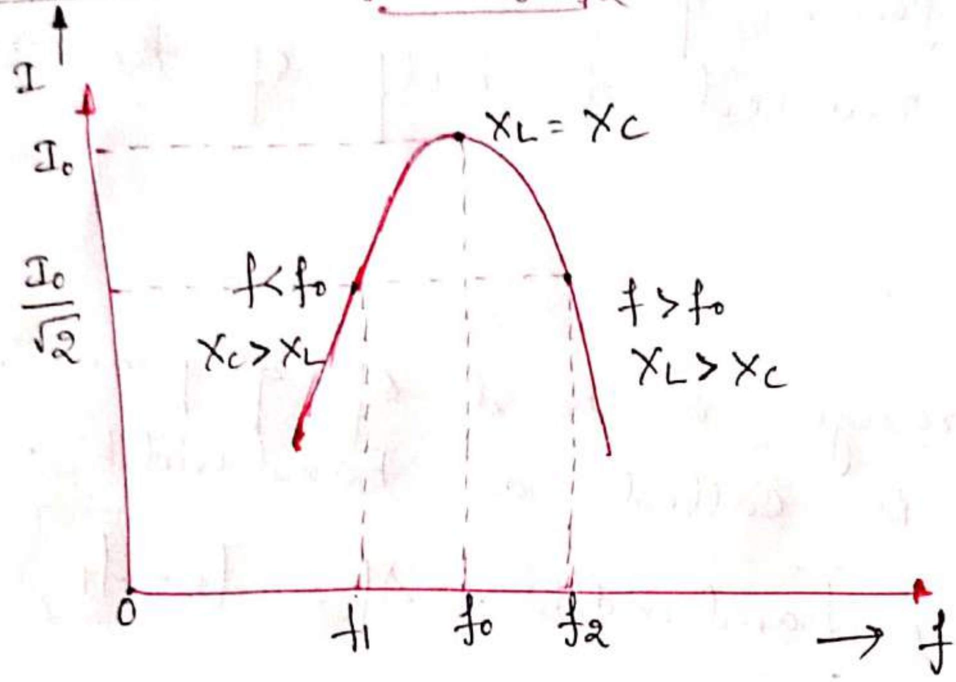
* Show that the resonant frequency is the geometric mean of the two half power frequencies i.e, $f_0 = \sqrt{f_1 . f_2}$



Let $X_{C_1} \rightarrow$ Capacitive reactance at f_1

$X_{C_2} \rightarrow$ Capacitive reactance at f_2.

$X_{L_1} \rightarrow$ Inductive reactance at f_1

$X_{L_2} \rightarrow$ Inductive reactance at f_2.

The impedance of RLC series resonant circuit at f_1 is

$$Z_1 = \sqrt{R^2 + (X_{C_1} - X_{L_1})^2} \quad (\because @ f_1 \; X_C > X_L)$$

The impedance of RLC series resonant circuit at f_2 is

$$Z_2 = \sqrt{R^2 + (X_{L_2} - X_{C_2})^2} \quad (\because @ f_2 \; X_L > X_C)$$

we have,

$$Z_1 = Z_2$$

$$\sqrt{R^2 + (X_{C1} - X_{L1})^2} = \sqrt{R^2 + (X_{L2} - X_{C2})^2}$$

$$\Rightarrow \cancel{R^2} + (X_{C1} - X_{L1})^2 = \cancel{R^2} + (X_{L2} - X_{C2})^2$$

$$\Rightarrow (X_{C1} - X_{L1})^{\cancel{2}} = (X_{L2} - X_{C2})^{\cancel{2}}$$

$$\Rightarrow X_{C1} - X_{L1} = X_{L2} - X_{C2}$$

$$X_{C1} + X_{C2} = X_{L2} + X_{L1} \quad \text{—— (1)}$$

But
$$\left.\begin{aligned} X_{C1} &= \frac{1}{2\pi f_1 C} = \frac{1}{\omega_1 C} \\ X_{C2} &= \frac{1}{2\pi f_2 C} = \frac{1}{\omega_2 C} \\ X_{L1} &= 2\pi f_1 L = \omega_1 L \\ X_{L2} &= 2\pi f_2 L = \omega_2 L \end{aligned}\right\} \quad \text{—— (2)}$$

Substituting (2) in eqn (1), we get

$$\frac{1}{\omega_1 C} + \frac{1}{\omega_2 C} = \omega_2 L + \omega_1 L$$

$$\frac{1}{C}\left[\frac{\cancel{\omega_2 + \omega_1}}{\omega_1 \omega_2}\right] = L\left[\cancel{\omega_1 + \omega_2}\right]$$

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$$\frac{1}{C\omega_1\omega_2} = L$$

or $\frac{1}{LC\omega_1\omega_2} = 1 \Rightarrow \frac{1}{LC} = \omega_1\omega_2$ —— (3)

WKT $\omega_0 = \frac{1}{\sqrt{LC}}$

or $\omega_0^2 = \frac{1}{LC}$

$\therefore$ eqn (3) becomes

$$\omega_0^2 = \omega_1\omega_2$$

$$\omega_0 = \sqrt{\omega_1\omega_2}$$

$$2\pi f_0 = \sqrt{2\pi f_1 \; 2\pi f_2}$$

$$2\pi f_0 = \sqrt{(2\pi)^2 f_1 f_2} \qquad \left(\sqrt{\cancel{(2\pi)^2}}\;\sqrt{f_1 f_2}\right)$$

$$\cancel{2\pi} f_0 = \cancel{2\pi}\sqrt{f_1 f_2}$$

$$\Rightarrow \boxed{f_0 = \sqrt{f_1 f_2}}$$

Expression for bandwidth or relationship b/w bandwidth & Q-factor:

Let f_1 & f_2 be the lower & upper half power frequencies & f_0 be the resonant frequency.

At f_1, $I = \dfrac{V}{\sqrt{R^2 + (X_{C_1} - X_{L_1})^2}}$ $\quad (\because @ f_1 \; X_C > X_L)$

Also @ f_1, $I = \dfrac{I_0}{\sqrt{2}}$ where $I_0 = \dfrac{V}{R}$

$$\frac{I_0}{\sqrt{2}} = \frac{V}{\sqrt{R^2 + (X_{C_1} - X_{L_1})^2}}$$

$$\frac{\cancel{V}}{\sqrt{2}R} = \frac{\cancel{V}}{\sqrt{R^2 + (X_{C_1} - X_{L_1})^2}}$$

$$\sqrt{R^2 + (X_{C_1} - X_{L_1})^2} = \sqrt{2}\,R$$

Squaring on B.S

$$R^2 + (X_{C_1} - X_{L_1})^2 = 2R^2$$

$$(X_{C_1} - X_{L_1})^2 = R^2$$

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$$X_{C1} - X_{L1} = R \quad \text{——— (1)}$$

@ f_2, $\quad I = \dfrac{V}{\sqrt{R^2 + (X_{L2} - X_{C2})^2}}$

Also @ f_2, $I = \dfrac{I_0}{\sqrt{2}}$, where $I_0 = \dfrac{V}{R}$

$$\frac{I_0}{\sqrt{2}} = \frac{V}{\sqrt{R^2 + (X_{L2} - X_{C2})^2}}$$

$$\frac{\cancel{V}}{\sqrt{2}\,R} = \frac{\cancel{V}}{\sqrt{R^2 + (X_{L2} - X_{C2})^2}}$$

$$\sqrt{R^2 + (X_{L2} - X_{C2})^2} = \sqrt{2}\,R$$

Squaring on both side

$$R^2 + (X_{L2} - X_{C2})^2 = 2R^2$$

$$(X_{L2} - X_{C2})^{\cancel{2}} = R^{\cancel{2}}$$

$$X_{L2} - X_{C2} = R \quad \text{——— (2)}$$

(1) + (2) gives,

$$X_{C1} - X_{L1} + X_{L2} - X_{C2} = 2R$$

$$X_{C1} - X_{C2} + X_{L2} - X_{L1} = 2R$$

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$$\frac{1}{\omega_1 C} - \frac{1}{\omega_2 C} + \omega_2 L - \omega_1 L = 2R$$

$$\frac{1}{C}\left[\frac{\omega_2 - \omega_1}{\omega_1 \omega_2}\right] + L(\omega_2 - \omega_1) = 2R$$

$$(\omega_2 - \omega_1)\left[\frac{1}{C\omega_1\omega_2} + L\right] = 2R$$

$$\omega_2 - \omega_1 = \frac{2R}{\left[\frac{1}{C\omega_1\omega_2} + L\right]} \qquad \frac{\div L}{\div L}$$

$$\omega_2 - \omega_1 = \frac{\frac{2R}{L}}{\frac{1}{C\omega_1\omega_2 L} + 1}$$

$$1$$

$$\omega_2 - \omega_1 = \frac{2R/L}{1+1} = \frac{\frac{2R}{L}}{2/1}$$

$$\omega_2 - \omega_1 = \frac{\cancel{2}R}{L} \times \frac{1}{\cancel{2}}$$

$$\omega_2 - \omega_1 = \frac{R}{L} \times \frac{\omega_0}{\omega_0}$$

$$\omega_2 - \omega_1 = \frac{\omega_0 R}{L\omega_0}$$

$$\omega_2 - \omega_1 = \frac{\omega_0}{L\omega_0/R} = \frac{\omega_0}{\frac{X_L}{R}}$$

$$Q$$

$$\omega_2 - \omega_1 = \frac{\omega_0}{Q}$$

$$f_2 - f_1 = \frac{f_0}{Q}$$

or $$\boxed{B.W = \frac{f_0}{Q}}$$

* Impedance of a Series resonant Circuit in terms of freq deviation (δ) :-

Frequency deviation (δ) is defined as the ratio of the difference b/w applied frequency or operating freq & resonant frequency.

i.e., $$\delta = \frac{f - f_0}{f_0} = \frac{\omega - \omega_0}{\omega_0}$$

where $f \rightarrow$ Operating frequency.

$f_0 \rightarrow$ Resonant frequency.

The impedance of series resonance circuit is

$$Z = R + j(X_L - X_C)$$

$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right)$$

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$$Z = R + \left[1 + j\left(\frac{\omega L}{R} - \frac{1}{\omega C R}\right)\right]$$

$$Z = R\left[1 + j\left(\frac{\omega L}{R} \times \frac{\omega_0}{\omega_0} - \frac{1}{\omega C R} \times \frac{\omega_0}{\omega_0}\right)\right]$$

$$Z = R\left[1 + j\left(\frac{\omega_0 L}{R} \times \frac{\omega}{\omega_0} - \frac{1}{\omega_0 C R} \times \frac{\omega_0}{\omega}\right)\right]$$

$$Z = R\left[1 + j\left(Q\frac{\omega}{\omega_0} - Q\frac{\omega_0}{\omega}\right)\right]$$

$$Z = R\left[1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right] \quad \text{—— ①}$$

WKT $\delta = \dfrac{\omega - \omega_0}{\omega_0}$

$$\delta = \frac{\omega}{\omega_0} - 1 \implies \frac{\omega}{\omega_0} = \delta + 1 \quad \text{— ②}$$

Substitute eqn ② in ① we get

$$Z = R\left[1 + jQ\left(\delta + 1 - \frac{1}{\delta + 1}\right)\right]$$

$$Z = R\left[1 + jQ\left(\frac{(\delta+1)^2 - 1}{\delta + 1}\right)\right]$$

$$Z = R\left[1 + jQ\left[\frac{\delta^2 + \cancel{1} + 2\delta - \cancel{1}}{\delta + 1}\right]\right]$$

$$Z = R\left[1 + jQ\left(\frac{\delta^2 + 2\delta}{\delta + 1}\right)\right]$$

$$Z = R\left[1 + jQ\,\frac{\delta(\delta+2)}{\delta+1}\right]$$

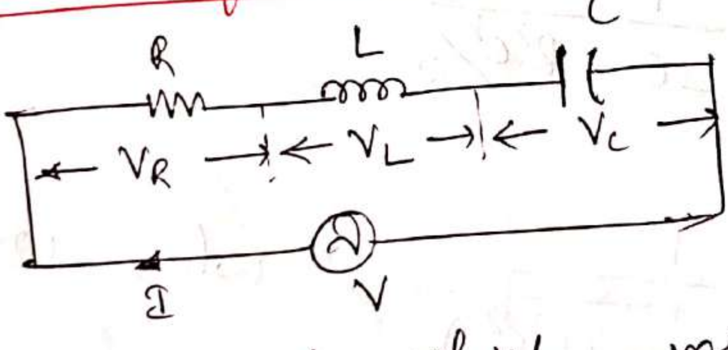
When δ is too small

$$\boxed{Z = R[1 + jQ\,2\delta]}$$

At resonance $\rightarrow$ $\delta = 0$

$$\therefore \boxed{Z = R}$$

* Expression for f_{Lmax} and f_{cmax} :-



Frequency at which voltage across the capacitor reaches its maximum is called f_{cmax}. V_{cmax} occurs earlier to f_0, for which $X_C > X_L$.

$$V_C = I X_C \implies V_C = \frac{V}{Z} \times \frac{1}{\omega C}$$

$$V_c = \frac{V}{\sqrt{R^2+(X_c-X_L)^2}} \times \frac{1}{\omega C}$$

Squaring on both side

$$V_c^2 = \frac{V^2}{R^2+\left(\frac{1}{\omega C}-\omega L\right)^2} \times \frac{1}{\omega^2 C^2}$$

$$L_p = \frac{V^2}{\omega^2 C^2}\left[\frac{1}{R^2+\frac{1}{\omega^2 C^2}+\omega^2 L^2 - 2\times\frac{1}{\cancel{\omega} C}\times\cancel{\omega} L}\right]$$

$$L_p = \frac{V^2}{\omega^2 C^2 R^2 + \omega^2 C^2\left(\frac{1}{\omega^2 C^2}+\omega^2 L^2 - 2\frac{L}{C}\right)}$$

$$V_c^2 = \frac{V^2}{\omega^2 C^2 R^2 + 1 + \omega^4 L^2 C^2 - 2\omega^2 LC}$$

$$V_c^2 = \frac{V^2}{\omega^2 C^2 R^2 + (\omega^2 LC - 1)^2}$$

V_c is max, when $\frac{dV_c^2}{d\omega} = 0$

$$\frac{dV_c^2}{d\omega} = \frac{\text{Denometir}\times 0 - V^2\{2\omega C^2 R^2 + 2(\omega^2 LC-1)\times 2\omega LC\}}{\{\omega^2 C^2 R^2 + (\omega^2 LC-1)^2\}^2} = 0$$

$$= -V^2\{2\omega C^2 R^2 + 2(\omega^2 LC-1)\times 2\omega LC\} = 0$$

As $V \neq 0$ $\quad 2\omega C^2 R^2 + 2(\omega^2 LC - 1)\times 2\omega LC = 0$

$$2\omega C\left[CR^2 + 2\omega^2 L^2 C - 2L\right] = 0$$

$$CR^2 + 2\omega^2 L^2 C - 2L = 0$$

$$\omega^2 = \frac{1}{LC} - \frac{R^2}{2L^2} \quad \text{or} \quad \omega = \sqrt{\frac{1}{LC} - \frac{R^2}{2L^2}}$$

$$f_{Cmax} = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{2L^2}}$$

f_{Lmax} is the freq at which V_{Lmax} occurs. V_{Lmax} occurs after f_0 for which $X_L > X_C$.

$$V_L = I X_L = \frac{V}{\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}} \times \omega L$$

$$V_L = \frac{V\omega L}{\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}} = \frac{V\omega L}{\sqrt{R^2 + \omega^2 L^2 + \frac{1}{\omega^2 C^2} - 2\times \omega L \times \frac{1}{\omega C}}}$$

$$= \frac{V\omega L \times \omega C}{\sqrt{\omega^2 C^2 R^2 + \omega^4 L^2 C^2 + 1 - 2\frac{L}{C}\omega^2 C^2}}$$

$$= \frac{V\omega L \times \omega C}{\sqrt{\omega^2 C^2 R^2 + (\omega^2 LC - 1)^2}}$$

$$V_L = \frac{V\omega^2 LC}{\sqrt{\omega^2 C^2 R^2 + (\omega^2 LC - 1)^2}}$$

Squaring on both side

$$V_L^2 = \frac{V^2 \omega^4 L^2 C^2}{\omega^2 C^2 R^2 + (\omega^2 LC - 1)^2}$$

V_L is max $\frac{dV_L^2}{d\omega} = 0$

$$\frac{dV_L^2}{d\omega} = \frac{\{\omega^2 C^2 R^2 + (\omega^2 LC - 1)^2\} \times 4\omega^3 V^2 L^2 C^2 - V^2 \omega^4 L^2 C^2 \{2\omega C^2 R^2 + 2(\omega^2 LC - 1) \times 2\omega LC\}}{\{\omega^2 C^2 R^2 + (\omega^2 LC - 1)^2\}^2} = 0$$

⑥

$$4\{\omega^2C^2R^2+(\omega^2LC-1)^2\}-\omega\{2\omega C^2R^2+4\omega^3L^2C^2-4\omega LC\}=0$$

$$=4\omega^2C^2R^2+4\cancel{\omega^4}L^2C^2+4-8\omega^2LC-2\omega^2C^2R^2-4\cancel{\omega^4L^2}C^2+4\omega^2LC=0$$

$$=\cancel{2\omega^2C^2R^2-2\omega^2C^2R^2}\quad 2\omega^2C^2R^2-4\omega^2LC+4=0$$

$$4\omega^2LC-2\omega^2C^2R^2=4$$

$$\omega^2=\frac{2}{2LC-C^2R^2}$$

$$\omega^2=\frac{1}{LC-\frac{R^2C^2}{2}}$$

$$\omega=\sqrt{\frac{1}{LC-\frac{R^2C^2}{2}}}$$

$$\boxed{f_{L\max}=\frac{1}{2\pi}\sqrt{\frac{1}{LC-\frac{R^2C^2}{2}}}}$$

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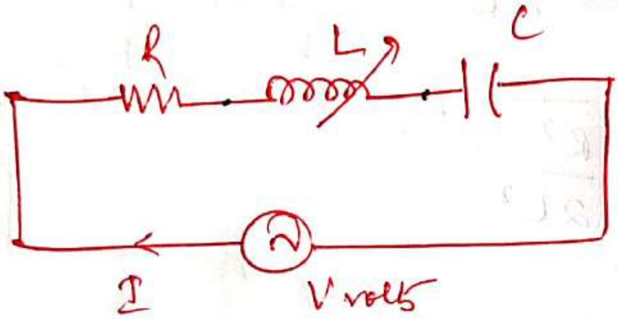
* Resonance by varying Circuit elements :-

Resonance can also be obtained by keeping f Constant & by varying L & C.

The resonance is made by varying L is termed as inductive tuning.



X_C remains unchanged since both f & C are fixed.

X_L varies as L varies since $X_L = 2\pi f L$

Let L_R denotes the inductance at resonance

$X_L = 2\pi f L$

WKT $V_L = I X_L$

$$V_L = \frac{V}{\sqrt{R^2 + (X_L - X_C)^2}} \times X_L$$

~~V_L is max if dX_L^2~~

Squaring ; $V_L^2 = \dfrac{V^2 X_L^2}{R^2 + (X_L - X_C)^2}$

V_L is max if $\frac{dV_L^2}{dX_L} = 0$

$$\frac{dV_L^2}{dX_L} = \frac{\left[R^2+(X_L-X_C)^2\right]V^2 \times 2X_L - V^2X_L^2\left(2(X_L-X_C)\right)}{\left\{R^2+(X_L-X_C)^2\right\}^2} = 0$$

$$\Rightarrow 2V^2X_L\left[R^2+X_L^2+X_C^2-2X_LX_C\right] - V^2X_L^2(2X_L-2X_C) = 0$$

$$\Rightarrow 2X_LV^2R^2 + \cancel{2V^2X_L^3} + 2V^2X_LX_C^2 - 4V^2X_L^2X_C - \cancel{2V^2X_L^3} + 2V^2X_L^2X_C = 0$$

$$\Rightarrow V^2(2X_LR^2 + 2X_LX_C^2 - 2X_L^2X_C) = 0$$

or $\quad 2X_LR^2 + 2X_LX_C^2 - 2X_L^2X_C = 0$

$$2X_L\left[R^2+X_C^2-X_LX_C\right] = 0$$

$$R^2+X_C^2 = X_LX_C$$

$$R^2+X_C^2 = \cancel{2\pi} fL \times \frac{1}{\cancel{2\pi} fC}$$

$$\boxed{L_R = C\left[R^2+X_C^2\right]}$$

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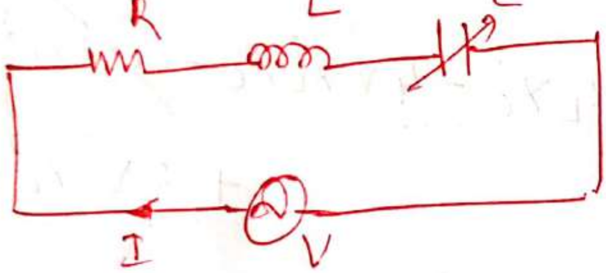
Resonance by varying Circuit elements :-

By varying Capacitance :-

S.T the value of the capacitor for maximum voltage across it in case of capacitive tuning of series resonance is $C_R = \frac{L}{R^2 + X_L^2}$



Let C_R denotes the capacitance at resonance.

Here X_L is fixed $\because$ f & L are fixed.

WKT, $V_C = I X_C$

$$V_C = \frac{V}{\sqrt{R^2 + (X_C - X_L)^2}} X_C$$

Squaring on both side.

$$V_C^2 = \frac{V^2 X_C^2}{R^2 + (X_C - X_L)^2}$$

Voltage across the cap is maximum i.e,

V_C is max. if $\frac{dV_C^2}{dX_C} = 0$

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$$\frac{dV_C^2}{dX_C} = \frac{[R^2+(X_C-X_L)^2]\times 2V^2X_C - V^2X_C^2[2(X_C-X_L)]}{[R^2+(X_C-X_L)^2]^2} = 0$$

$$\Rightarrow [R^2+X_C^2+X_L^2-2X_CX_L]2V^2X_C - 2X_C^3V^2 + 2V^2X_C^2X_L = 0$$

$$\Rightarrow 2V^2X_CR^2 + 2V^2X_C^3 + 2V^2X_CX_L^2 - 4V^2X_C^2X_L - 2V^2X_C^3 + 2V^2X_C^2X_L = 0$$

$$\Rightarrow 2V^2[R^2X_C + X_CX_L^2 - 2X_C^2X_L + X_C^2X_L] = 0$$

$$X_C[R^2+X_L^2-2X_CX_L+X_CX_L] = 0$$

$$\Rightarrow R^2+X_L^2-X_CX_L = 0$$

$$\Rightarrow R^2+X_L^2 = X_CX_L$$

$$\Rightarrow R^2+X_L^2 = \frac{1}{\cancel{2\pi}fC}\times\cancel{2\pi}fL$$

$$\Rightarrow \boxed{C_R = \frac{L}{R^2+X_L^2}}$$

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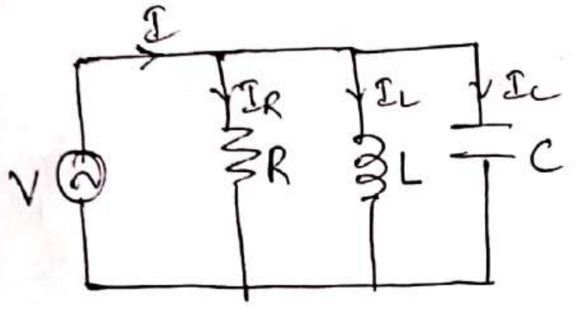
Parallel Resonance :-

1) General parallel resonance Circuit :-



WKT

$$I = I_R + I_L + I_C$$

(from KCL)

from KCL, $I = I_R + I_L + I_C$

$$\frac{V}{Z} = \frac{V}{R} + \frac{V}{jX_L} + \frac{V}{-jX_C}$$

$$\frac{1}{Z} = \frac{1}{R} - j\frac{1}{X_L} + j\frac{1}{X_C}$$

$$\frac{1}{Z} = \frac{1}{R} + j\left(\frac{1}{X_C} - \frac{1}{X_L}\right)$$

$$Y = G + jB$$

where $Y = \frac{1}{Z}$ → admittance

$G = \frac{1}{R}$ → Conductance

$B = \left(\frac{1}{X_C} - \frac{1}{X_L}\right)$ → Susceptance

At resonance the net susceptance is zero

i.e, $B = 0$

$$\frac{1}{X_C} - \frac{1}{X_L} = 0$$

$$\omega_0 C - \frac{1}{\omega_0 L} = 0$$

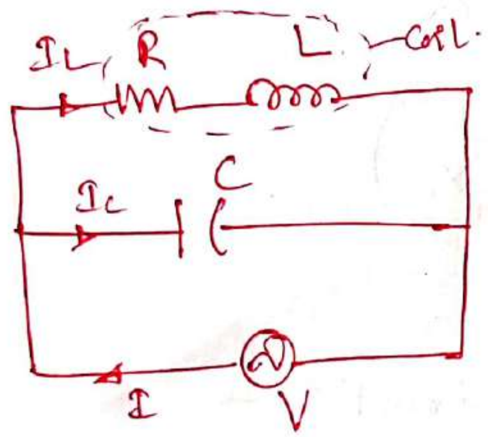
$$\omega_0 C = \frac{1}{\omega_0 L}$$

$$\omega_0^2 = \frac{1}{LC} \Rightarrow \omega_0 = \frac{1}{\sqrt{LC}}$$

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{LC}}}$$

..

2) Practical parallel resonance Circuit



The circuit consists of an inductive coil of resistance R Ω & inductance L Henry which is connected in ||lel with the capacitance C farad. This combo is connected across alternating supply.

$$I = I_L + I_C$$

$$\frac{V}{Z} = \frac{V}{R+jX_L} + \frac{V}{-jX_C}$$

$$\frac{1}{Z} = \frac{1}{R+jX_L} + \frac{j}{X_C}$$

$$\frac{1}{Z} = \frac{1}{R+jX_L} \times \frac{R-jX_L}{R-jX_L} + \frac{j}{X_C}$$

$$\frac{1}{Z} = \frac{R-jX_L}{R^2+X_L^2} + \frac{j}{X_C}$$

$$\frac{1}{Z} = \frac{R}{R^2+X_L^2} - \frac{jX_L}{R^2+X_L^2} + \frac{j}{X_C}$$

$$\frac{1}{Z} = \frac{R}{R^2+X_L^2} + j\left[\frac{1}{X_C} - \frac{X_L}{R^2+X_L^2}\right]$$

$$Y = G + jB$$

At resonance susceptance is zero. (i.e $B=0$)

$$\frac{1}{X_C} - \frac{X_L}{R^2+X_L^2} = 0$$

$$\frac{1}{X_C} = \frac{X_L}{R^2+X_L^2}$$

$$\cancel{\omega_0} C = \frac{\cancel{\omega_0} L}{R^2 + \omega_0^2 L^2}$$

$$R^2 + \omega_0^2 L^2 = \frac{L}{C}$$

$$\omega_0^2 L^2 = \frac{L}{C} - R^2$$

$$\omega_0^2 = \frac{L}{C \times L^2} - \frac{R^2}{L^2}$$

$$\omega_0^2 = \frac{1}{LC} - \frac{R^2}{L^2}$$

$$\omega_0 = \sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$\boxed{f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}}$$

@ resonance ($B=0$)

$$Y = \frac{R}{R^2 + X_L^2}$$

$$Y = \frac{R}{\underbrace{R^2 + \omega_0^2 L^2}_{L/C}}$$

$$Y = \frac{CR}{L}$$

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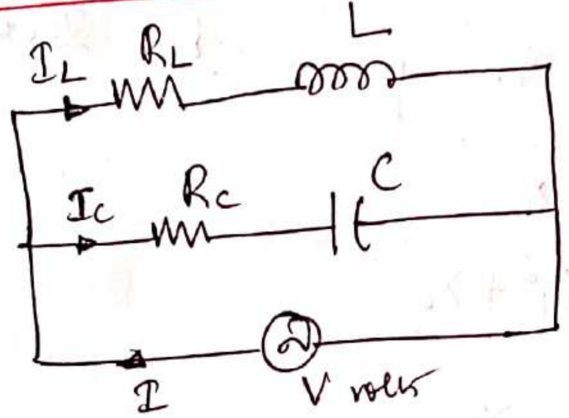
$Z = \frac{L}{RC}$ → which is called as dynamic impedance

$$\boxed{Z_d = \frac{L}{RC}}$$

3) Parallel resonance circuit when the resistance of the capacitor considered :-



$I_C = \frac{V}{Z}$

$= \frac{V}{R_C - jX_C}$

from the circuit

$$I = I_L + I_C$$

$$\frac{V}{Z} = \frac{V}{R_L + jX_L} + \frac{V}{R_C - jX_C}$$

$$\frac{\cancel{V}}{Z} = \cancel{V}\left[\frac{1}{R_L + jX_L} + \frac{1}{R_C - jX_C}\right]$$

$$\frac{1}{Z} = \frac{1}{R_L + jX_L} \times \frac{R_L - jX_L}{R_L - jX_L} + \frac{1}{R_C - jX_C} \times \frac{R_C + jX_C}{R_C + jX_C}$$

$$\frac{1}{Z} = \frac{R_L - jX_L}{R_L^2 + X_L^2} + \frac{R_C + jX_C}{R_C^2 + X_C^2}$$

$$\frac{1}{Z} = \frac{R_L}{R_L^2 + X_L^2} - \frac{jX_L}{R_L^2 + X_L^2} + \frac{R_C}{R_C^2 + X_C^2} + \frac{jX_C}{R_C^2 + X_C^2}$$

$$\frac{1}{Z} = \frac{R_L}{R_L^2 + X_L^2} + \frac{R_C}{R_C^2 + X_C^2} + j\left[\frac{X_C}{R_C^2 + X_C^2} - \frac{X_L}{R_L^2 + X_L^2}\right] \quad (1)$$

$$Y = G + jB.$$

At resonance net susceptance is zero (i.e, $B = 0$)

$$\frac{X_C}{R_C^2 + X_C^2} - \frac{X_L}{R_L^2 + X_L^2} = 0$$

$$\frac{X_C}{R_C^2 + X_C^2} = \frac{X_L}{R_L^2 + X_L^2}$$

$$X_C(R_L^2 + X_L^2) = X_L(R_C^2 + X_C^2)$$

$$\frac{1}{\omega_0 C}(R_L^2 + \omega_0^2 L^2) = \omega_0 L\left(R_C^2 + \frac{1}{\omega_0^2 C^2}\right)$$

$$\frac{1}{LC}(R_L^2 + \omega_0^2 L^2) = \omega_0^2\left(R_C^2 + \frac{1}{\omega_0^2 C^2}\right)$$

$$\frac{R_L^2}{LC} + \omega_0^2 \frac{L}{C} = \omega_0^2 R_C^2 + \frac{1}{C^2}$$

$$\frac{R_L^2}{LC} - \frac{1}{C^2} = \omega_0^2 R^2 - \omega_0^2 \frac{L}{C}$$

$$\frac{R_L^2}{LC} - \frac{1}{C^2} = \omega_0^2\left(R_C^2 - \frac{L}{C}\right)$$

or $$\omega_0^2 = \frac{\frac{R_L^2}{LC} - \frac{1}{C^2}}{R_C^2 - \frac{L}{C}}$$

$$\omega_0^2 = \frac{\frac{1}{LC}\left(R_L^2 - \frac{L}{C}\right)}{\left(R_C^2 - L/C\right)}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}\sqrt{\frac{R_L^2 - L/C}{R_C^2 - L/C}}$$

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{R_L^2 - L/C}{R_C^2 - L/C}}}$$

Impedance at resonance :-

$$Y_0 = \frac{R_L}{R_L^2 + X_L^2} + \frac{R_C}{R_C^2 + X_C^2}$$ (from (1))

$$Z_0 = \frac{1}{Y_0}$$

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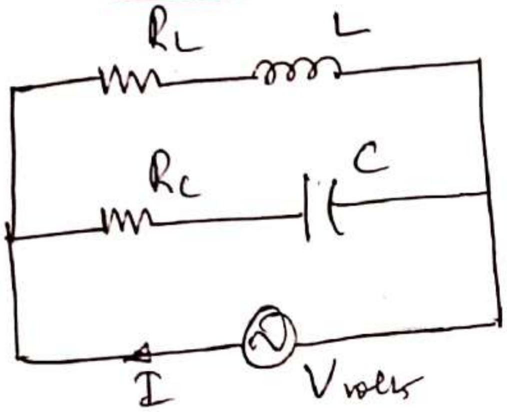
Current at resonance

$$I_0 = \frac{V}{Z_0} = V Y_0 = V\left[\frac{R_L}{R_L^2+X_L^2} + \frac{R_C}{R_C^2+X_C^2}\right]$$

* S.T the parallel ckt is resonant at all frequencies if $R_L = R_C = \sqrt{\frac{L}{C}}$



WKT,

$$f_0 = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{R_L^2 - L/C}{R_C^2 - L/C}}$$

if $R_L = R_C$ then

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

@ resonance (B = 0)

$$\frac{X_C}{R^2+X_C^2} - \frac{X_L}{R_L^2+X_L^2} = 0$$

$$\frac{X_C}{R_C^2+X_C^2} = \frac{X_L}{R_L^2+X_L^2}$$

$$\frac{\frac{1}{\omega_0 C}}{R_C^2+\frac{1}{\omega_0^2 C^2}} = \frac{\omega_0 L}{R_L^2+\omega_0^2 L^2}$$

$$\frac{\omega_0 C}{\omega_0^2 C^2 R_C^2 + 1} = \frac{\omega_0 L}{R_L^2 + \omega_0^2 L^2}$$

$$\cancel{\omega_0} C \left[R_L^2 + \omega_0^2 L^2 \right] = \cancel{\omega_0} L \left[\omega_0^2 C^2 R_C^2 + 1 \right]$$

$$\frac{C R_L^2}{LC} + \frac{\omega_0^2 L^2 C}{LC} = \frac{\omega_0^2 C^2 R_C^2 L}{LC} + \frac{L}{LC} \qquad \div LC$$

$$\frac{R_L^2}{L} + \omega_0^2 L = \omega_0^2 C R_C^2 + \frac{1}{C}$$

$$\text{Given } R_L = R_C = \sqrt{L/C}$$

$$R_L^2 = R_C^2 = L/C$$

$$\frac{\cancel{L}}{\cancel{L}C} + \omega_0^2 L = \omega_0^2 \cancel{C} \times \frac{L}{\cancel{C}} + \frac{1}{C}$$

$$\therefore \boxed{\frac{1}{C} + \omega_0^2 L = \frac{1}{C} + \omega_0^2 L}$$

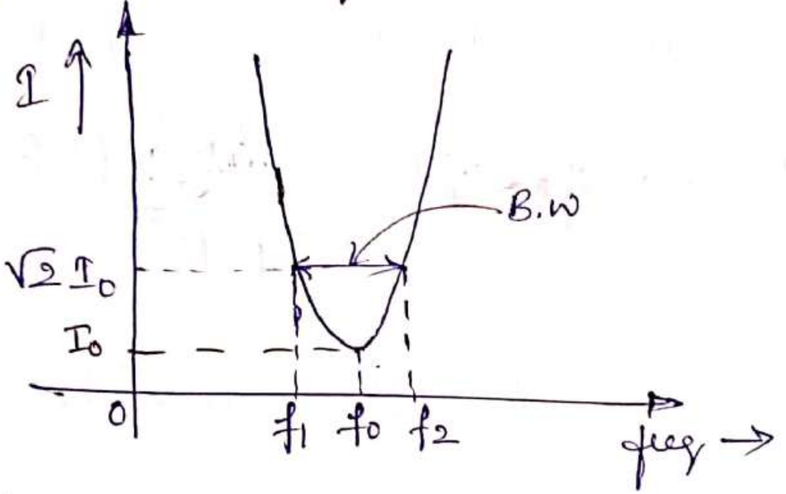
Hence whatever the value of ω_0,

RHS = LHS.

Any change in the value of ω_0 equally affects both sides.

In other words, the circuit is resonant at all frequencies.

Frequency response of parallel resonance circuit:-



Since the current at resonance is minimum the circuit is called as <u>antiresonant</u> <u>circuit</u> or <u>rejector circuit</u>.

Also, the impedance of the $\parallel^{el}$ resonance circuit is <u>max</u> @ resonance.

The <u>chars</u> of the $\parallel^{el}$ resonant circuit are,

1) The impedance at resonance will be purely resistive & will be maximum.

2) Total current in the circuit is minimum & will be in phase with the applied <u>vg</u>.

3) The power factor at resonance will be unity.
4) Parallel resonance circuit is known as antiresonance ckt
5) Impedance at resonance is known as dynamic resistance (Z_d)

Comparison between Series and parallel resonance

Parameter	Series Circuit	Parallel circuit
1) Impedance	$Z = R$ minimum	$Z_d = \frac{L}{CR}$ maximum
2) Power factor	unity	unity
3) Resonance freq	$f_0 = \frac{1}{2\pi\sqrt{LC}}$	$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$
4) Current at resonance	Current is maximum at resonance, $I_0 = \frac{V}{R}$ & will be in phase with the applied vg	Current is minimum at resonance $I_0 = \frac{V}{Z_d}$ & will be in phase with the applied voltage.

Series Resonance

Note :- 1) $f_0 = \frac{1}{2\pi\sqrt{LC}}$ Resonant frequency.

$$\left.\begin{array}{l} 2)\ Z = R \\ 3)\ X_L = X_C \\ 4)\ I_0 = \frac{V}{R} \end{array}\right\}$$ @ resonance ;

5) $Q = \frac{X_L}{R} = \frac{\omega_0 L}{R} = \frac{2\pi f_0 L}{R}$

6) $Q = \frac{X_C}{R} = \frac{1}{\omega_0 C R}$

7) $B.W = \frac{f_0}{Q}$ & $B.W = f_2 - f_1$

8) $V_C = I X_C$ & $V_L = I X_L$

9) $f_{Lmax} = \frac{1}{2\pi}\sqrt{\frac{1}{LC - \frac{R^2C^2}{2}}}$

10) $f_{Cmax} = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{2L^2}}$

11) $f_0 = \sqrt{f_1 f_2}$

12) $f_1 = f_0 - \frac{R}{4\pi L}$ & $f_2 = f_0 + \frac{R}{4\pi L}$

Problems :-

1) A series RLC circuit has $R = 10\Omega$, $L = 0.1\,H$ & $C = 100\mu F$ is connected across 200 V variable freq source. Find i) f_0 ii) Z at this freq.
iii) Vg drop across L & C @ this freq.
iv) Q-factor v) B.W vi) The freq @ which voltage across inductor is max.
vii) the freq at which vg across capacitor is max.

Given :-

$R = 10\Omega$

$L = 0.1H$

$C = 100\mu F$

$V = 200V$

i) $f_0 = ?$

ii) Z @ f_0

iii) V_L & V_C @ f_0

iv) Q v) B.W

vi) $f_{Lmax} = ?$

vii) $f_{Cmax} = ?$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{0.1 \times 100 \times 10^{-6}}}$$

$$\boxed{f_0 = 50.32 Hz}$$

$$\boxed{Z = R = 10\Omega}$$

$$V_L = I X_L = \frac{V}{R} \times 2\pi f_0 L$$

$$V_L = \frac{200}{10} \times 2\pi \times 50.32 \times 0.1$$

$$\boxed{V_L = 632.33 V}$$

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$V_C = I X_C$

$$V_C = \frac{V}{R} \times \frac{1}{2\pi f_0 C} = \frac{200}{10} \times \frac{1}{2\pi \times 50.32 \times 100 \times 10^{-6}}$$

$$V_C = 632.57 \text{ volts}$$

or $V_L = V_C = 632.57$ volts

$$Q = \frac{X_L}{R} = \frac{2\pi f_0 L}{R} = 3.16$$

$$Q = 3.16$$

$$B.W = \frac{f_0}{Q} \Rightarrow B.W = 15.92 \text{ Hz}$$

$$f_{L\max} = \frac{1}{2\pi} \sqrt{\frac{1}{LC - \frac{R^2 C^2}{2}}}$$

$$f_{L\max} = 51.63 \text{ Hz}$$

$$f_{C\max} = \frac{1}{2\pi} \sqrt{\frac{1}{LC} - \frac{R^2}{2L^2}}$$

$$f_{C\max} = 49.05 \text{ Hz}$$

2) A series RLC circuit consists of 50Ω resistance $0.2H$ inductance & capacitance of $10\mu F$ with an apply vg of 20V. Determine i) Resonant freq. ii) Q-factor iii) Upper & lower cutoff freq & also find the B.W.

Given.

$R = 50\Omega$

$L = 0.2H$

$C = 10\mu F$

$V = 20V$

i) $f_0 = ?$

ii) $Q = ?$

iii) f_1 & $f_2 = ?$

iv) $B.W = ?$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$f_0 = \frac{1}{2\pi\sqrt{0.2 \times 10 \times 10^{-6}}}$$

$$\boxed{f_0 = 112.54 \text{ Hz}}$$

$$Q = \frac{X_L}{R} = \frac{2\pi f_0 L}{R}$$

$$Q = \frac{2\pi \times 112.54 \times 0.2}{50}$$

$$\boxed{Q = 2.82}$$

$$f_1 = f_0 - \frac{R}{4\pi L} = 94.39 \text{ Hz} \qquad \boxed{f_1 = 94.39 \text{ Hz}}$$

$$f_2 = f_0 + \frac{R}{4\pi L} = 134.18 \text{ Hz} \qquad \boxed{f_2 = 134.18 \text{ Hz}}$$

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$\therefore$ $B.W = f_2 - f_1$ or $B.W = \dfrac{f_0}{Q}$

$$\boxed{B.W = 39.79\,Hz}$$

$$B.W = \frac{112.54}{2.82} = 39.9\,Hz$$

3) A Series RLC circuit consists of $R = 10\Omega$, $L = 0.01H$ & $C = 0.01\mu F$ is connected across a supply of 10 mV. Determine.

i) f_0 ii) B.W iii) Q iv) I_0 v) f_1 & f_2.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$f_0 = \frac{1}{2\pi\sqrt{0.01 \times 0.01 \times 10^{-6}}}$$

$$\boxed{f_0 = 15.91\,KHz}$$

$$Q = \frac{X_L}{R} = \frac{2\pi f_0 L}{R}$$

$$\boxed{Q = 99.96}$$

$$Q = \frac{f_0}{B.W} \qquad \boxed{B.W = \frac{f_0}{Q} = 159.16\,Hz}$$

$$f_1 = f_0 - \frac{R}{4\pi L} \qquad \boxed{f_1 = 15.83\,KHz}$$

$$f_2 = f_0 + \frac{R}{4\pi L}$$

$$f_2 = 15.91 \times 10^3 + \frac{10}{4\pi \times 0.01}$$

$$\boxed{f_2 = 15.99\ KHz}$$

$$I_0 = \frac{V}{R} = \frac{10 \times 10^{-3}}{10}$$

$$\boxed{I_0 = 1m\ Amp}$$

4) A coil of resistance 20Ω & inductance 10mH is in series with a capacitance & is supplied with a constant voltage, variable freq source. The maximum current is 2A at 1000 Hz. Find the cut off frequencies.

Given:

$R = 20\Omega$

$L = 10 \times 10^{-3} H$.

$I_0 = 2A$

$f_0 = 1000\ Hz$

$f_1 = ?$

$f_2 = ?$

WKT,

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$f_0^2 = \frac{1}{4\pi^2 LC}$$

$$C = \frac{1}{4\pi^2 L f_0^2}$$

$$\boxed{C = 2.53\ \mu F}$$

$$f_1 = f_0 - \frac{R}{4\pi L}$$

$$f_1 = 1000 - \frac{20}{4\pi \times 10 \times 10^{-3}}$$

$$\boxed{f_1 = 854.02\ Hz}$$

$$f_2 = f_0 + \frac{R}{4\pi L}$$

$$f_2 = 1000 + \frac{20}{4\pi \times 10 \times 10^{-3}}$$

$$\boxed{f_2 = 1172.33\ Hz}$$

5) An RLC series ckt draws a maximum current of 15A when connected to 230V - 50Hz supply. If the Q-factor is 5, find the parameters of the circuit.

Given.

$I_0 = 15A$

$f_0 = 50 Hz$

$V = 230V$

$Q = 5$

$R = ?$ $L = ?$

$C = ?$

WKT, $I_0 = \frac{V}{R}$

$$R = \frac{V}{I_0} = 15.33\Omega$$

$$\boxed{R = 15.33\Omega}$$

$$\rightarrow Q = \frac{X_L}{R}$$

$$X_L = Q R$$

$$2\pi f_0 L = Q . R. \longrightarrow L = \frac{Q \times R}{2\pi f_0} = \frac{5 \times 15.33}{2\pi \times 50}$$

$$\boxed{L = 0.24 H}$$

$$\rightarrow Q = \frac{X_C}{R}$$

or $X_C = Q R$

$$\frac{1}{2\pi f_0 C} = Q R \Rightarrow C = \frac{1}{2\pi f_0 Q R}$$

$$\boxed{C = 41.52 \mu F}$$

6) An RLC series circuit has $R = 50\Omega$, $L = 0.5 H$ & $C = 20\mu F$. If a constant voltage of 200V at variable fq is applied. Find the frequency at which resonance occurs. Also find the max vg drop across L & C.

Given:

$R = 50\Omega$

$L = 0.5 H$

$C = 20 \mu F$

WKT.

$$f_0 = \frac{1}{2\pi \sqrt{LC}}$$

$$f_0 = \frac{1}{2\pi \sqrt{0.5 \times 20 \times 10^{-6}}}$$

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$$\boxed{f_0 = 50.33\ Hz}$$

To find V_{Lmax} :-

$$f_{Lmax} = \frac{1}{2\pi}\sqrt{\frac{1}{LC - \frac{R^2C^2}{2}}}$$

$$f_{Lmax} = 51.63\ Hz$$

$$V_{Lmax} = I X_L$$

$$= \frac{V}{Z} X_L$$

$$= \frac{V}{\sqrt{R^2 + (X_L - X_C)^2}} \times X_L$$

Now X_L & X_C @ f_{Lmax}

$$X_L = 2\pi f_{Lmax} L \qquad X_C = \frac{1}{2\pi f_{Lmax} C}$$

$$= 2\pi \times 51.63 \times 0.5$$

$$= 162.2\,\Omega \qquad X_C = 154.13\,\Omega$$

$$\therefore V_{Lmax} = \frac{200}{\sqrt{50^2 + (162.2 - 154.13)^2}} \times 162.2$$

$$\boxed{V_{Lmax} = 640.54\ \text{volts}}$$

To find V_{Cmax} :-

$$f_{Cmax} = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{2L}}$$

$$f_{Cmax} = 49.69 \text{ Hz}$$

X_L & X_C @ f_{Cmax}

$$X_L = 2\pi f_{Cmax} L \qquad X_C = \frac{1}{2\pi f_{Cmax} C}$$

$$X_L = 156.12\,\Omega \qquad X_C = 160.13\,\Omega$$

$$V_{Cmax} = I X_C$$

$$= \frac{V}{Z} X_C$$

$$= \frac{V}{\sqrt{R^2 + (X_C - X_L)^2}} X_C$$

$$= \frac{200}{\sqrt{R^2 + (160.13 - 156.12)^2}} \times 160.12$$

$$\boxed{V_{Cmax} = 638.46 \text{ volts}}$$

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Exlra

$$I_0 = \frac{V}{R} = \frac{200}{50} = 4 \text{ Amp.}$$

$V_L = I_0 X_L$

$= I_0 \times 2\pi f_0 L$

$= 4 \times 2\pi \times 50.33 \times 0.5$

$\boxed{V_L = 632.46 \text{ volts}}$

$V_c = I_0 X_c$

$= I_0 \times \frac{1}{2\pi f_0 C}$

$\boxed{V_C = 632.46 \text{ volts}}$

$\boxed{X_L = X_C}$ @ resonance.

$X_L = X_C = 158.115\ \Omega$

7) A voltage of $100\sqrt{2} \sin \omega t$ is applied to an RLC series circuit. At resonance freq, the vg across the inductor is 500V, the B.W is 50Hz. The impedance at resonance is 75Ω, find f_0 & constants of the circuit.

Given :-

$V = 100\sqrt{2} \sin \omega t$

At f_0, $V_L = 500$ volts.

B.W = 50 Hz.

$Z = R = 75\Omega$

$f_0 = ?$

R, L & C = ?

$V = \underbrace{100\sqrt{2}}_{V_m} \sin \omega t$

$V_{rms} = \frac{V_m}{\sqrt{2}} = 100$ volts

$\therefore \boxed{V = V_{rms} = 100 \text{ volts}}$

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$$Q = \frac{V_L}{V} = \frac{500}{100}$$

$$\boxed{Q = 5}$$

WKT $Q = \frac{f_0}{B.W}$

$$f_0 = 5 \times 50$$

$$\boxed{f_0 = 250\ Hz}$$

At resonance $Z = R = 75\,\Omega$

$$\boxed{R = 75\,\Omega}$$

$$Q = \frac{X_L}{R} \qquad Q = \frac{X_C}{R}$$

$$X_L = QR \qquad \frac{1}{2\pi f_0 C} = QR$$

$$2\pi f_0 L = QR$$

$$L = \frac{QR}{2\pi f_0} \qquad C = \frac{1}{2\pi f_0 QR}$$

$$L = \frac{5 \times 75}{2\pi \times 250} \qquad C = \frac{1}{2\pi \times 250 \times 5 \times 75}$$

$$\boxed{L = 0.23\ H} \qquad \boxed{C = 1.69\ \mu F}$$

8) A voltage of $E = 100 \sin \omega t$ is applied to an RLC series circuit at resonant freq, the vg across the capacitor found to be 400V. The B.W is 75 Hz, the impedance at resonance is 100Ω. Find the resonant freq & the constants of the circuit.

Given:-

$E = 100 \sin \omega t$

$V_C = 400V$

$B.W = 75 Hz$

$Z = R = 100\Omega$

$f_0 = ?$

$R, L, C = ?$

Given, $E = 100 \sin \omega t$

$E_m = V_m = 100$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{100}{\sqrt{2}}$$

$V_{rms} = 70.71$ volts

$$Q = \frac{V_C}{V} = \frac{400}{70.71} = 5.65.$$

WKT $$Q = \frac{f_0}{B.W}$$

$f_0 = 5.65 \times 75 = 423.75 Hz$

$$\boxed{f_0 = 423.75 Hz}$$

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$$Q = \frac{X_L}{R}$$

$$X_L = QR$$

$$2\pi f_0 L = QR$$

$$L = \frac{5.65 \times 100}{2\pi \times 423.75}$$

$$\boxed{L = 0.21\ H}$$

$$Q = \frac{X_C}{R}$$

$$QR = \frac{1}{2\pi f_0 C}$$

$$C = \frac{1}{2\pi f_0 QR}$$

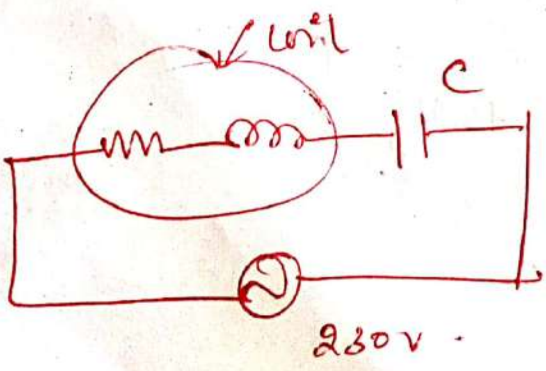
$$C = \frac{1}{2\pi \times 423.75 \times 5.65 \times 100}$$

$$\boxed{C = 0.66\ \mu F}$$

$$\boxed{Z = R = 100\ \Omega}$$

9) A coil of resistance 20Ω & inductance 1 H is connected in series with a capacitor. The resonant freq is 100 rad/sec. If the supply is 230V - 50Hz, find the

i) Line current 2) P.f 3) voltage across the coil & cap.



$R = 20\Omega$

$L = 1H$

$\omega_0 = 100 rad/sec$

$V = 230V$, 50Hz

$I = ?$

p.f = ?

$V_{coil} = ?$

To find line current,

$$I = \frac{V}{Z}$$

$$I = \frac{V}{\sqrt{R^2 + (X_L - X_C)^2}}$$

$$I = \frac{230}{\sqrt{20^2 + (314.15 - 31.83)^2}} = 0.812A$$

WKT, $X_L = 2\pi f L$

$X_L = 2\pi \times 50 \times 1$

$$\boxed{X_L = 314.15\Omega}$$

$$X_C = \frac{1}{2\pi f C}$$

$$X_C = \frac{1}{2\pi \times 50 \times 100\mu}$$

$$\boxed{X_C = 31.83\Omega}$$

WKT, $\omega_0 = \frac{1}{\sqrt{LC}}$

$$\omega_0^2 = \frac{1}{LC}$$

$$C = \frac{1}{L\omega_0^2} = 100\mu F$$

$$\therefore \boxed{I = 0.812 \text{ Amp}}$$

$$\text{Power factor} = \frac{R}{Z}$$

$$= \frac{20}{\sqrt{R^2 + (X_L - X_C)^2}} = \frac{20}{\sqrt{20^2 + (314.15 - 31.83)^2}}$$

$$\boxed{P.f = 0.07}$$

Vg across the coil.

$$V_{coil} = I_{coil} \times Z_{coil}$$

$$Z_{coil} = \sqrt{R^2 + X_L^2}$$

$$= \sqrt{20^2 + (314.15)^2}$$

$$= 314.79\,\Omega$$

$$V_{coil} = 0.812 \times 314.79$$

$$\boxed{V_{coil} = 255.6 \text{ volts}}$$

$$V_C = I X_C$$

$$= 0.812 \times 31.83$$

$$\boxed{V_C = 25.84 \text{ volts}}$$

10) A 220 V, 100 Hz AC source supplies a series RLC circuit with a capr & a coil. If the coil has 50 mΩ resistance & 5 mH inductance, find at a resonant frq of 100 Hz what is the value of capacitor. Also calculate the Q-factor & half power frequencies of the circuit.

Given.

$V = 220$ volts

$f = 100$ Hz

$R = 50\, m\Omega$

$L = 5\, mH$

At $f_0 = 100$ Hz.

$C = ?$

$Q = ?$

f_1 & $f_2 = ?$

WKT

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C}}$$

Squaring

$$C = \frac{1}{4\pi^2 L f_0^2}$$

$$C = \frac{1}{4\pi^2 \times 5\times10^{-3} \times (100)^2}$$

$$\boxed{C = 506.6\,\mu F}$$

$$Q = \frac{X_L}{R}$$

$$Q = \frac{2\pi f_0 L}{R}$$

$$\boxed{Q = 62.83}$$

$$f_1 = f_0 - \frac{R}{4\pi L}$$

$$f_1 = 100 - \frac{50\times10^{-3}}{4\pi \times 5\times10^{-3}}$$

$$\boxed{f_1 = 99.20\text{ Hz}}$$

$$f_2 = f_0 + \frac{R}{4\pi L}$$

$$f_2 = 100 + \frac{50\times10^{-3}}{4\pi\times5\times10^{-3}}$$

$$\boxed{f_2 = 100.8\text{ Hz}}$$

11) A series RLC circuit has a resistance of 10Ω an inductance of 0.3H & a capce of $100\mu F$. The applied vg is 230V. Find i) f_0 ii) Q iii) lower & upper cut off fs iv) B.W v) Current at resonance vi) Currents at f_1 & f_2 vii) vg across inductance at resonance.

given

$R = 10\Omega$

$L = 0.3H$

$C = 100\mu F$

$V = 230V$

$f_0 =$

$Q =$

$f_1 =$

$f_2 =$

$B.W =$

$I_0 =$

Current at f_1 & f_2

@ f_1 $I = \frac{I_0}{\sqrt{2}} =$

$V_L = I_0 X_L$

$L_0 = I_0 \times 2\pi f_0 L$

$V_L =$

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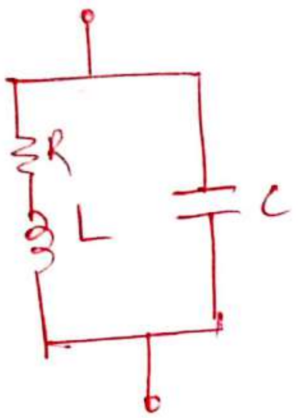
1) If $R = 25\Omega$, $L = 0.5H$ & $C = 5\mu F$, find the ω_0, f_0, Q & B.W for the circuit shown below.



WKT,

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{0.5\times 5\mu} - \frac{25^2}{(0.5)^2}}$$

$$f_0 = 100.58 \text{ Hz}$$

$$\omega_0 = 2\pi f_0$$

$$= 2\pi \times 100.58$$

$$\omega_0 = 631.96 \text{ rad/sec}$$

$$Q = \frac{\omega_0 L}{R}$$

$$Q = \frac{631.96 \times 0.5}{25}$$

$$Q = 12.64$$

$$B.W = \frac{f_0}{Q}$$

$$B.W = \frac{100.58}{12.64}$$

$$B.W = 50 \text{ rad/sec}$$

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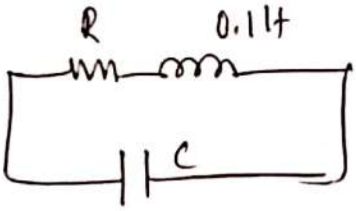
2) In the ckt given, an inductance of 0.1H having a Q-factor of 5 is in ||lel with a capr. Determine the value of capacitor & coil resistance at resonant fq of 500 rad/sec.



$$Q = \frac{X_L}{R}$$

$R = ?$

$C = ?$

$W_0 = 500$ rad/sec

$L = 0.1H$

$Q = 5$

$$R = \frac{X_L}{Q} = \frac{W_0 L}{Q}$$

$$R = \frac{500 \times 0.1}{5}$$

$$\boxed{R = 10\Omega}$$

WKT,

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$W_0^2 = \frac{1}{LC} - \frac{R^2}{L^2}$$

$$\frac{1}{LC} = W_0^2 + \frac{R^2}{L^2}$$

$$\frac{1}{C} = L\left[W_0^2 + \frac{R^2}{L^2}\right] = 0.1\left[500^2 + \frac{10^2}{0.1^2}\right]$$

$$\boxed{C = 38.46\,\mu F}$$

3) A coil of 20Ω resistance has an inductance of $0.2H$ & is connected in $\|^{el}$ with $100\mu F$ capr. Cal the freq at which the circuit will act as a non-inductive resistance & also find the value of non-inductive resistance.

↳ pure resistance. (dynamic resistance)

$R = 20\Omega$

$L = 0.2H$

$C = 100\mu F$

$f_0 = ?$

$Z_d = ?$

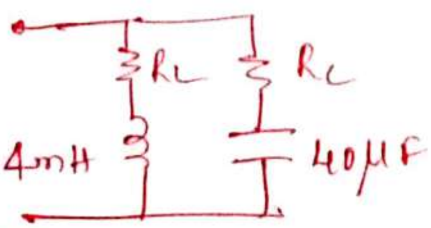
$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$\boxed{f_0 = 31.83\,Hz}$$

$$\& \; Z_d = \frac{L}{RC} = \frac{0.2}{20 \times 100 \times 10^{-6}}$$

$$\boxed{Z_d = 100\Omega}$$

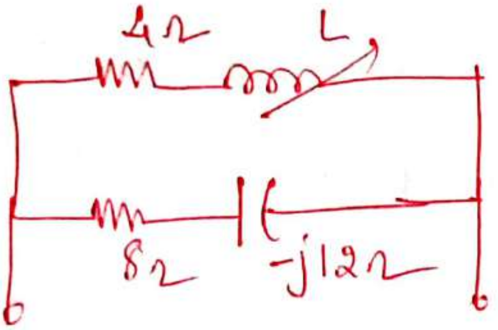
4) Determine R_L & R_C for which the circuit shown below resonates at all frequencies



WKT, $R_L = R_C = \sqrt{\frac{L}{C}}$

$$\boxed{R_L = R_C = 10\Omega}$$

5) Find the value of L for which the ckt given in below figure resonates at $\omega = 5000$ rad/sec.



WKT,

$$\frac{1}{Z} = \frac{1}{Z_1} + \frac{1}{Z_2}$$

$$Y = \frac{1}{4 + jX_L} \times \frac{4 - jX_L}{4 - jX_L} + \frac{1}{8 - j12} \times \frac{8 + j12}{8 + j12}$$

$$Y = \frac{4 - jX_L}{4^2 + X_L^2} + \frac{8 + j12}{64 + 12^2}$$

$$Y = \frac{4}{16 + X_L^2} + \frac{8}{208} \underbrace{- j\frac{X_L}{16 + X_L^2} + j\frac{12}{208}}$$

@ resonance $(B = 0)$

$$\frac{12}{208} = \frac{X_L}{16 + X_L^2}$$

$$12(16 + X_L^2) = 208 X_L$$

144
64
208

$$192 + 12X_L^2 = 208 X_L$$

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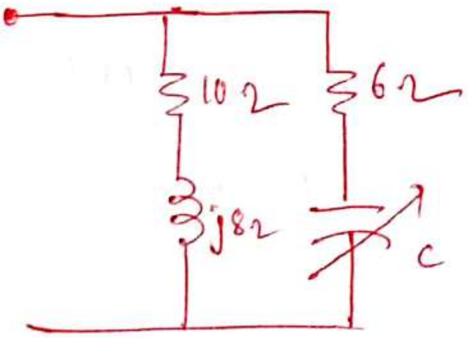
$$12X_L^2 - 208X_L + 192 = 0$$

$X_L = 16.36\,\Omega$ or $X_L = 0.978\,\Omega$

$\omega_0 L = 16.36$	$\omega_0 L = 0.978$
$L = \dfrac{16.36}{5000}$	$L = \dfrac{0.978}{5000}$
$L = 3.72\,mH$	$L = 0.196\,mH$

6) find the value of C for which the circuit given in fig resonants at 750 Hz.



$$Y = \frac{1}{10+j8} + \frac{1}{6-jX_C}$$

$$Y = \frac{1}{10+j8} \times \frac{10-j8}{10-j8} + \frac{1}{6-jX_C} \times \frac{6+jX_C}{6+jX_C}$$

$f = 750\,Hz$

$$Y = \frac{10-j8}{100+64} + \frac{6+jX_C}{36+X_C^2}$$

$$Y = \frac{10}{164} - \frac{j8}{164} + \frac{6}{36+X_C^2} + \frac{jX_C}{36+X_C^2}$$

$Y = G + jB$ @ resonance $B = 0$.

$$\frac{X_c}{36 + X_c^2} = \frac{8}{164}$$

$$164 X_c = 288 + 8 X_c^2$$

$$8 X_c^2 - 164 X_c + 288 = 0$$

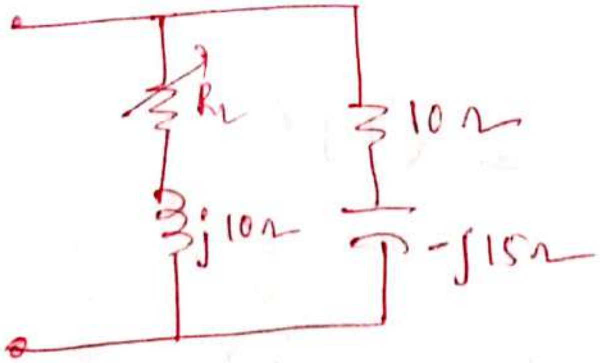
$X_c = 18.56\,\Omega$ or $X_c = 1.94\,\Omega$

$$\frac{1}{\omega_0 C} = 18.56\,\Omega \qquad \frac{1}{2\pi f_0 C} = 1.94$$

$$C = \frac{1}{2\pi f_0 \times 18.56} \qquad C = \frac{1}{2\pi \times 750 \times 1.94}$$

$$\boxed{C = 11.43\,\mu F} \qquad \boxed{C = 109.38\,\mu F}$$

7) find the value of R_L for which, the ckt shown in below fig is ~~Ser~~ resonant.



$$Y = \frac{1}{R_L + j10} + \frac{1}{10 - j15}$$

$$Y = \frac{R_L - j10}{R_L^2 + 10^2} + \frac{10 + j15}{10^2 + 15^2}$$

$$Y = \frac{R_L}{R_L^2 + 100} + \frac{10}{100 + 225} + j\underbrace{\left[\frac{15}{225} - \frac{10}{R_L^2 + 100}\right]}_{\text{reactance}\quad B = 0}$$

$$\Rightarrow \quad \frac{15}{225} = \frac{10}{R_L^2 + 100}$$

$$15\left[R_L^2 + 100\right] = 2250$$

$$15R_L^2 + 1500 = 3250$$

$$15R_L^2 = 3250 - 1500$$

$$15R_L^2 = 1750$$

$$R_L^2 = \frac{1750}{15}$$

$$R_L^2 = 116.67$$

$$\boxed{R_L = 10.8\,\Omega}$$

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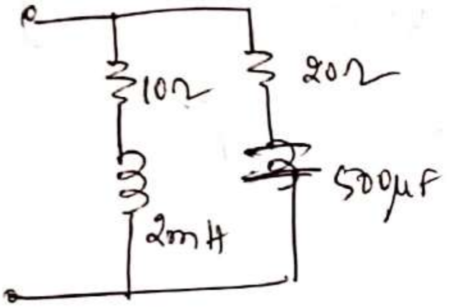
8) An inductive coil of resistance 10Ω & inductance 20mH is connected in 11ul with another branch consisting of a resistance of 20Ω in series with a capacitance of 500μF. Find the resonant frq & the corresponding current, when the applied vg is 230V.



$$f_0 = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{R_L^2 - L/C}{R_C^2 - L/C}}$$

$R_L = 10\Omega$

$R_C = 20\Omega$

$L = 2mH$

$C = 500\mu F$

$f_0 = ?$

$I_0 = ?$

$V = 230V$

$$f_0 = \frac{1}{2\pi\sqrt{2\times10^{-3}\times 500\times10^{-6}}}\sqrt{\frac{100 - \frac{2\times10^{-3}}{500\times10^{-6}}}{400 - \frac{2\times10^{-3}}{500\times10^{-6}}}}$$

$$\boxed{f_0 = 78.36 \text{ Hz}}$$

$$I_0 = V Y_0$$

$$I_0 = V\left[\frac{R_L}{R_L^2 + X_L^2} + \frac{R_C}{R_C^2 + X_C^2}\right]$$

$X_L = 2\pi f_0 L$ & $X_C = \frac{1}{2\pi f_0 C}$

$X_L = 0.98\,\Omega$ $\quad X_C = 4.06\,\Omega$

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$$I_0 = 230\left[\frac{10}{100+0.98^2} + \frac{20}{400+4.06^2}\right]$$

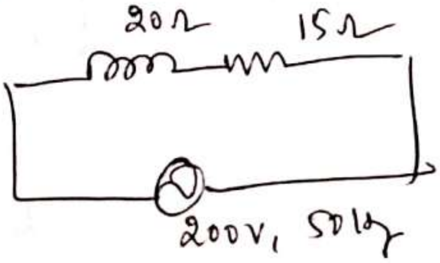
$$\boxed{I_0 = 33.82 \text{ Amp}}$$

9) A circuit has inductive reactance of 20Ω at 50Hz in series with a resistance of 15Ω for an applied vg of 200V at 50Hz. Calculate

1) Phase angle b/n current & voltage

2) the current.

3) The value of shunting capacitance to bring the ckt to resonance & the current at resonance



$X_L = 20\Omega$

$f = 50Hz$

$R = 15\Omega$

$V = 200V$

1) $\phi = ?$

2) $I = ?$

3) $\left.\begin{array}{l} C = ? \\ I_0 = ? \end{array}\right\} @ f_0$

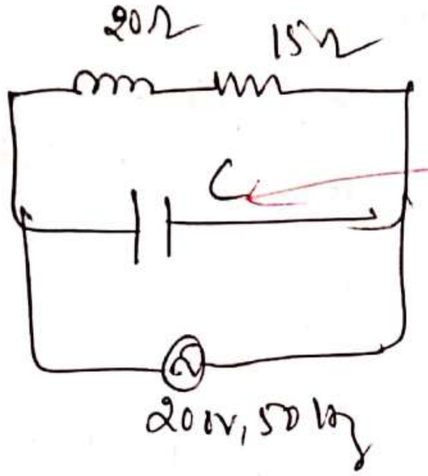
$$\phi = \tan^{-1}\left(\frac{X_L}{R}\right)$$

$$\boxed{\phi = 53.13^\circ}$$

$$I = \frac{V}{Z} = \frac{V}{R+jX_L}$$

$$I = \frac{200}{15 - j20} = 4.8 - j6.4$$

$$\boxed{I = 8\angle -53.13^\circ \text{ amp}}$$



Shunting cap C

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$f_0^2 = \frac{1}{4\pi^2}\left[\frac{1}{LC} - \frac{R^2}{L^2}\right]$$

$$4\pi f_0^2 = \frac{1}{LC} - \frac{R^2}{L^2}$$

$X_L = 20$

$2\pi f_0 L = 20$

$$L = \frac{20}{2\pi \times 50}$$

$$L = 0.0637\,H$$

$$\frac{1}{LC} = 4\pi f_0^2 + \frac{R^2}{L^2}$$

$$\frac{1}{C} = L\left[4\pi f_0^2 + \frac{R^2}{L^2}\right]$$

$$\frac{1}{C} = 0.0637\left[4\pi^2 \times (50)^2 + \frac{15^2}{(0.0637)^2}\right]$$

$$\frac{1}{C} = 6322.26$$

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or $\boxed{C = 158.17\ \mu F}$

$I_0 = \dfrac{V}{Z_d}$ where $Z_d = \dfrac{L}{RC}$

$Z_d = \dfrac{0.0637}{15 \times 158.17 \times 10^{-6}}$

$I_0 = \dfrac{200}{26.55}$

$Z_d = 26.55\ \Omega$

$\boxed{I_0 = 7.533\ \text{amp}}$

10) A parallel resonant ckt has a capacitance of 100pF in one branch & an inductance of 100μH with a resistance of 10Ω in the other branch, the line voltage is 100V. Find i) f_0 2) I_L & I_C 3) I & Z at resonance

$R = 10\ \Omega$

$L = 100\ \mu H$

$C = 100\ pF$

$V = 100\ V$

$f_0 = \dfrac{1}{2\pi}\sqrt{\dfrac{1}{LC} - \dfrac{R^2}{L^2}}$

$\boxed{f_0 = 1.59\ MHz}$

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$$I_L = \frac{V}{Z_L} = \frac{V}{R + jX_L}$$

$$X_L = 2\pi f_0 L$$

$$X_L = 999.02\,\Omega$$

$$= \frac{100}{10 + j999.02}$$

$$\boxed{I_L = 0.1\angle{-89.42}\ \text{Amp}}$$

$$I_c = \frac{V}{Z_c} = \frac{V}{-jX_c}$$

$$X_c = \frac{1}{2\pi f_0 C}$$

$$I_c = \frac{100}{-j1\times10^3}$$

$$X_c = 1k\Omega$$

$$I_c = \frac{100}{1\times10^3\angle{-90}}$$

$$\boxed{I_c = 0.1\angle{90^\circ}\ \text{amp}}$$

$$Z_d = \frac{L}{RC} = 100k\Omega$$

$$I_0 = \frac{V}{Z_d} = 1m\,\text{Amp.}$$

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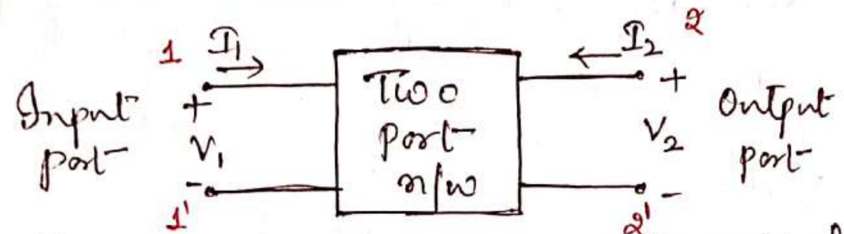
Module-5 Two-Port Network Parameters

Representation of a two-port network:-

A two-port network is a four terminal network. Two input terminals & two output terminals. V_1 & I_1 are the variables at input port & V_2 & I_2 are the variables @ output port. Out of 4 variables V_1, I_1, V_2 & I_2, two of them chosen as independent variables & the remaining two as dependent variables.

11' → i/p port.
22' → o/p port.



Two-port networks are important in modeling electronic devices & system components.

For eg: In Electronics, two port n/ws are employed to model transistors & Op-amps.

Other examples of electrical components modeled by two ports are transformers & transmission lines.

The parameters of a two-port n/w completely describes the physical behaviour of any electronic devices.

Thus knowing the parameters of a two-port n/w permits us to describe its operation when it is connected to a larger network.

Two port n/w parameters are classified as

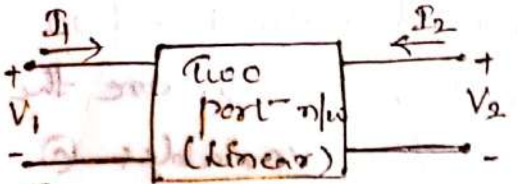
1) Impedance parameters or Z-parameters. (Open-ckt)

2) Admittance parameters or Y-parameters (Short-ckt)

3) Hybrid parameters or h-parameters

4) Transmission parameters or ABCD parameters or T-parameters.

⇒ Impedance Parameters (or Z-parameters or Open ckt impedance parameters)



The n/w shown in figure is assumed to be linear & no independent sources.
Then using superposition theorem, we can write the I/p & output voltages as the sum of two components, one due to I_1 & other due to I_2.

Z-parameters eqns are described by,

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \quad \text{--- (1)}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \quad \text{--- (2)}$$

In matrix form,

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

The Z-parameters are defined as follows,

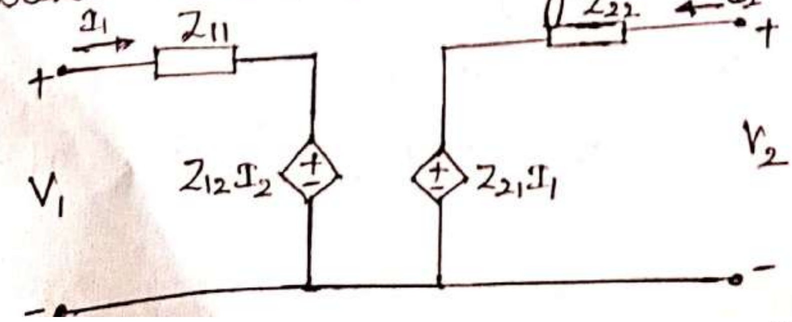
$Z_{11} = \left.\dfrac{V_1}{I_1}\right|_{I_2=0}$ open circuit input impedance parameter.

$Z_{12} = \left.\dfrac{V_1}{I_2}\right|_{I_1=0}$ Open circuit reverse transfer impedance.

$Z_{21} = \left.\dfrac{V_2}{I_1}\right|_{I_2=0}$ open circuit forward transfer impedance.

$Z_{22} = \left.\dfrac{V_2}{I_2}\right|_{I_1=0}$ open circuit output impedance parameter

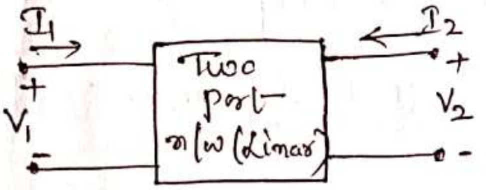
Equivalent circuit describing Z-parameters are,



If $\boxed{Z_{12} = Z_{21}}$ i.e., the transfer impedances are equal then such a n/w is called the "RECIPROCAL NETWORK"

If $\boxed{Z_{11} = Z_{22}}$ then such a n/w is called a Symmetrical n/w.

⇒ Admittence Parameters or Y- Parameters (or Short-circuit admittence parameters)



The n/w shown in figure is assumed to be linear & no independent sources. Then using superposition theorem, we can write the i/p & output currents as the sum of two components, one due to V_1 & other due to V_2.

Y- Parameter eqns are described by,

$$I_1 = Y_{11} V_1 + Y_{12} V_2 \quad \text{——} ①$$

$$I_2 = Y_{21} V_1 + Y_{22} V_2 \quad \text{——} ②$$

In matrix form,

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

Y- Parameters are defined as follows,

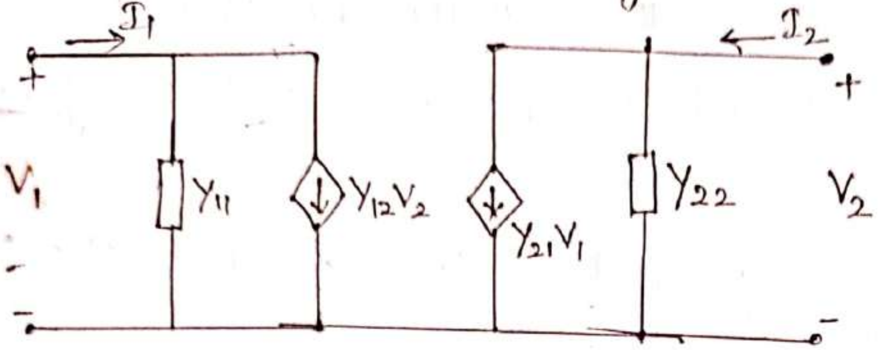
$Y_{11} = \left.\dfrac{I_1}{V_1}\right|_{V_2=0}$ Short circuit input admittence parameters.

$Y_{12} = \left.\dfrac{I_1}{V_2}\right|_{V_1=0}$ Short circuit reverse transfer admittence parameters.

$Y_{21} = \left.\dfrac{I_2}{V_1}\right|_{V_2=0}$ Short circuit forward transfer admittence.

$Y_{22} = \left.\dfrac{I_2}{V_2}\right|_{V_1=0}$ Short circuit Output admittence parameter.

Equivalent circuit describing Y-parameters are,

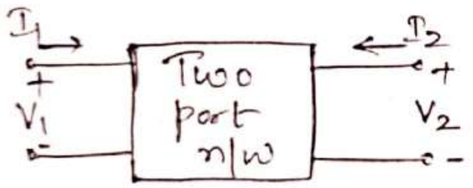


If $\boxed{Y_{12} = Y_{21}}$ then such a n/w is called a "reciprocal n/w"

& If $\boxed{Y_{11} = Y_{22}}$ then such a network is called "symmetrical n/w"

⇒ Hybrid parameters or h-parameters :-

Hybrid parameters are very useful in constructing models for transistors. h-parameters completely describes the internal behaviour of transistors (BJT's).



h-parameters eqns are described by,

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \text{—— (1)}$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \text{—— (2)}$$

In matrix form,

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

h-parameters are defined as follows,

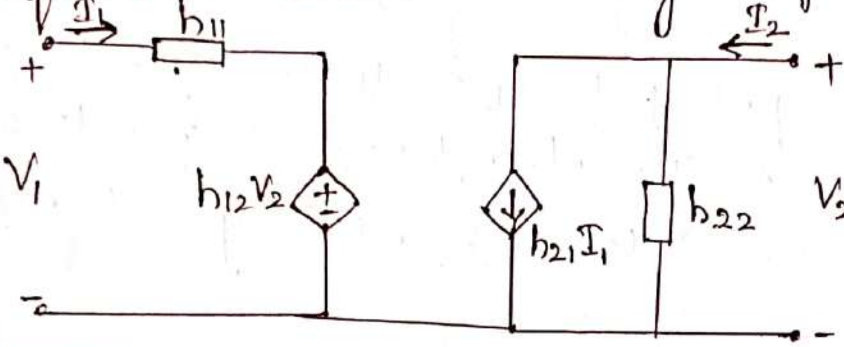
$h_{11} = \left.\dfrac{V_1}{I_1}\right|_{V_2=0}$ Short-circuit input impedance parameter.

$h_{12} = \left.\dfrac{V_1}{V_2}\right|_{I_1=0}$ Known as reverse-voltage gain.

$h_{21} = \left.\dfrac{I_2}{I_1}\right|_{V_2=0}$ Known as forward-current gain.

$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$ known as Open-Circuit Output admittence parameter.

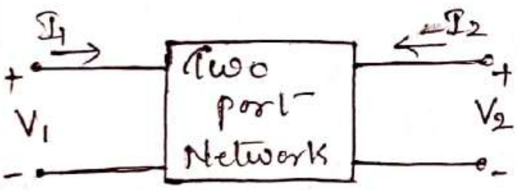
Equivalent circuit describing h-parameters,



If $\boxed{h_{12} = -h_{21}}$ then the circuit is said to be reciprocal n/w

& if $\boxed{h_{11}h_{22} - h_{12}h_{21} = 1}$ or $\boxed{\Delta h = 1}$ then the n/w is said to be Symmetrical n/w.

⇒ Transmission parameters or ABCD parameters or T-parameters.



The T-parameters eqns are described by,

$$V_1 = AV_2 - BI_2 \quad \text{——①}$$

$$I_1 = CV_2 - DI_2 \quad \text{——②}$$

In matrix form,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

T-parameters are mainly used in analysis of Transmission lines & Cascaded networks. & hence they are called as transmission parameters.

T-parameters are defined as,

$A = \left.\frac{V_1}{V_2}\right|_{I_2=0}$ reverse voltage gain with o/p port open circuited

$B = \left.\frac{V_1}{-I_2}\right|_{V_2=0}$ reverse transfer impedance

$\therefore\ C = \left.\frac{I_1}{V_2}\right|_{I_2=0}$ reverse transfer admittance.

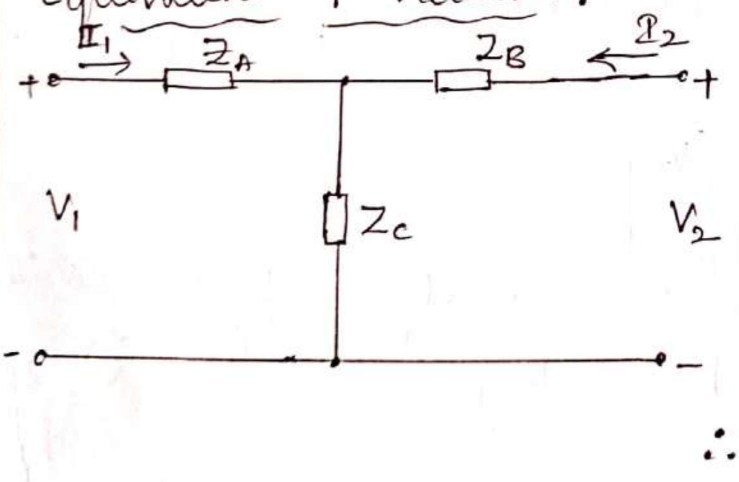
$D = \left.\frac{I_1}{-I_2}\right|_{V_2=0}$ reverse current gain with o/p port short ckt.

Quantities at the input port V_1 & I_1 are called as sending end voltages & currents. Where as quantities at the output port are called as receiving end voltages & currents.

T and π network representation of a two port network

Practically the transmission lines, filters & attenuators are represented in the form of equivalent T or π networks. Thus if the Y-parameters are known, an equivalent π n/w can be easily constructed & if the Z-parameters are known an equivalent T n/w can be made.

Equivalent T-network:



It is required to determine Z_A, Z_B & Z_C in terms of Z_{11}, Z_{12}, Z_{21} & Z_{22}.

W.K.T $Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0}$

$\therefore\ \boxed{Z_{11} = Z_A + Z_C}$

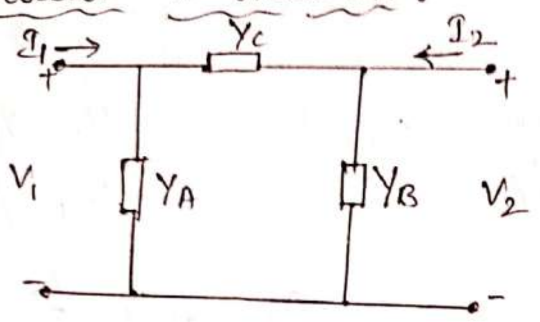
Also $Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}$ (when $I_1=0$ current through Z_A is zero, $\therefore$ it can be neglected)

$\boxed{Z_{22} = Z_B + Z_C}$

& $\boxed{Z_{12} = Z_{21} = Z_C}$

If Z-parameters of the n/w are known, the equivalent-T n/w can be found out using the above relations.

Equivalent π network :-



It is required to find Y_A, Y_B & Y_C in terms of Y-parameters.

W.K.T $Y_{11} = \left.\dfrac{I_1}{V_1}\right|_{V_2=0}$

when $V_2=0$, i.e o/p port shorted then Y_B becomes zero,

$\therefore \boxed{Y_{11} = Y_A + Y_C}$

|||ly $\boxed{Y_{22} = Y_B + Y_C}$

Also, $Y_{12} = \left.\dfrac{I_1}{V_2}\right|_{V_1=0}$, $Y_{21} = \left.\dfrac{I_2}{V_1}\right|_{V_2=0}$

$$\boxed{Y_{12} = Y_{21} = -Y_C}$$

Thus knowing Y-parameters of a 2-port n/w, elements of π n/w can be found out using the relations derived above.

Relations between two parameters :-

1) Z-parameters in terms of Y-parameters

The equations describing Z-parameters are

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \quad \text{--- (1)}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \quad \text{--- (2)}$$

The equations describing Y-parameters are

$$I_1 = Y_{11} V_1 + Y_{12} V_2 \quad \text{--- (3)}$$

$$I_2 = Y_{21} V_1 + Y_{22} V_2 \quad \text{--- (4)}$$

Y-parameters in matrix form,

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

By using Crammer's rule,

$$V_1 = \frac{\Delta_1}{\Delta Y} \quad , \quad V_2 = \frac{\Delta_2}{\Delta Y} \quad \text{where } \Delta Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$$

$$\Delta Y = Y_{11} Y_{22} - Y_{12} Y_{21}$$

$$V_1 = \frac{\begin{vmatrix} I_1 & Y_{12} \\ I_2 & Y_{22} \end{vmatrix}}{\Delta Y}$$

$$V_1 = \frac{Y_{22} I_1 - Y_{12} I_2}{\Delta Y} = \frac{Y_{22}}{\Delta Y} I_1 - \frac{Y_{12}}{\Delta Y} I_2$$

$$V_1 = \frac{Y_{22}}{\Delta Y} I_1 - \frac{Y_{12}}{\Delta Y} I_2 \quad \text{——} (5)$$

Comparing equations (5) & (1)

$$\boxed{Z_{11} = \frac{Y_{22}}{\Delta Y}} \qquad \boxed{Z_{12} = \frac{-Y_{12}}{\Delta Y}}$$

Also, $$V_2 = \frac{\begin{vmatrix} Y_{11} & I_1 \\ Y_{21} & I_2 \end{vmatrix}}{\Delta Y}$$

$$V_2 = \frac{Y_{11} I_2 - Y_{21} I_1}{\Delta Y}$$

$$V_2 = \frac{Y_{11}}{\Delta Y} I_2 - \frac{Y_{21}}{\Delta Y} I_1 \quad \text{rearranging the terms}$$

$$V_2 = \frac{-Y_{21}}{\Delta Y} I_1 + \frac{Y_{11}}{\Delta Y} I_2 \quad \text{——} (6)$$

Comparing eqn ② & ⑥

$$\boxed{Z_{21} = -\frac{Y_{21}}{\Delta Y}} \qquad \boxed{Z_{22} = \frac{Y_{11}}{\Delta Y}}$$

$$\therefore \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} & -\frac{Y_{12}}{\Delta Y} \\ -\frac{Y_{21}}{\Delta Y} & +\frac{Y_{11}}{\Delta Y} \end{bmatrix}$$

2) Z-parameters in terms of h-parameters:

The equations describing Z-parameters are,

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \quad \text{—①}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \quad \text{—②}$$

The equations describing h-parameters are,

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \text{—③}$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \text{—④}$$

From eqn ④ $I_2 = h_{21} I_1 + h_{22} V_2$

$$h_{22} V_2 = I_2 - h_{21} I_1$$

$$V_2 = \frac{I_2}{h_{22}} - \frac{h_{21}}{h_{22}} I_1$$

or $V_2 = -\frac{h_{21}}{h_{22}} I_1 + \frac{1}{h_{22}} I_2$ —⑤

Comparing ② & ⑤

$$\boxed{Z_{21} = \frac{-h_{21}}{h_{22}}} \qquad \boxed{Z_{22} = \frac{1}{h_{22}}}$$

Substitute eqn ⑤ in eqn ③, we get.

$$V_1 = h_{11} I_1 + h_{12}\left[-\frac{h_{21}}{h_{22}} I_1 + \frac{1}{h_{22}} I_2\right]$$

$$V_1 = h_{11} I_1 - \frac{h_{12} h_{21}}{h_{22}} I_1 + \frac{h_{12}}{h_{22}} I_2$$

$$V_1 = \left(\frac{h_{11} h_{22} - h_{12} h_{21}}{h_{22}}\right) I_1 + \frac{h_{12}}{h_{22}} I_2$$

$$V_1 = \frac{\Delta h}{h_{22}} I_1 + \frac{h_{12}}{h_{22}} I_2 \quad \text{—— ⑥} \qquad \text{where } \Delta h = h_{11} h_{22} - h_{12} h_{21}$$

Comparing ① & ⑥, we get -

$$\boxed{Z_{11} = \frac{\Delta h}{h_{22}}}, \quad \boxed{Z_{12} = \frac{h_{12}}{h_{22}}}$$

$$Z \begin{cases} Y \\ h \\ T \end{cases}$$

$$\therefore \quad \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \frac{\Delta h}{h_{22}} & \frac{h_{12}}{h_{22}} \\ \frac{-h_{21}}{h_{22}} & \frac{1}{h_{22}} \end{bmatrix}$$

3) Z - parameters in terms of T - parameters.

Z-parameters equations are, T-parameters eqns are.

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \quad \text{—— ①} \qquad V_1 = A V_2 - B I_2 \quad \text{—— ③}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \quad \text{—— ②} \qquad I_1 = C V_2 - D I_2 \quad \text{—— ④}$$

from eqn ④, $I_1 = C V_2 - D I_2$

$$C V_2 = I_1 + D I_2$$

$$V_2 = \frac{1}{C} I_1 + \frac{D}{C} I_2 \quad \text{—— ⑤}$$

Comparing this with eqn ②.

$$\boxed{Z_{21} = \frac{1}{C}} \qquad \boxed{Z_{22} = \frac{D}{C}}$$

From eqn, ③.

$$V_1 = A\left[\frac{1}{C} I_1 + \frac{D}{C} I_2\right] - B I_2$$

$$V_1 = \frac{A}{C} I_1 + \frac{AD}{C} I_2 - B I_2$$

$$V_1 = \frac{A}{C} I_1 + \frac{(AD - BC)}{C} I_2 \quad \text{——} \quad (6)$$

Comparing (6) with eqn (1), we get,

$$\boxed{Z_{11} = \frac{A}{C}} \qquad \boxed{Z_{12} = \frac{AD - BC}{C}}$$

$$\therefore \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \frac{A}{C} & \frac{AD-BC}{C} \\ \frac{1}{C} & D/C \end{bmatrix}$$

4) Y-parameters in terms of Z-parameters:

The equations describing Y-parameters are,

$$I_1 = Y_{11} V_1 + Y_{12} V_2 \quad \text{——} \quad (1)$$

$$I_2 = Y_{21} V_1 + Y_{22} V_2 \quad \text{——} \quad (2)$$

The equations describing Z-parameters are,

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \quad \text{——} \quad (3)$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \quad \text{——} \quad (4)$$

In matrix form, $\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$

But $I_1 = \frac{\Delta_1}{\Delta Z}$, $I_2 = \frac{\Delta_2}{\Delta Z}$ $\qquad \Delta Z = \begin{vmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{vmatrix}$

$$\Delta Z = Z_{11} Z_{22} - Z_{12} Z_{21}$$

$$I_1 = \frac{\begin{vmatrix} V_1 & Z_{12} \\ V_2 & Z_{22} \end{vmatrix}}{\Delta Z}$$

$$I_1 = \frac{V_1 Z_{22} - V_2 Z_{12}}{\Delta Z} = \frac{Z_{22}}{\Delta Z} V_1 - \frac{Z_{12}}{\Delta Z} V_2 \quad \text{——} \quad (5)$$

Comparing ⑤ with eqn ①, we get

$$\boxed{Y_{11} = \frac{Z_{22}}{\Delta Z}} \quad \boxed{Y_{12} = \frac{-Z_{12}}{\Delta Z}}$$

Similarly, $I_2 = \dfrac{\begin{vmatrix} Z_{11} & V_1 \\ Z_{21} & V_2 \end{vmatrix}}{\Delta Z}$

$$I_2 = \frac{Z_{11} V_2 - Z_{21} V_1}{\Delta Z}$$

$$I_2 = \frac{Z_{11}}{\Delta Z} V_2 - \frac{Z_{21}}{\Delta Z} V_1$$ rearranging the terms

or $I_2 = \dfrac{-Z_{21}}{\Delta Z} V_1 + \dfrac{Z_{11}}{\Delta Z} V_2$ —— ⑥

Comparing ⑥ with eqn ②, we get.

$$\boxed{Y_{21} = \frac{-Z_{21}}{\Delta Z}} \quad \boxed{Y_{22} = \frac{Z_{11}}{\Delta Z}}$$

$$\therefore \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{Z_{22}}{\Delta Z} & -\frac{Z_{12}}{\Delta Z} \\ \frac{-Z_{21}}{\Delta Z} & \frac{Z_{11}}{\Delta Z} \end{bmatrix}$$

5) Y-parameters in terms of h-parameters :

Y-parameters eqns are

$\therefore I_1 = Y_{11} V_1 + Y_{12} V_2$ —— ①

$I_2 = Y_{21} V_1 + Y_{22} V_2$ —— ②

h-parameters eqns are.

$V_1 = h_{11} I_1 + h_{12} V_2$ —— ③

$I_2 = h_{21} I_1 + h_{22} V_2$ —— ④

From ③, $V_1 = h_{11} I_1 + h_{12} V_2$

$$I_1 = \frac{V_1 - h_{12} V_2}{h_{11}} = \frac{1}{h_{11}} V_1 - \frac{h_{12}}{h_{11}} V_2$$ —— ⑤

Comparing (5) & (1).

$$\boxed{Y_{11} = \frac{1}{h_{11}}} \qquad \boxed{Y_{12} = \frac{-h_{12}}{h_{11}}}$$

Substitute (5) in eqn (4)

$$I_2 = h_{21}\left[\frac{1}{h_{11}}V_1 - \frac{h_{12}}{h_{11}}V_2\right] + h_{22}V_2$$

$$I_2 = \frac{h_{21}}{h_{11}}V_1 - \frac{h_{21}h_{12}}{h_{11}}V_2 + h_{22}V_2$$

$$I_2 = \frac{h_{21}}{h_{11}}V_1 + V_2\left[h_{22} - \frac{h_{21}h_{12}}{h_{11}}\right] \longrightarrow h_{11}h_{22} - h_{21}h_{12} = \Delta h$$

$$I_2 = \frac{h_{21}}{h_{11}}V_1 + \frac{\Delta h}{h_{11}}V_2 \quad \text{—— (6)}$$

Comparing (6) & (2), we get.

$$\boxed{Y_{21} = \frac{h_{21}}{h_{11}}} \qquad \boxed{Y_{22} = \frac{\Delta h}{h_{11}}}$$

$$\therefore \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{h_{11}} & \frac{-h_{12}}{h_{11}} \\ \frac{h_{21}}{h_{11}} & \frac{\Delta h}{h_{11}} \end{bmatrix}$$

Y — Z, h, T

6) Y- Parameters in terms of T- Parameters :

Y- parameters eqns are,

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \quad \text{—— (1)}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \quad \text{—— (2)}$$

T- parameters eqns are

$$V_1 = AV_2 - BI_2 \quad \text{—— (3)}$$

$$I_1 = CV_2 - DI_2 \quad \text{—— (4)}$$

From (3) $V_1 = AV_2 - BI_2$

or $I_2 = \dfrac{AV_2 - V_1}{B} = -\dfrac{1}{B}V_1 + \dfrac{A}{B}V_2$ —— (5)

Comparing ② & ⑤

$$\boxed{Y_{21} = \frac{-1}{B}} \qquad \boxed{Y_{22} = \frac{A}{B}}$$

from equation ④,

$$I_1 = CV_2 - D\left[\frac{-1}{B}V_1 + \frac{A}{B}V_2\right]$$

$$I_1 = CV_2 + \frac{D}{B}V_1 - \frac{AD}{B}V_2$$

$$I_1 = \left(C - \frac{AD}{B}\right)V_2 + \frac{D}{B}V_1$$

or $$I_1 = \frac{D}{B}V_1 + \frac{BC-AD}{B}V_2 \quad \text{—— ⑥}$$

Comparing ① & ⑥.

$$\boxed{Y_{11} = \frac{D}{B}} \qquad \boxed{Y_{12} = \frac{BC-AD}{B}}$$

$$\therefore \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{D}{B} & \frac{BC-AD}{B} \\ \frac{-1}{B} & \frac{A}{B} \end{bmatrix}$$

7) h-parameters in terms of Z-parameters :-

h-parameters eqns are

$V_1 = h_{11}I_1 + h_{12}V_2$ —— ①

$I_2 = h_{21}I_1 + h_{22}V_2$ —— ②

Z-parameters eqns are

$V_1 = Z_{11}I_1 + Z_{12}I_2$ —— ③

$V_2 = Z_{21}I_1 + Z_{22}I_2$ —— ④

From eqn ④

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

$$I_2 = \frac{V_2 - Z_{21}I_1}{Z_{22}} = \frac{1}{Z_{22}}V_2 - \frac{Z_{21}}{Z_{22}}I_1$$

$$I_2 = -\frac{Z_{21}}{Z_{22}} I_1 + \frac{1}{Z_{22}} V_2 \quad \text{——} (5)$$

Comparing eqn (2) & (5)

$$\boxed{h_{21} = -\frac{Z_{21}}{Z_{22}}} \qquad \boxed{h_{22} = \frac{1}{Z_{22}}}$$

From (3), $V_1 = Z_{11} I_1 + Z_{12}\left[-\frac{Z_{21}}{Z_{22}} I_1 + \frac{1}{Z_{22}} V_2\right]$

$$V_1 = Z_{11} I_1 + \frac{Z_{12}}{Z_{22}} V_2 - \frac{Z_{12} Z_{21}}{Z_{22}} I_1$$

$$V_1 = \left[\frac{Z_{11} Z_{22} - Z_{12} Z_{21}}{Z_{22}}\right] I_1 + \frac{Z_{12}}{Z_{22}} V_2$$

$$V_1 = \frac{\Delta Z}{Z_{22}} I_1 + \frac{Z_{12}}{Z_{22}} V_2 \quad \text{——} (6)$$ where $\Delta Z = Z_{11} Z_{22} - Z_{12} Z_{21}$

Comparing (1) & (6), we get,

$$\boxed{h_{11} = \frac{\Delta Z}{Z_{22}}}, \quad \boxed{h_{12} = \frac{Z_{12}}{Z_{22}}}$$

$$\therefore \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \frac{\Delta Z}{Z_{22}} & \frac{Z_{12}}{Z_{22}} \\ -\frac{Z_{21}}{Z_{22}} & \frac{1}{Z_{22}} \end{bmatrix}$$

$h \begin{cases} Z \\ Y \\ T \end{cases}$

8) h-parameters in terms of Y-parameters.

h-parameters equations are,

$V_1 = h_{11} I_1 + h_{12} V_2$ —— (1)

$I_2 = h_{21} I_1 + h_{22} V_2$ —— (2)

Y-parameters eqns are

$I_1 = Y_{11} V_1 + Y_{12} V_2$ —— (3)

$I_2 = Y_{21} V_1 + Y_{22} V_2$ —— (4)

from (3) $I_1 = Y_{11} V_1 + Y_{12} V_2$

$$V_1 = \frac{1}{Y_{11}} I_1 - \frac{Y_{12}}{Y_{11}} V_2 \quad \text{——} ⑤$$

Compare ⑤ with ①, we get.

$$\boxed{h_{11} = \frac{1}{Y_{11}}} \qquad \boxed{h_{12} = \frac{-Y_{12}}{Y_{11}}}$$

From (4),

$$I_2 = Y_{21}\left[\frac{1}{Y_{11}} I_1 - \frac{Y_{12}}{Y_{11}} V_2\right] + Y_{22} V_2$$

$$I_2 = \frac{Y_{21}}{Y_{11}} I_1 - \frac{Y_{21} Y_{12}}{Y_{11}} V_2 + Y_{22} V_2 .$$

$$I_2 = \frac{Y_{21}}{Y_{11}} I_1 + V_2 \left[\frac{Y_{11} Y_{22} - Y_{12} Y_{21}}{Y_{11}}\right] \rightarrow \Delta h \quad \text{——} ⑥$$

compare ⑥ with ②, we get,

$$\boxed{h_{21} = \frac{Y_{21}}{Y_{11}}} \qquad \boxed{h_{22} = \frac{\Delta Y}{Y_{11}}}$$

$$\therefore \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{Y_{11}} & -\frac{Y_{12}}{Y_{11}} \\ \frac{Y_{21}}{Y_{11}} & \frac{\Delta Y}{Y_{11}} \end{bmatrix}$$

9) h-parameters in terms of T- parameters :

h- parameters eqns are

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \text{——} ①$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \text{——} ②$$

T- parameters eqns are,

$$V_1 = A V_2 - B I_2 \quad \text{——} ③$$

$$I_1 = C V_2 - D I_2 \quad \text{——} ④$$

From (4), $I_2 = \dfrac{C V_2 - I_1}{D}$

$$I_2 = \frac{C}{D} V_2 - \frac{1}{D} I_1 \Rightarrow I_2 = -\frac{1}{D} I_1 + \frac{C}{D} V_2 \text{——} ⑤$$

Comparing 5 with eqn 2

$$\boxed{h_{21} = \frac{-1}{D}} \qquad \boxed{h_{22} = \frac{C}{D}}$$

From eqn (3),

$$V_1 = AV_2 - B\left[-\frac{1}{D} I_1 + \frac{C}{D} V_2\right]$$

$$V_1 = AV_2 + \frac{B}{D} I_1 - \frac{BC}{D} V_2 = \frac{(AD-BC)}{D} V_2 + \frac{B}{D} I_1$$

$$\Rightarrow V_1 = \frac{B}{D} I_1 + \frac{(AD-BC)}{D} V_2 \quad \text{—— (6)}$$

Comparing 6 with 1

$$\boxed{h_{11} = \frac{B}{D}} \qquad \boxed{h_{12} = \frac{AD-BC}{D}}$$

$$\therefore \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \frac{B}{D} & \frac{AD-BC}{D} \\ -\frac{1}{D} & \frac{C}{D} \end{bmatrix}$$

10. T-parameters in terms of Z-parameters

T-parameters eqns are

$$V_1 = AV_2 - BI_2 \quad \text{—— (1)}$$

$$I_1 = CV_2 - DI_2 \quad \text{—— (2)}$$

Z-parameters eqns are

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \quad \text{—— (3)}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \quad \text{—— (4)}$$

From (4),

$$I_1 = \frac{V_2 - Z_{22} I_2}{Z_{21}}$$

T
Z
Y
h

$$I_1 = \frac{1}{Z_{21}} V_2 - \frac{Z_{22}}{Z_{21}} I_2 \quad \text{—— (5)}$$

from 2 & 5

$$\boxed{C = \frac{1}{Z_{21}}} \qquad \boxed{D = \frac{Z_{22}}{Z_{21}}}$$

From (3), $V_1 = Z_{11}\left[\frac{1}{Z_{21}} V_2 - \frac{Z_{22}}{Z_{21}} I_2\right] + Z_{12} I_2$

$$V_1 = \frac{Z_{11}}{Z_{21}} V_2 - \underbrace{\frac{Z_{11} Z_{22}}{Z_{21}} I_2 + Z_{12} I_2}$$

$$V_1 = \frac{Z_{11}}{Z_{21}} V_2 + I_2\left[\frac{Z_{12} Z_{21} - Z_{11} Z_{22}}{Z_{21}}\right]$$

$$V_1 = \frac{Z_{11}}{Z_{21}} V_2 - \frac{(Z_{11} Z_{22} - Z_{12} Z_{21})}{Z_{21}} I_2 \quad \Delta Z$$

$$\therefore \quad V_1 = \frac{Z_{11}}{Z_{21}} V_2 - \frac{\Delta Z}{Z_{21}} I_2 \quad \text{——} \quad (6)$$

Comparing (6) & (1) we get.

$$\boxed{A = \frac{Z_{11}}{Z_{21}}} \qquad \boxed{B = \frac{\Delta Z}{Z_{21}}}$$

$$\therefore \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{Z_{11}}{Z_{21}} & \frac{\Delta Z}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{bmatrix}$$

iii) T-parameters in terms Y- parameters.

T-parameters eqns are

$$V_1 = A V_2 - B I_2 \quad \text{——} \quad (1)$$

$$I_1 = C V_2 - D I_2 \quad \text{——} \quad (2)$$

Y-parameters eqns are,

$$I_1 = Y_{11} V_1 + Y_{12} V_2 \quad \text{——} \quad (3)$$

$$I_2 = Y_{21} V_1 + Y_{22} V_2 \quad \text{——} \quad (4)$$

from (4)

$$V_1 = \frac{I_2 - Y_{22} V_2}{Y_{21}}$$

$$V_1 = -\frac{Y_{22}}{Y_{21}} V_2 + \frac{1}{Y_{21}} I_2 \quad \text{——} \quad (5)$$

comparing ① & ⑤, we get-

$$\boxed{A = -\frac{Y_{22}}{Y_{21}}} \qquad \boxed{B = -\frac{1}{Y_{21}}}$$

from (3) $I_1 = Y_{11}\left[-\frac{Y_{22}}{Y_{21}} V_2 + \frac{1}{Y_{21}} I_2\right] + Y_{12} V_2$

$$I_1 = -\frac{Y_{11} Y_{22}}{Y_{21}} V_2 + \frac{Y_{11}}{Y_{21}} I_2 + Y_{12} V_2$$

$$I_1 = -\left(\frac{Y_{11} Y_{22} - Y_{12} Y_{21}}{Y_{21}}\right) V_2 + \frac{Y_{11}}{Y_{21}} I_2$$

or $$I_1 = -\frac{\Delta Y}{Y_{21}} V_2 + \frac{Y_{11}}{Y_{21}} I_2 \quad \text{——} ⑥$$

Comparing ⑥ & ① we get,

$$\boxed{C = -\frac{\Delta Y}{Y_{21}}} \qquad \boxed{D = -\frac{Y_{11}}{Y_{21}}}$$

$$\therefore \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} -\frac{Y_{22}}{Y_{21}} & -\frac{1}{Y_{21}} \\ -\frac{\Delta Y}{Y_{21}} & -\frac{Y_{11}}{Y_{21}} \end{bmatrix}$$

12) T-parameters in terms of h-parameters :-

T-parameters eqns are

$V_1 = AV_2 - BI_2$ —— ①

$I_1 = CV_2 - DI_2$ —— ②

h-parameters eqns are

$V_1 = h_{11} I_1 + h_{12} V_2$ —— ③

$I_2 = h_{21} I_1 + h_{22} V_2$ —— ④

from eqn (4) $I_1 = \frac{I_2 - h_{22} V_2}{h_{21}}$

$$I_1 = -\frac{h_{22}}{h_{21}} V_2 + \frac{1}{h_{21}} I_2 \quad \text{——} ⑤$$

Comparing (5) with (2)

$$\boxed{C = \frac{-h_{22}}{h_{21}}} \qquad \boxed{D = \frac{-1}{h_{21}}}$$

From (3), $V_1 = h_{11}\left[\frac{-h_{22}}{h_{21}} V_2 + \frac{1}{h_{21}} I_2\right] + h_{12} V_2$

$$V_1 = \frac{-h_{11}h_{22}}{h_{21}} V_2 + \frac{h_{11}}{h_{21}} I_2 + h_{12} V_2$$

$$V_1 = -\left[\frac{h_{11}h_{22} - h_{12}h_{21}}{h_{21}}\right] V_2 + \frac{h_{11}}{h_{21}} I_2$$

$$V_2\left(h_{12} - \frac{h_{11}h_{22}}{h_{21}}\right)$$

$$V_2\left[\frac{h_{12}h_{21} - h_{11}h_{22}}{h_{21}}\right]$$

$$-\left(\frac{h_{11}h_{22} - h_{12}h_{21}}{h_{21}}\right)$$

or $V_1 = \frac{-\Delta h}{h_{21}} V_2 + \frac{h_{11}}{h_{21}} I_2$ —— (6)

Comparing (6) with (1)

$$\boxed{A = \frac{-\Delta h}{h_{21}}} \qquad \boxed{B = \frac{-h_{11}}{h_{21}}}$$

$$\therefore \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{-\Delta h}{h_{21}} & \frac{-h_{11}}{h_{21}} \\ \frac{-h_{22}}{h_{21}} & \frac{-1}{h_{21}} \end{bmatrix}$$

Symmetry & Reciprocity of two-port n/ws.

"Symmetry & reciprocity are the two imp characteristics of two-port n/ws. A network is said to be symmetrical if the it exhibits the same characteristics when its ports are interchanged."

For Z-parameters, if the impedance measured at one point is equal to the impedance measured @ the other port with remaining port open ckt, the n/w is said to be symmetrical.

$$\boxed{Z_{11} = Z_{22}}$$

"A n/w is said to be reciprocal, if it exhibits the property that the ratio of source to response @ both ports are same."

For z-parameters, if $\boxed{Z_{12} = Z_{21}}$, the network is said to be reciprocal.

2) Y-Parameters :-

Condition of symmetry for y-parameters is $\boxed{Y_{11} = Y_{22}}$

& Condition of reciprocity is $\boxed{Y_{12} = Y_{21}}$.

3) h-parameters :-

For h-parameters, condition of symmetry is $\Delta h = 1$

i.e., $\boxed{h_{11}h_{22} - h_{12}h_{21} = 1}$

& the condition of reciprocity is $\boxed{h_{12} = -h_{21}}$

4) ABCD or T-parameters :

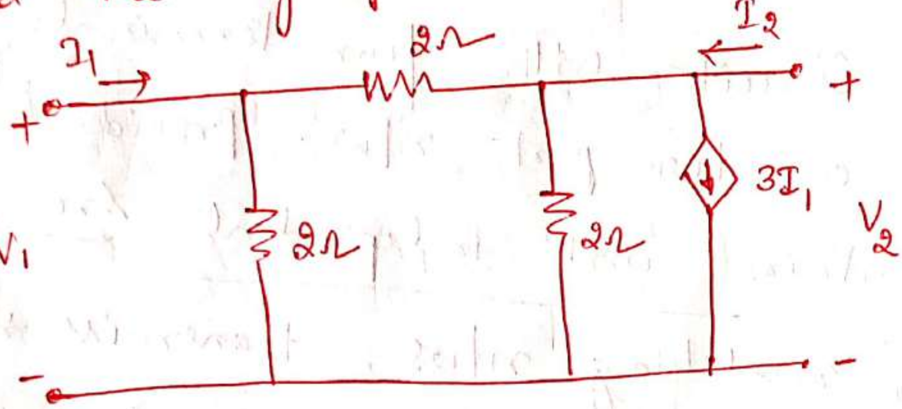
T-n/w is said to be symmetrical if $\boxed{A = D}$ & it is said to be reciprocal if $\boxed{AD - BC = 1}$.

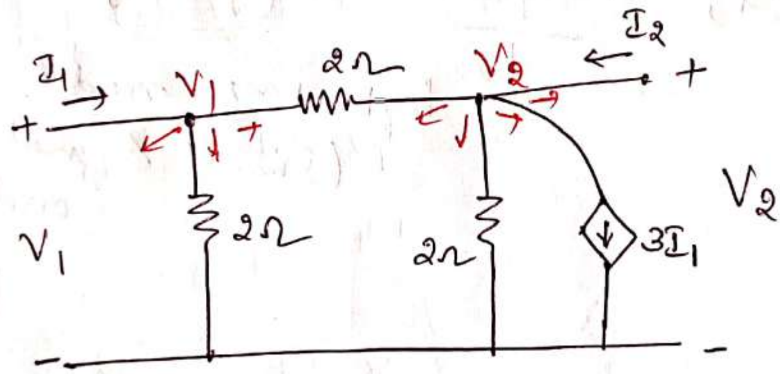
	Parameters	Condition of symmetry	Cond of reciprocity
a)	Z	$Z_{11} = Z_{22}$	$Z_{12} = Z_{21}$
b)	Y	$Y_{11} = Y_{22}$	$Y_{12} = Y_{21}$
c)	h	$\Delta h = 1$	$h_{12} = -h_{21}$
d)	T	$A = D$	$AD - BC = 1$

Problems on Two-port network :-

I) Problems on dependent source [Always use KCL method]

1) Find the y- parameters.





Apply KCL @ node 1

$$-I_1 + \frac{V_1}{2} + \frac{V_1 - V_2}{2} = 0$$

$$-I_1 + \frac{V_1}{2} + \frac{V_1}{2} - \frac{V_2}{2} = 0$$

$$I_1 = V_1 - \frac{V_2}{2} \Rightarrow I_1 = V_1 - 0.5V_2 \quad \text{—(1)}$$

Scanned with CamScanner

Comparing with Std eqn

$$I_1 = Y_{11} V_1 + Y_{12} V_2$$

$\boxed{Y_{11} = 1 \mho}$ $\boxed{Y_{12} = -0.5 \mho}$

Apply KCL @ node 2.

$$\frac{V_2 - V_1}{2} + \frac{V_2}{2} + 3I_1 - I_2 = 0$$

$$\frac{V_2}{2} - \frac{V_1}{2} + \frac{V_2}{2} + 3 I_1 - I_2 = 0$$

↳ eqn ①

$$V_2 - 0.5 V_1 + 3 (V_1 - 0.5 V_2) - I_2 = 0$$

$$V_2 - 0.5 V_1 + 3V_1 - 1.5 V_2 - I_2 = 0$$

$$I_2 = 2.5 V_1 - 0.5 V_2 \quad \text{—— ②}$$

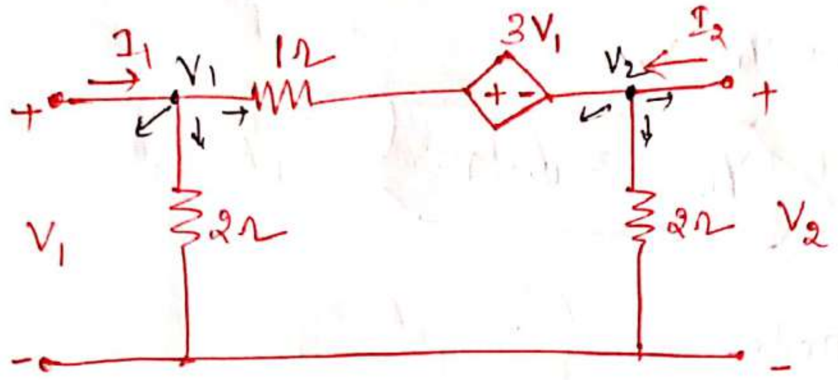
Comparing with Std eqn

$$I_2 = Y_{21} V_1 + Y_{22} V_2$$

$\boxed{Y_{21} = 2.5 \mho}$ $\boxed{Y_{22} = -0.5 \mho}$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 1 & -0.5 \\ 2.5 & -0.5 \end{bmatrix} \mho$$

2) Find Y- parameters



Apply KCL @ node 1.

$$-I_1 + \frac{V_1}{2} + \left(\frac{V_1 - 3V_1 - V_2}{1}\right) = 0$$

$$-I_1 + 0.5V_2 + V_1 - 3V_1 - V_2 = 0$$

$$I_1 = -1.5V_1 - V_2 \quad \text{—— (1)}$$

Comparing with Std eqn. $I_1 = Y_{11}V_1 + Y_{12}V_2$

$\boxed{Y_{11} = -1.5\,\mho}$ $\boxed{Y_{12} = -1\,\mho}$

Apply KCL @ node 2

$$\frac{V_2}{2} + \frac{V_2 + 3V_1 - V_1}{1} - I_2 = 0$$

$$0.5V_2 + V_2 + 3V_1 - V_1 - I_2 = 0$$

$$I_2 = 2V_1 + 1.5V_2$$

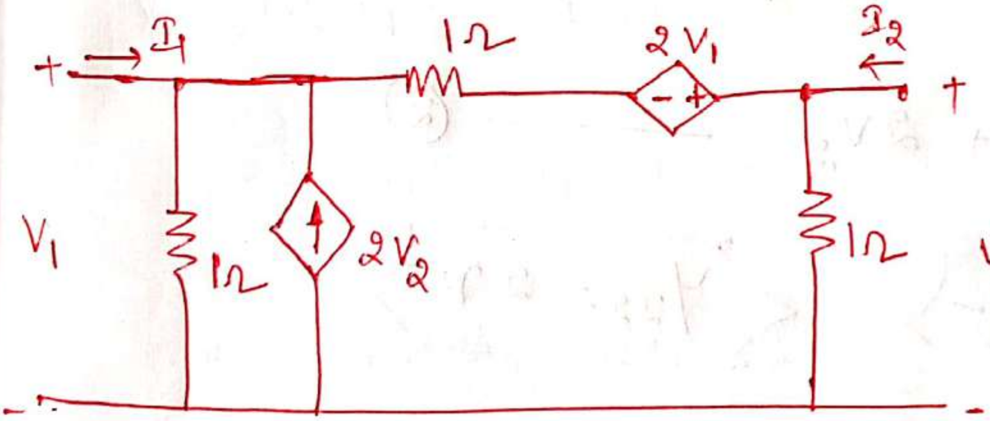
Comparing with std eqn

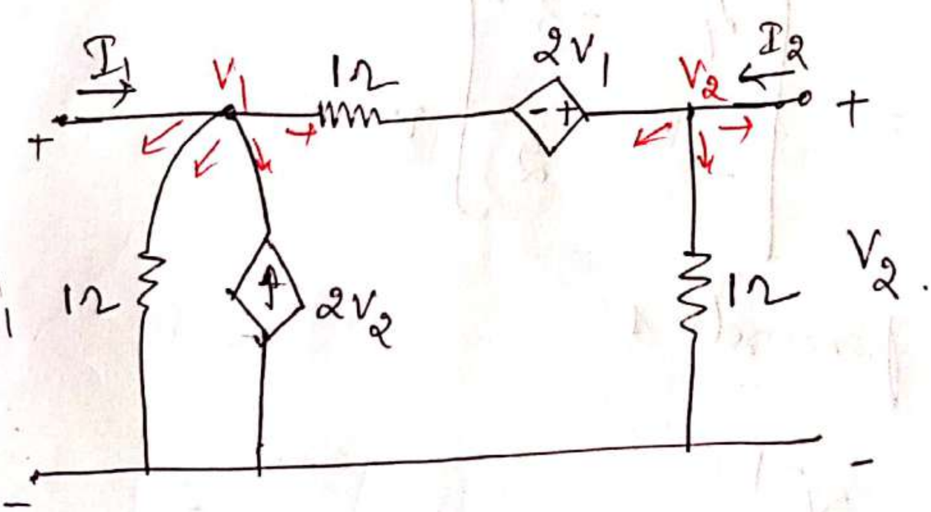
$$I_2 = Y_{21} V_1 + Y_{22} V_2$$

$$Y_{21} = 2\,\mho \qquad Y_{22} = 1.5\,\mho$$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} -1.5 & -1 \\ 2 & 1.5 \end{bmatrix} \mho$$

) Find Y & Z parameters :





$$-I_1+\frac{V_1}{1}-2V_2+\frac{V_1+2V_1-V_2}{1}=0$$

$$-I_1+V_1-2V_2+V_1+2V_1-V_2=0$$

$$I_1=4V_1-3V_2 \quad \text{—— (1)}$$

$\boxed{Y_{11}=4\,\mho}$ $\boxed{Y_{12}=-3\,\mho}$

Apply KCL @ node 2.

$$\frac{V_2-2V_1-V_1}{1}+\frac{V_2}{1}-I_2=0$$

$$I_2=-3V_1+2V_2 \quad \text{—— (2)}$$

$\boxed{Y_{21}=-3\,\mho}$ $\boxed{Y_{22}=2\,\mho}$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}=\begin{bmatrix} 4 & -3 \\ -3 & 2 \end{bmatrix}\mho$$

To find Z- parameters

$$Z=Y^{-1}$$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} & \frac{-Y_{12}}{\Delta Y} \\ \frac{-Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y} \end{bmatrix}$$

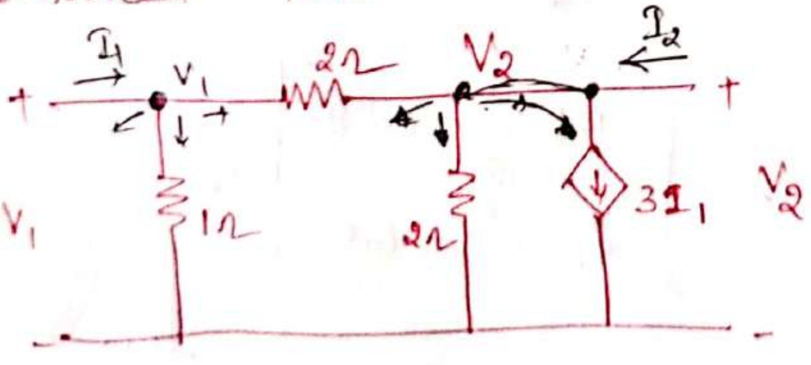
$$\Delta Y = Y_{11} Y_{22} - Y_{12} Y_{21}$$

$$\Delta Y = 4 \times 2 - (-3)(-3)$$

$$\Delta Y = 8 - 9 = -1$$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} -2 & -3 \\ -3 & -4 \end{bmatrix} \Omega$$

4) Find Y & Z parameters for the n/w which contains current controlled src.



KCL @ node 1

$$-I_1 + \frac{V_1}{1} + \frac{V_1 - V_2}{2} = 0$$

$$I_1 = 1.5V_1 - 0.5V_2 \quad \text{—— (1)}$$

on Comparing. $\boxed{Y_{11} = 1.5\,\mho}$ $\boxed{Y_{12} = -0.5\,\mho}$

KCL @ node 2

$$\frac{V_2 - V_1}{2} + \frac{V_2}{2} + 3I_1 - I_2 = 0$$

$$\frac{V_2}{2} - \frac{V_1}{2} + \frac{V_2}{2} + 3I_1 - I_2 = 0$$

$$I_2 = 0.5V_2 - 0.5V_1 + 0.5V_2 + 3I_1$$

$$I_2 = -0.5V_1 + V_2 + 3\underbrace{\left[1.5V_1 - 0.5V_2\right]}_{\text{from eqn (1)}}$$

$$I_2 = 4V_1 - 0.5V_2 \quad \text{—— (2)}$$

on Comparing

$\boxed{Y_{21} = 4\,\mho}$ $\boxed{Y_{22} = -0.5\,\mho}$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 1.5 & -0.5\mho \\ 4 & -0.5 \end{bmatrix} \mho$$

$$Z = Y^{-1} = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} & -\frac{Y_{12}}{\Delta Y} \\ -\frac{Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y} \end{bmatrix}$$

$$\frac{-0.5}{1.25} \quad \frac{+0.5}{1.25}$$

$$\frac{-4}{1.25} \quad \frac{1.5}{1.25}$$

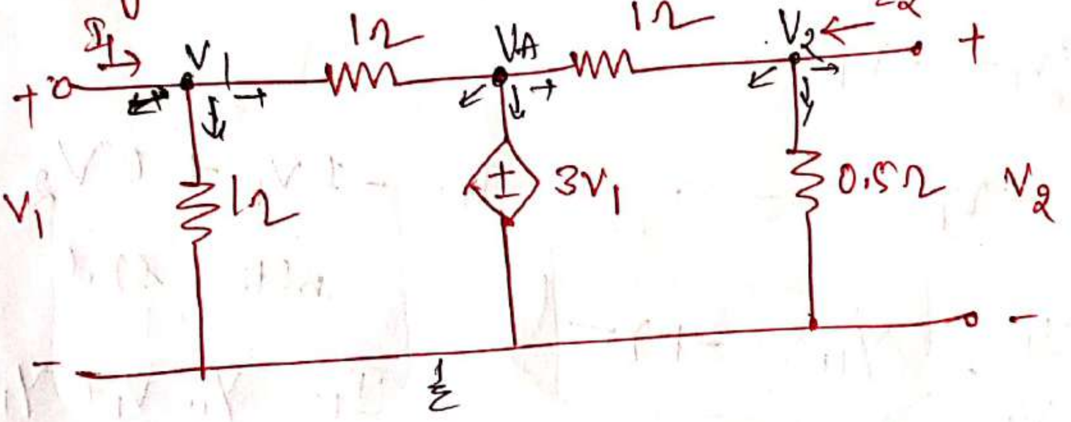
Scanned with CamScanner

$$\Delta Y = Y_{11} Y_{22} - Y_{12} Y_{21}$$

$$\Delta Y = 1.25 \, \mho$$

$$Z = \begin{bmatrix} -0.4 & 0.4 \\ -3.2 & 1.2 \end{bmatrix} \Omega$$

5) Find open circuit impedance parameters



KCL @ node 1

$$-I_1 + \frac{V_1}{1} + \frac{V_1 - V_A}{1} = 0$$

$$I_1 = 2V_1 - V_A \quad \text{——— (1)}$$

@ node A

$$\boxed{V_A = 3V_1} \quad \text{——— (2)}$$

@ node 2

$$\frac{V_2 - V_A}{1} + \frac{V_2}{0.5} - I_2 = 0$$

Scanned with CamScanner

$$V_2 - 3V_1 + 2V_2 = I_2$$

or $I_2 = -3V_1 + 3V_2$ ——— (3)

on comparing with $I_2 = Y_{21}V_1 + Y_{22}V_2$

$\boxed{Y_{21} = -3\,℧}$ $\boxed{Y_{22} = 3\,℧}$

Substitute V_A in eqn (1)

$$I_1 = 2V_1 - 3V_1$$

$I_1 = -V_1 \implies I_1 = -1V_1 + 0V_2$

with std eqn

$\Rightarrow \frac{I_1}{V_1} = \boxed{Y_{11} = -1\,℧}$ $\quad I_1 = Y_{11}V_1 + Y_{12}V_2$.

$\boxed{Y_{12} = 0\,℧}$

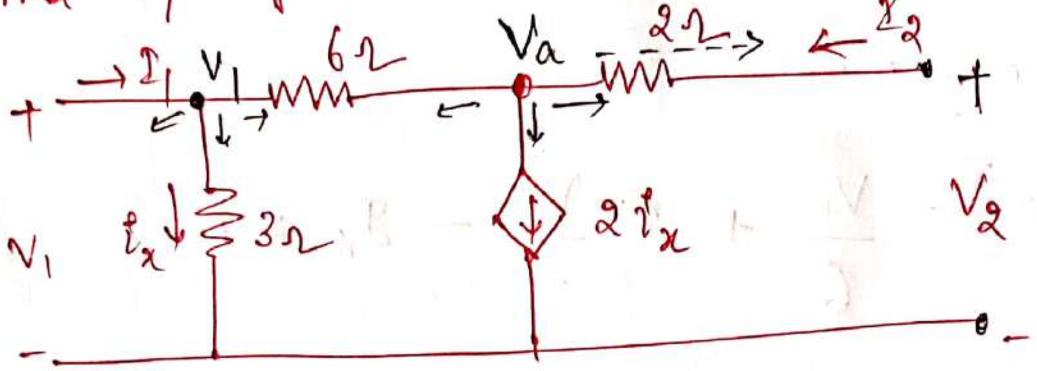
$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ -3 & 3 \end{bmatrix} ℧$$

$$Z = Y^{-1} = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} & -\frac{Y_{12}}{\Delta Y} \\ -\frac{Y_{21}}{\Delta Y} & \frac{Y_{22}}{\Delta Y} \end{bmatrix} = \begin{bmatrix} 3/-3 & 0 \\ \frac{+3}{-3} & \frac{-1}{-3} \end{bmatrix}$$

$$\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21} = -3$$

$$Z = \begin{bmatrix} -1 & 0 \\ -1 & 1/3 \end{bmatrix} \Omega$$

6) find Y parameters



KCL @ node 1

$$-I_1 + \frac{V_1}{3} + \frac{V_1 - V_a}{6} = 0 \quad \text{—— (1)}$$

KCL @ node a

$$\frac{V_a - V_1}{6} + 2i_x - I_2 = 0 \quad \text{—— (2)}$$

from the figure,

$$i_x = \frac{V_1}{3}$$

& $$I_2 = \frac{V_2 - V_a}{2}$$

$$2I_2 = V_2 - V_a \implies V_a = V_2 - 2I_2$$

eqn (1) becomes

$$-I_1 + \frac{V_1}{3} + \frac{V_1}{6} - \frac{1}{6}\left[V_2 - 2I_2\right]$$

$$I_1 = \frac{V_1}{3} + \frac{V_1}{6} - \frac{V_2}{6} + \frac{2I_2}{6}$$

$$I_1 - 0.33 I_2 = 0.5 V_1 - 0.166 V_2 \quad \text{———} \quad (*)$$

eqn ② becomes.

$$\frac{(V_2 - 2I_2)}{6} - \frac{V_1}{6} + 2 \times \frac{V_1}{3} - I_2 = 0$$

$$\frac{V_2}{6} - \frac{I_2}{3} - \underbrace{\frac{V_1}{6} + \frac{2V_1}{3}}_{} - I_2 = 0$$

or $0.5V_1 + 0.166 V_2 = I_2 + I_2/3 = 1.33 I_2$

or $I_2 = 0.375 V_1 + 0.125 V_2$ ——— ③

on comparing with $I_2 = Y_{21} V_1 + Y_{22} V_2$.

$$\boxed{Y_{21} = 0.375\ \mho} \qquad \boxed{Y_{22} = 0.125\ \mho}$$

from (*)

$$I_1 = 0.5V_1 - 0.166 V_2 + 0.33\underbrace{(0.375 V_1 + 0.125 V_2)}_{}$$

$$I_1 = 0.5 V_1 - 0.166 V_2 + 0.1237 V_1 + 0.041 V_2$$

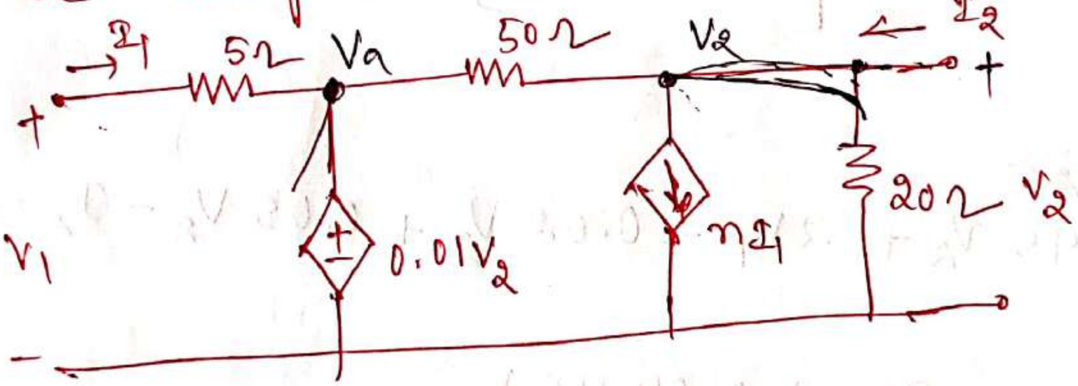
$$I_1 = 0.625V_1 - 0.125V_2.$$

on comparing with $I_1 = Y_{11}V_1 + Y_{12}V_2$

$$\boxed{Y_{11} = 0.625\ \mho} \quad \boxed{Y_{12} = -0.125\ \mho}$$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 0.625 & -0.125 \\ 0.375 & 0.125 \end{bmatrix} \mho$$

7) Find Y_{12} & Y_{21} for the n/w for $n=10$. what is the value of 'n' for the n/w to be reciprocal.



from the figure

$$\boxed{V_a = 0.01V_2} \quad \text{——— ①}$$

KCL @ node 2.

$$\frac{V_2 - V_a}{50} + nI_1 + \frac{V_2}{20} - I_2 = 0 \quad \text{——— ②}$$

$$\frac{V_2}{50} - \frac{0.01 V_2}{50} + 10 I_1 + \frac{V_2}{20} - I_2 = 0$$

Va

$$0.0198 V_2 + 10 I_1 + \frac{V_2}{20} - I_2 = 0$$

from the fig

$$I_1 = \frac{V_1 - V_a}{5}$$

$$I_1 = \frac{V_1 - 0.01 V_2}{5} \quad \text{——— (3)}$$

$$0.0198 V_2 + 10 \left[\frac{V_1 - 0.01 V_2}{5}\right] + \frac{V_2}{20} - I_2 = 0$$

$$0.0198 V_2 + 2V_1 - 0.02 V_2 + 0.05 V_2 - I_2 = 0$$

$$I_2 = 2V_1 + 0.0498 V_2$$

Comparing with std eqn.

$$I_2 = Y_{21} V_1 + Y_{22} V_2$$

$$\boxed{Y_{21} = 2 \mho} \qquad \boxed{Y_{22} = 0.0498 \mho}$$

$5I_1 = V_1 - 0.01\, V_2$

$I_1 = 0.2V_1 - 0.002\, V_2$

Comparing with $I_1 = Y_{11} V_1 + Y_{12} V_2$

$\boxed{Y_{11} = 0.2\,℧}$ $\boxed{Y_{12} = -0.002\,℧}$

Conditions for reciprocity

$Y_{12} = Y_{21}$

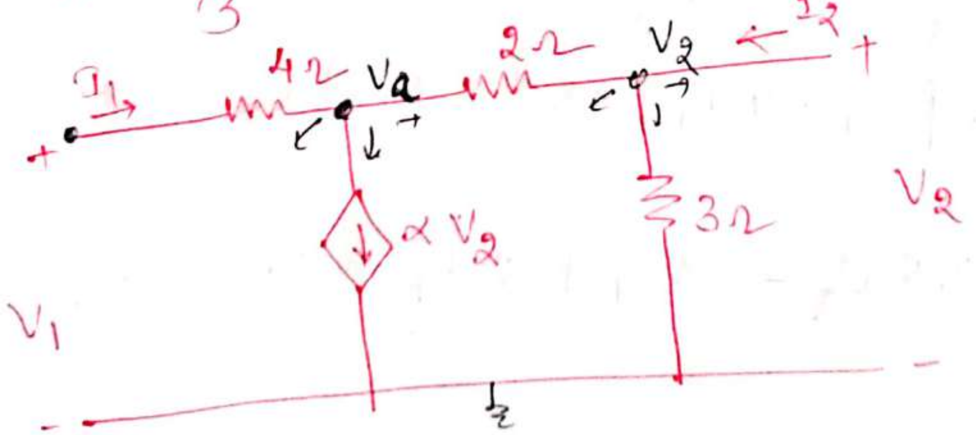
$-0.002 = 2$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 0.2 & -0.002 \\ 2 & 0.0498 \end{bmatrix}$$

$\boxed{n = 0.001}$ or $\boxed{n = 1000}$

** 8) Find the Z-parameters for the n/w take

$\alpha = 4/3$



KCL @ node a

$\cancel{-I_1+I_2}$ $\quad -I_1 + \alpha V_2 + \dfrac{V_a - V_2}{2} = 0$

$$I_1 = \frac{4}{3} V_2 + \frac{V_a}{2} - \frac{V_2}{2} \quad \text{—— } ①$$

KCL @ node 2 :

$$\frac{V_2 - V_a}{2} + \frac{V_2}{3} - I_2 = 0$$

$$\frac{V_2}{2} - \frac{V_a}{2} + \frac{V_2}{3} - I_2 = 0 \quad \text{—— } ②$$

from the $\quad I_1 = \dfrac{V_1 - V_a}{4}$

$$4I_1 = V_1 - V_a$$

$$V_a = \underline{\underline{V_1}} - 4I_1$$

Eqn ② becomes

$$0.5\, V_2 - [V_1 - 4I_1] \times 0.5 + 0.33\, V_2 = I_2$$

or $\quad I_2 = 0.5V_2 - 0.5V_1 + 2\underline{\underline{I_1}} + 0.33\, V_2 \quad \text{—— } ②^*$

Eqn ① becomes.

$$I_1 = 1.33V_2 + \frac{(V_1 - 4I_1)}{2} - 0.5V_2$$

$$I_1 = 1.33V_2 + 0.5V_1 - 2I_1 - 0.5V_2$$

$$3I_1 = 0.5V_1 + 0.83V_2$$

or $I_1 = 0.166V_1 + 0.2766V_2$ —— (3)

Comparing with $I_1 = Y_{11}V_1 + Y_{12}V_2$

$\boxed{Y_{11} = 0.166\ \mho}$ $\boxed{Y_{12} = 0.2766\ \mho}$

Substituting (3) in (2)*

$$I_2 = 0.5V_2 - 0.5V_1 + 2[0.166V_1 + 0.2766V_2] + 0.33V_2.$$

$$I_2 = -0.168V_1 + 1.386V_2$$

Comparing with $I_2 = Y_{21}V_1 + Y_{22}V_2$

$\boxed{Y_{21} = -0.168\ \mho}$ $\boxed{Y_{22} = 1.386\ \mho}$

$$Z = Y^{-1} = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} & \frac{-Y_{12}}{\Delta Y} \\ \frac{-Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y} \end{bmatrix}$$

$$\Delta Y = Y_{11} Y_{22} - Y_{12} Y_{21}$$

$$\Delta Y = 0.276$$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \frac{1.386}{0.276} & \frac{-0.2766}{0.276} \\ \frac{-(-0.168)}{0.276} & \frac{0.166}{0.276} \end{bmatrix}$$

$$[Z] = \begin{bmatrix} 5.02 & -1 \\ 0.608 & 0.6 \end{bmatrix} \Omega$$

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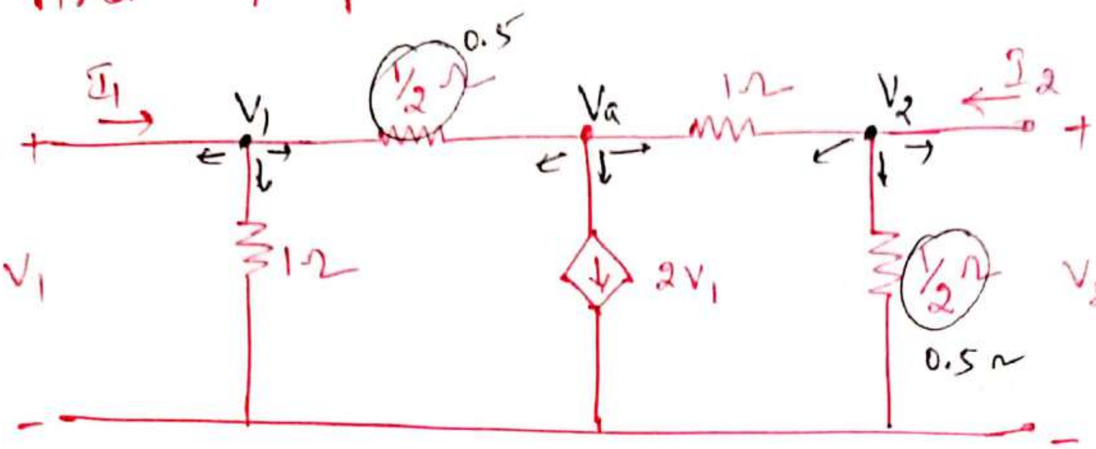
Q) find Y paramelers



KCL @ node 1

$$-I_1 + \frac{V_1}{1} + \frac{V_1 - V_a}{0.5} = 0$$

$$-I_1 + V_1 + \frac{V_1}{0.5} - \frac{V_a}{0.5} = 0 \quad \text{——} \quad (1)$$

@ node a:

$$\frac{V_a - V_1}{0.5} + 2V_1 + \frac{V_a - V_2}{1} = 0$$

$$\frac{V_a}{0.5} - \cancel{\frac{V_1}{0.5}}^{\,2V_1} + \cancel{2V_1} + V_a - V_2 = 0$$

$$2V_a + \cancel{2V_1} + V_a - V_2 = 0 \quad \text{——} \quad (2)$$

@ node 2

$$\frac{V_2 - V_a}{1} + \frac{V_2}{0.5} - I_2 = 0$$

$$V_2 - V_a + 2V_2 - I_2 = 0 \quad \text{---} (3)$$

from (2)

$$3V_a = V_2$$

$$\boxed{V_a = \frac{V_2}{3}}$$

$\therefore$ eqn (1) becomes.

$$-I_1 + V_1 + \frac{V_1}{0.5} - \frac{V_2}{3 \times 0.5} = 0$$

or $I_1 = 3V_1 - 0.666\, V_2$

$\therefore$ $\boxed{Y_{11} = 3\, \mho}$ $\boxed{Y_{12} = -0.66\, \mho}$

eqn (3) becomes,

$$V_2 - \frac{V_2}{3} + \frac{V_2}{0.5} = I_2$$

or $I_2 = 2.667\, V_2$

$\therefore$ $I_2 = 0\, V_1 + 2.667\, V_2$

$\boxed{Y_{21} = 0\, \mho}$ $\boxed{Y_{22} = 2.667\, \mho}$

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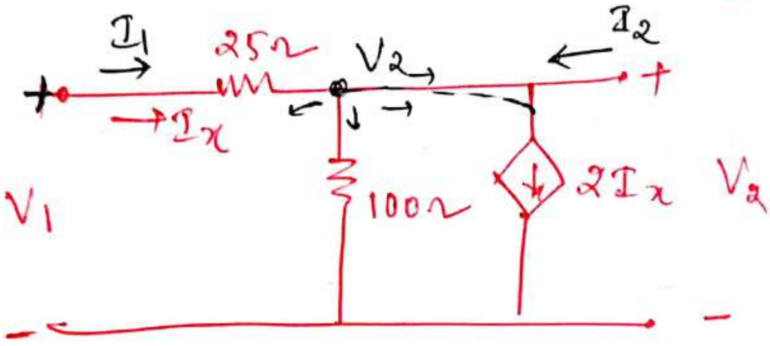
$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 3 & -0.66 \\ 0 & 2.667 \end{bmatrix} \mho.$$

10) Find the Y parameters of the n/w shown



→ KCL @ node 2 :

$$-I_1 + \frac{V_2}{100} + 2I_x - I_2 = 0$$

from the fig.

$$\boxed{I_x = I_1} \quad \text{—— (1)}$$

$$-I_1 + \frac{V_2}{100} + 2I_1 - I_2 = 0 \quad \text{—— (2)}$$

from the figure,

$$I_1 = \frac{V_1 - V_2}{25}$$

$$I_1 = 0.04\,V_1 - 0.04\,V_2 \quad \text{—— (3)}$$

Comparing with std eqn

$$\boxed{Y_{11} = 0.04\,\mho} \quad \boxed{Y_{12} = -0.04\,\mho}$$

from eq ②,

$$I_1 + 0.01 V_2 - I_2 = 0$$

$$I_2 = I_1 + 0.01 V_2$$

Substituting ③ in the above eqn

$$I_2 = [0.04 V_1 - 0.04 V_2] + 0.01 V_2$$

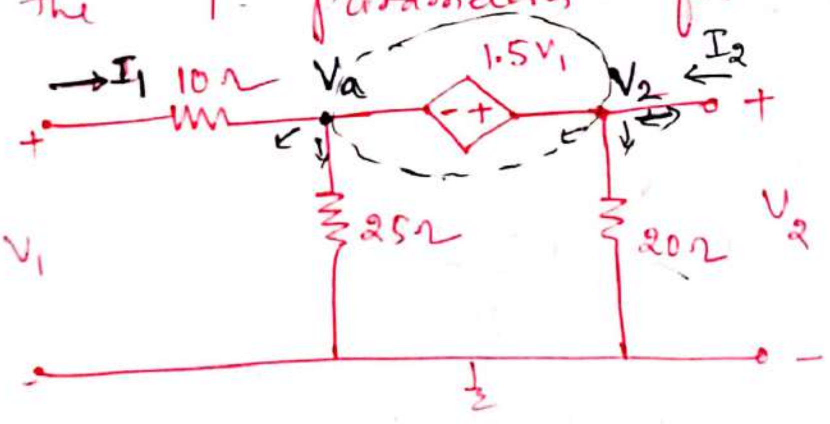
$$I_2 = 0.04 V_1 - 0.03 V_2 \quad \text{—— ④}$$

Comparing with Std eqn

$\boxed{Y_{21} = 0.04 \, \mho}$ $\boxed{Y_{22} = -0.33 \, \mho}$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 0.04 & -0.04 \\ 0.04 & -0.03 \end{bmatrix} \mho$$

11) Find the T parameters for the n/w.



Since $1.5V_1$ is b/w V_a & V_2 it leads to super node.

$$V_2 - V_a = 1.5 V_1 \quad \text{—— ①}$$

Applying KCL to super node.

$$-I_1 + \frac{V_a}{25} + \frac{V_2}{20} - I_2 = 0 \qquad \text{--- (2)}$$

from the fig.

$$I_1 = \frac{V_1 - V_a}{10}$$

$$10 I_1 = V_1 - V_a$$

$$\boxed{V_a = V_1 - 10 I_1}$$

Eqn (1) becomes.

$$V_2 - [V_1 - 10 I_1] - 1.5 V_1 = 0$$

$$V_2 - V_1 + 10 I_1 - 1.5 V_1 = 0$$

$$10 I_1 = 2.5 V_1 - V_2$$

$$\text{or } I_1 = 0.25 V_1 - 0.1 V_2$$

Comparing with std eqn.

$$\boxed{Y_{11} = 0.25 \,\mho} \qquad \boxed{Y_{12} = -0.1 \,\mho}$$

Eqn (2) is now.

$$I_2 = -[0.25 V_1 - 0.1 V_2] + 0.04 [V_1 - 10 I_1] + 0.05 V_2$$

$$I_2 = -0.25 V_1 + 0.1 V_2 + 0.04 V_1 - 0.4 I_1 + 0.05 V_2$$

$$I_2 = -0.25V_1 + 0.1V_2 + 0.04V_1 - 0.4\left[0.25V_1 - 0.1V_2\right] + 0.05V_2$$

$$I_2 = -0.21V_1 + 0.15V_2 - 0.1V_1 + 0.04V_2$$

$$\boxed{I_2 = -0.31V_1 + 0.19V_2}$$

Comparing with std eqn.

$\boxed{Y_{21} = -0.31\,\mho}$ $\boxed{Y_{22} = 0.19\,\mho}$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 0.25 & -0.1 \\ -0.31 & 0.19 \end{bmatrix} \mho$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0.633 & 3.23 \\ 0.053 & 0.05 \end{bmatrix}$$

$V_1 = AV_2 - BI_2$ — (1)　　$I_1 = Y_{11}V_1 + Y_{12}V_2$ — (3)

$I_1 = CV_2 - DI_2$ — (2)　　$I_2 = Y_{21}V_1 + Y_{22}V_2$ — (4)

$$Y_{21}V_1 = I_2 - Y_{22}V_2$$

$$V_1 = -\frac{Y_{22}}{Y_{21}}V_2 + \frac{1}{Y_{21}}I_2 \quad \text{— (5)}$$

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$$A = \frac{-Y_{22}}{Y_{21}} = -\frac{0.19}{-0.31} = 0.633$$

$$B = -\frac{1}{Y_{21}} = \frac{-1}{-0.31} = 3.23$$

eqn ③ becomes.

$$I_1 = Y_{11}\left[-\frac{Y_{22}}{Y_{21}} V_2 + \frac{1}{Y_{21}} I_2\right] + Y_{12} V_2 .$$

$$I_1 = -\frac{Y_{11} Y_{22}}{Y_{21}} V_2 + \frac{Y_{11}}{Y_{21}} I_2 + Y_{12} V_2$$

$$I_1 = \frac{(-Y_{11} Y_{22} + Y_{21} Y_{12})}{Y_{21}} V_2 + \frac{Y_{11}}{Y_{21}} I_2$$

$$I_1 = \underbrace{\frac{-\Delta Y}{Y_{21}}}_{C} V_2 + \underbrace{\frac{Y_{11}}{Y_{21}}}_{D} I_2$$

$$C = \frac{-\Delta Y}{Y_{21}} \qquad D = -\frac{Y_{11}}{Y_{21}} = -\frac{0.25}{-0.31} = 0.05$$

$$\Delta Y = 0.25 \times 0.19 - [(-0.1)(-0.31)] = 0.0165$$

$$C = 0.053$$

12) The eqns that describes behaviour of the n/w are

$11 I_1 + 4 I_2 = 5V_1$

$4 I_1 + 6 I_2 = 5V_2$. Find Y parameters.

Given $5V_1 = 11 I_1 + 4 I_2$

$V_1 = \frac{11}{5} I_1 + \frac{4}{5} I_2$

$V_1 = 2.2 I_1 + 0.8 I_2$ —— ①

$5V_2 = 4 I_1 + 6 I_2$

$V_2 = \frac{4}{5} I_1 + \frac{6}{5} I_2$

$V_2 = 0.8 I_1 + 1.2 I_2$ —— ②

WKT $V_1 = Z_{11} I_1 + Z_{12} I_2$ —— ③

$V_2 = Z_{21} I_1 + Z_{22} I_2$ —— ④

From ① & ③

$\boxed{Z_{11} = 2.2\,\Omega}$ & $\boxed{Z_{12} = 0.8\,\Omega}$

From ② & ④

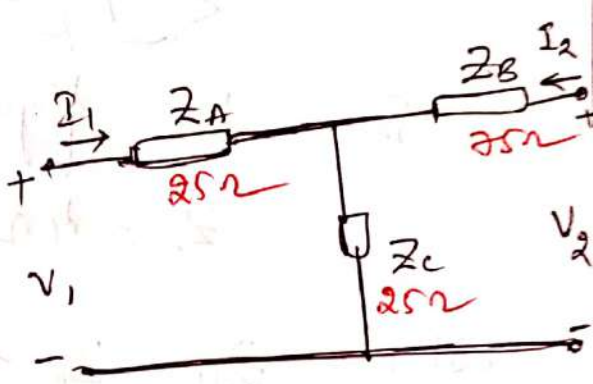
$\boxed{Z_{21} = 0.8\,\Omega}$ & $\boxed{Z_{22} = 1.2\,\Omega}$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 2.2 & 0.8 \\ 0.8 & 1.2 \end{bmatrix}$$

13) The impedance parameters of the T n/w are given by $\begin{bmatrix} 50 & 25 \\ 25 & 100 \end{bmatrix}$. Find the parameters of the T- n/w.

Given $\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 50 & 25 \\ 25 & 100 \end{bmatrix}$

WKT $Z_{11} = Z_A + Z_C$



$Z_{22} = Z_B + Z_C$

& $Z_{12} = Z_{21} = Z_C$

$\therefore \boxed{Z_C = 25\Omega}$

$\therefore Z_A = Z_{11} - Z_C$

$Z_A = 50 - 25$

$\boxed{Z_A = 25\Omega}$

& $Z_B = Z_{22} - Z_C$

$Z_B = 100 - 25$ $\boxed{Z_B = 75\Omega}$

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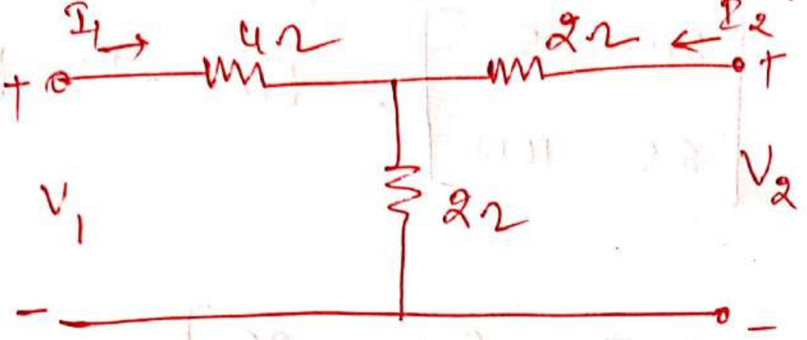
14) Determine Y parameters of the T-n/w



For T-n/w first find Z & then

$$\boxed{Y = Z^{-1}}$$

from the figure

$Z_A = 4\Omega$, $Z_B = 2\Omega$, $Z_C = 2\Omega$

WKT $Z_{11} = Z_A + Z_C$ $\qquad Z_{12} = Z_{21} = Z_C$

$\boxed{Z_{11} = 6\Omega}$ $\qquad \boxed{Z_{12} = Z_{21} = 2\Omega}$

& $Z_{22} = Z_B + Z_C$

$\boxed{Z_{22} = 4\Omega}$

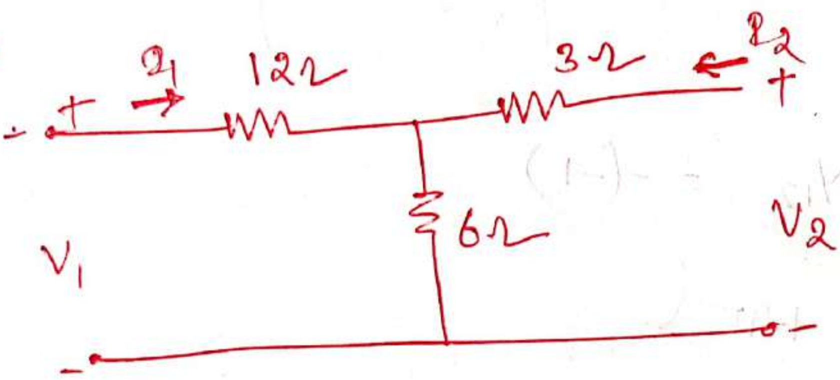
$$\therefore \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 6 & 2 \\ 2 & 4 \end{bmatrix} \Omega$$

$$Y = Z^{-1} = \begin{bmatrix} \frac{Z_{22}}{\Delta Z} & \frac{-Z_{12}}{\Delta Z} \\ \frac{-Z_{21}}{\Delta Z} & \frac{Z_{11}}{\Delta Z} \end{bmatrix}$$

$\Delta Z = 24 - 4 = 20$

$$\therefore \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 0.2 & -0.1 \\ -0.1 & 0.3 \end{bmatrix} \mho$$

15) Find the Z-parameters of the n/w shown below



$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 18 & 6 \\ 6 & 9 \end{bmatrix} \Omega.$$

16) The port current of a two-port n/w are given by

$I_1 = 2.5 V_1 - V_2$

$I_2 = -V_1 + 5V_2$

Find equivalent π n/w.

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 2.5 & -1 \\ -1 & 5 \end{bmatrix} \mho$$

The admittances of π n/w are, Y_A, Y_B & Y_C

$\cancel{Y_A = Y_{11} + Y_{12}}$

$\cancel{Y_A = 2.5 - 1 = 1.5\mho}$

$\cancel{Y_A = 1.5\mho}$

$\cancel{Y_B = Y}$

$Y_{11} = Y_A + Y_C$

$Y_{22} = Y_B + Y_C$

& $Y_{12} = Y_{21} = -Y_C$

$Y_C = -Y_{12} = -(-1)$

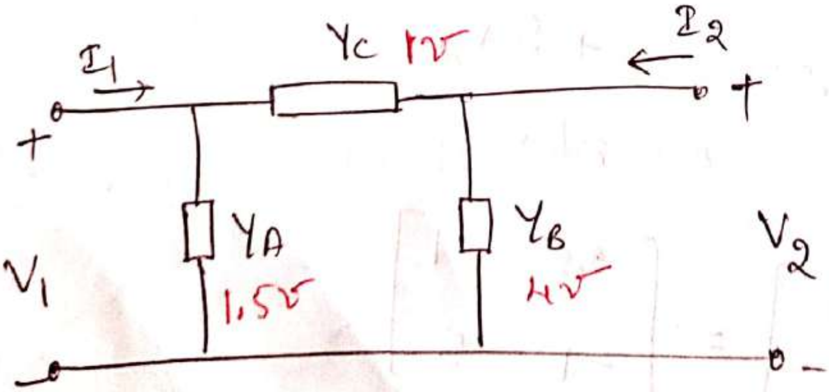
$\boxed{Y_C = 1\mho}$

$Y_A = Y_{11} - Y_C$

$Y_A = 2.5 - 1 = 1.5\mho$

$Y_B = Y_{22} - Y_C$

$Y_B = 5 - 1 = 4\mho$



17) The Z- parameters of a two port n/w are

$Z_{11} = 20\Omega$, $Z_{12} = 10\Omega$, $Z_{21} = 10\Omega$ & $Z_{22} = 10\Omega$.

find its Y & ABCD parameters.

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{Z_{22}}{\Delta Z} & \frac{-Z_{12}}{\Delta Z} \\ \frac{-Z_{21}}{\Delta Z} & \frac{Z_{11}}{\Delta Z} \end{bmatrix}$$

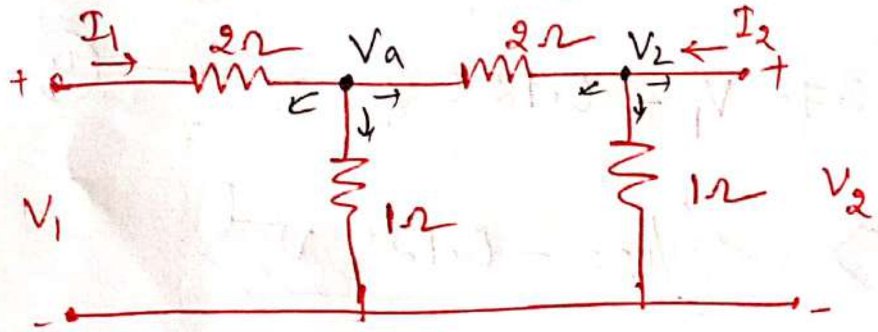
$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{Z_{11}}{Z_{21}} & \frac{\Delta Z}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{bmatrix}$$

$$\Delta Z = Z_{11} Z_{22} - Z_{12} Z_{21}$$

[illegible] Shown :

18) Find Z-parameters of the n/w shown.

June/July-19



→ Apply KCL @ node a

$$\frac{V_a}{1} + \frac{V_a - V_2}{2} - I_1 = 0$$

$$I_1 = 1.5V_a - 0.5V_2 \quad \text{———} \quad (1)$$

→ KCL @ node 2

$$\frac{V_2 - V_a}{2} + \frac{V_2}{1} - I_2 = 0$$

$$I_2 = 1.5V_2 - 0.5V_a \quad \text{———} \quad (2)$$

from the figure.

$$I_1 = \frac{V_1 - V_a}{2} \Rightarrow 2I_1 = V_1 - V_a$$

$$\text{* or } V_a = V_1 - 2I_1 \quad \text{———} \quad (3)$$

Substitute (3) in (1)

$$I_1 = 1.5\left[V_1 - 2I_1\right] - 0.5V_2$$

$$I_1 = 1.5V_1 - 3I_1 - 0.5V_2$$

$$4I_1 = 1.5V_1 - 0.5V_2$$

$$I_1 = 0.375\,V_1 - 0.125\,V_2 \quad \text{———— (4)}$$

$$\boxed{Y_{11} = 0.375\ \mho} \qquad \boxed{Y_{12} = -0.125\ \mho}$$

Substitute (3) in (2)

$$I_2 = 1.5V_2 - 0.5\left[V_1 - 2I_1\right]$$

$$I_2 = 1.5\,V_2 - 0.5\,V_1 + I_1$$

$$I_2 = 1.5V_2 - 0.5\,V_1 + 0.375\,V_1 - 0.125\,V_2$$

$$I_2 = -0.125V_1 + 1.375\,V_2$$

$$\boxed{Y_{21} = -0.125\mho} \qquad \boxed{Y_{22} = 1.375\ \mho}$$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 0.375 & -0.125 \\ -0.125 & 1.375 \end{bmatrix} \mho$$

$$Z = Y^{-1} = \begin{bmatrix} \dfrac{Y_{22}}{\Delta Y} & \dfrac{-Y_{12}}{\Delta Y} \\[2ex] \dfrac{-Y_{21}}{\Delta Y} & \dfrac{Y_{11}}{\Delta Y} \end{bmatrix}$$

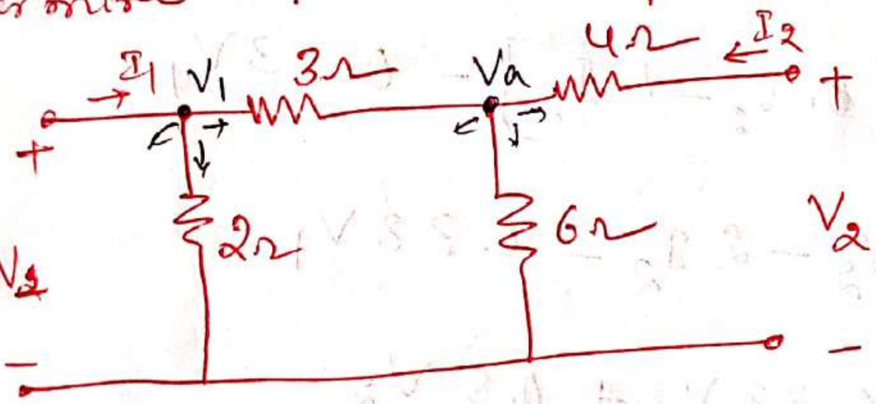
$$\Delta Y = Y_{11} Y_{22} - Y_{12} Y_{21}$$

$$= 0.375 \times 1.375 - (-0.125)(-0.125)$$

$$= 0.51 - 0.015 = \cancel{0.2225}\ 0.5$$

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 2.75 & 0.25 \\ 0.25 & 0.75 \end{bmatrix} \Omega$$

19) Determine Y & Z parameters:



KCL @ node V_1

$$-I_1 + \frac{V_1}{2} + \frac{V_1 - V_a}{3} = 0$$

$$0.5 V_1 + 0.33 V_1 - 0.33 V_a - I_1 = 0$$

or $I_1 = 0.83 V_1 - 0.33 V_a$ ——— (1)

KCL @ node V_a

$$\frac{V_a - V_1}{3} + \frac{V_a}{6} - I_2 = 0$$

Scanned with CamScanner

or $I_2 = 0.5 V_a - 0.33 V_1$ —— (2)

from the fig.

$$I_2 = \frac{V_2 - V_a}{4}$$

$$4 I_2 = V_2 - V_a$$

or $V_a = V_2 - 4 I_2$ —— (3)

Substitute (3) in (2)

$$I_2 = 0.5\left[\cancel{0.}\, V_2 - 4 I_2\right] - 0.33 V_1$$

$$I_2 = 0.5 V_2 - 2 I_2 - 0.33 V_1$$

$$3 I_2 = -0.33 V_1 + 0.5 V_2$$

$$I_2 = -0.11 V_1 + 0.166 V_2 \text{ —— *}$$

Comparing with Std eqn $Y_{21} = -0.11\,\mho$

& $Y_{22} = 0.166\,\mho$

Now (3) in (1) becomes.

$$I_1 = 0.83 V_1 - 0.33\left[V_2 - 4 I_2\right]$$

Scanned with CamScanner

$$I_1 = 0.83V_1 - 0.33V_2 + 1.32\, I_2$$

$$I_1 = 0.83V_1 - 0.33V_2 + 1.32\Big[\underbrace{-0.11V_1 + 0.166V_2}_{I_2 \text{ eqn } (*)}\Big]$$

$$I_1 = 0.83V_1 - 0.33V_2 - 0.145V_1 + 0.219V_2$$

$$I_1 = 0.685V_1 - 0.111V_2$$

Comparing with std eqn $I_1 = Y_{11}V_1 + Y_{12}V_2$

$$\boxed{Y_{11} = 0.685\,\mho} \quad \boxed{Y_{12} = -0.111\,\mho}$$

$$\therefore \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 0.685 & -0.111 \\ -0.111 & 0.166 \end{bmatrix} \mho$$

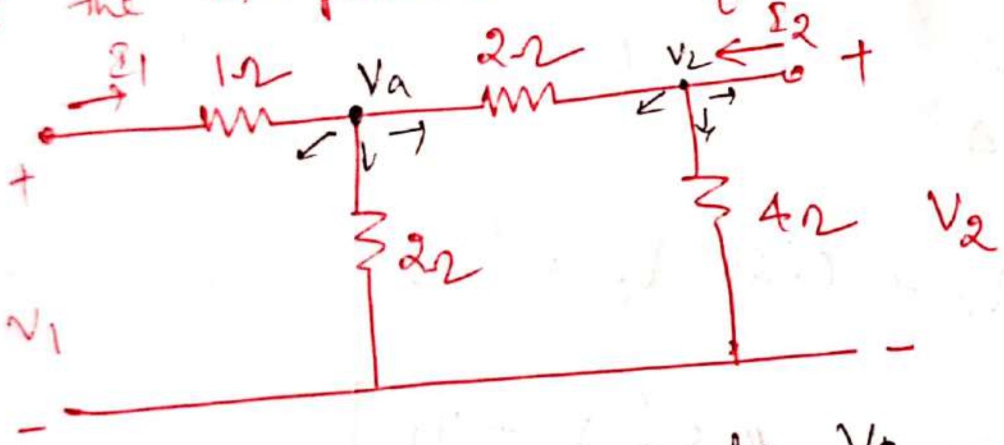
$$Z = Y^{-1} = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} & \frac{-Y_{12}}{\Delta Y} \\ \frac{-Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y} \end{bmatrix}$$

$$\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21} = 0.113 - [0.0123]$$

$$\underline{\underline{\Delta Y = 0.1}}$$

$$\therefore \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 1.66\,\Omega & 1.1 \\ 1.1 & 6.8 \end{bmatrix} \Omega$$

2) Find the h-parameters of the ckt shown NOV-2020 (ACV)



KCL method

Apply KCL at node V_a

$$\frac{V_a - V_2}{2} + \frac{V_a}{2} - I_1 = 0$$

$$I_1 = \frac{V_a - V_2}{2} \quad \text{——— (1)}$$

from the fig $I_1 = \dfrac{V_1 - V_a}{1}$

$$V_a = V_1 - I_1 \quad \text{——— (2)}$$

substitute ② in ①

$$I_1 = V_1 - I_1 - \frac{V_2}{2}$$

$$2I_1 = V_1 - V_2/2$$

$$\cancel{I_1 = 0.5 V_1 - 0.8 V_2}$$

$$I_1 = 0.5 V_1 - 0.25 V_2 \quad \text{——— ③}$$

$$\boxed{Y_{11} = 0.5\ \mho} \qquad \boxed{Y_{12} = -0.25\ \mho}$$

KCL @ node 2

$$\frac{V_2 - V_a}{2} + \frac{V_2}{4} - I_2 = 0$$

$$0.5 V_2 - 0.5 V_a + 0.25 V_2 = I_2$$

or $I_2 = 0.75 V_2 - 0.5 \left[V_1 - I_1 \right]$

$$I_2 = 0.75 V_2 - 0.5 V_1 + 0.5 \Big[\underbrace{0.5 V_1 - 0.25 V_2}_{\text{eqn ③ } I_1} \Big]$$

$$I_2 = 0.75 V_2 - 0.5 V_1 + 0.25 V_1 - 0.125 V_2$$

$$I_2 = -0.25 V_1 + 0.625 V_2 \quad \text{——— ④}$$

$$Y_{21} = -0.25\,\mho \qquad Y_{22} = 0.625\,\mho$$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 0.5 & -0.25 \\ -0.25 & 0.625 \end{bmatrix} \mho$$

WKT, $$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} 1/Y_{11} & -\frac{Y_{12}}{Y_{11}} \\ \frac{Y_{21}}{Y_{11}} & \frac{\Delta Y}{Y_{11}} \end{bmatrix}$$

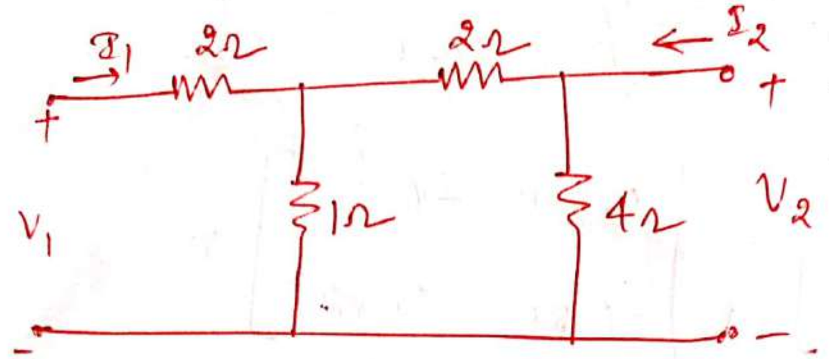
$$\Delta Y = Y_{11} Y_{22} - Y_{12} Y_{21}$$

$$\Delta Y = 0.25$$

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} 1/0.5 & -\frac{(-0.25)}{0.5} \\ \frac{-0.25}{0.5} & \frac{0.25}{0.5} \end{bmatrix}$$

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} 2 & 0.5 \\ -0.5 & 0.5 \end{bmatrix}$$

21) S.T the n/w is reciprocal but not symmetrical by finding h parameters.



Ans :- $\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} 2.66 & 0.33 \\ -0.33 & 0.59 \end{bmatrix}$

Since $h_{12} = -h_{21}$

$$0.33 = -(-0.33)$$

$$0.33 = 0.33$$

$\therefore$ The n/w is reciprocal.

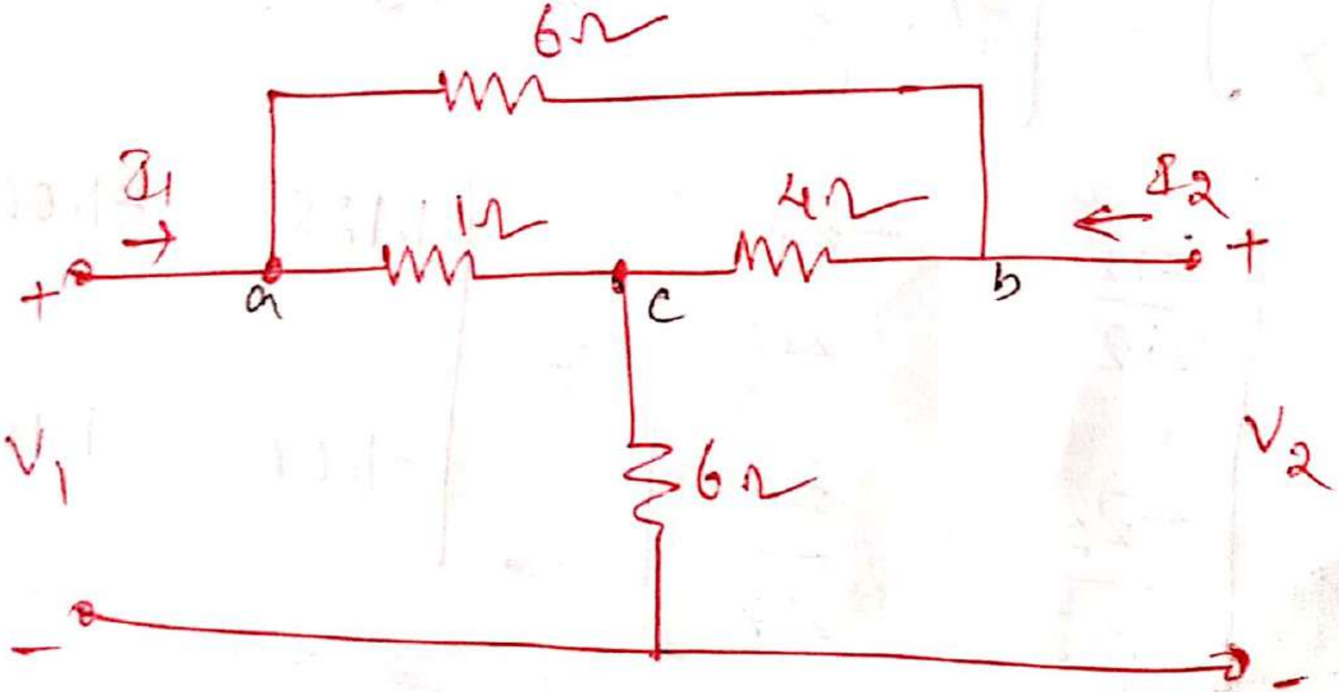
$$\Delta h = \begin{vmatrix} 2.66 & 0.33 \\ -0.33 & 0.59 \end{vmatrix}$$

$$\Delta h = 1.67$$

Since $\Delta h \neq 1$ $\therefore$ the n/w is not Symmetrical.

method.

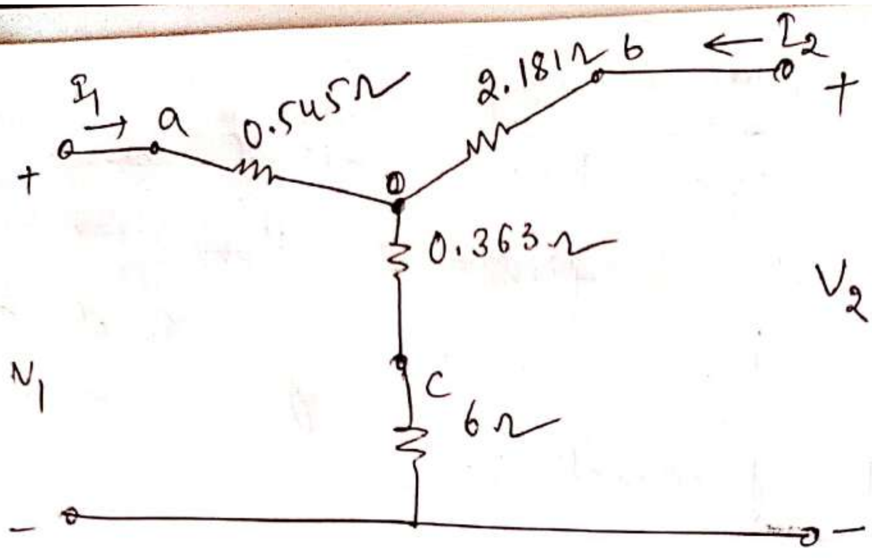
22) Find the Y- parameters

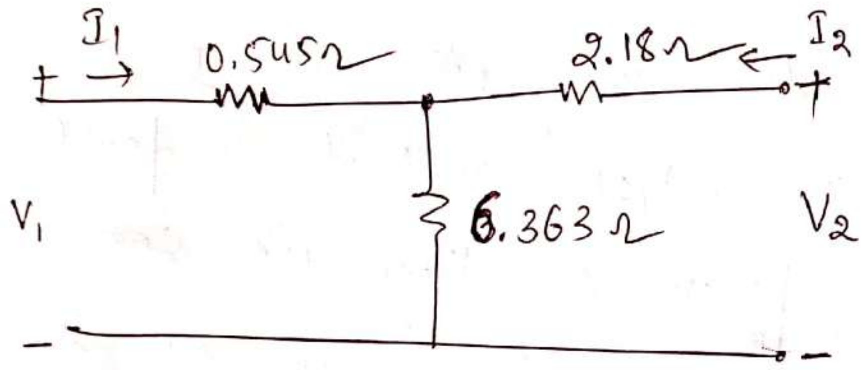


$R_1 = 0.545\ \Omega$

$R_2 = 2.18\ \Omega$

$R_3 = 0.363\ \Omega$





Since T- n/w,

$Z_{11} = 6.908\,\Omega \qquad Z_{12} = Z_{21} = 6.363\,\Omega$

$Z_{22} = 8.54\,\Omega$

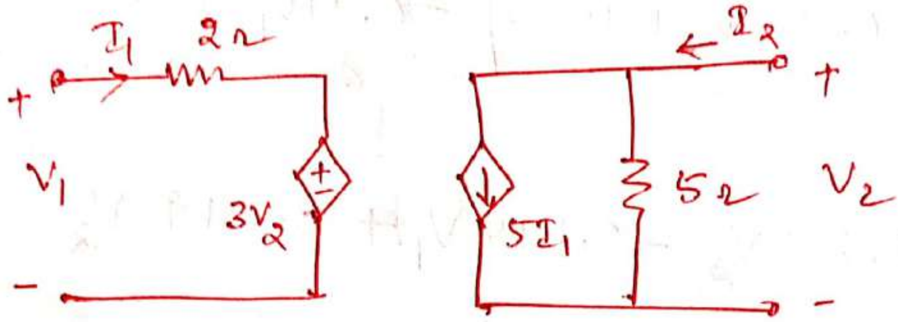
$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 6.908 & 6.363 \\ 6.363 & 8.54 \end{bmatrix} \Omega$$

$$Y = Z^{-1} = \begin{bmatrix} \frac{Z_{22}}{\Delta Z} & \frac{-Z_{12}}{\Delta Z} \\ \frac{-Z_{21}}{\Delta Z} & \frac{Z_{11}}{\Delta Z} \end{bmatrix} = \begin{bmatrix} 1.125 & -1.06 \\ -1.06 & 1.15 \end{bmatrix} \mho$$

$\Delta Z = 5.97\,\Omega$

23) Determine the transmission parameters for the n/w shown below

June/July - 2019



WKT Transmission parameters,

$$V_1 = AV_2 - BI_2 \quad \text{——} (1)$$

$$I_1 = CV_2 - DI_2 \quad \text{——} (2)$$

By KVL (to the LHS side)

$$+V_1 - 2I_1 - 3V_2 = 0$$

or $$V_1 = 2 I_1 + 3V_2 \quad \text{——} (3)$$

By KCL (to the RHS side)

$$I_2 = \frac{V_2}{5} + 5I_1$$

$$5I_1 = I_2 - 0.2V_2$$

$$I_1 = -\frac{0.2}{5}V_2 + \frac{I_2}{5}$$

$$I_1 = -0.04\,V_2 + 0.2\,I_2 \quad \text{——} (4)$$

Compare (4) & (2)

$\boxed{C = -0.04}$ $\boxed{D = -0.2}$

Substituting (4) in (3)

$$V_1 = 2\left[-0.04V_2 + 0.2I_2\right] + 3V_2$$

$$V_1 = -0.08V_2 + 0.4I_2 + 3V_2$$

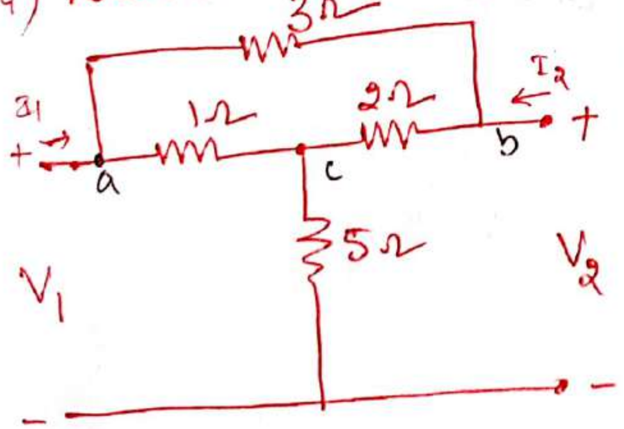
$$V_1 = 2.92V_2 + 0.4I_2 \quad \text{—— (5)}$$

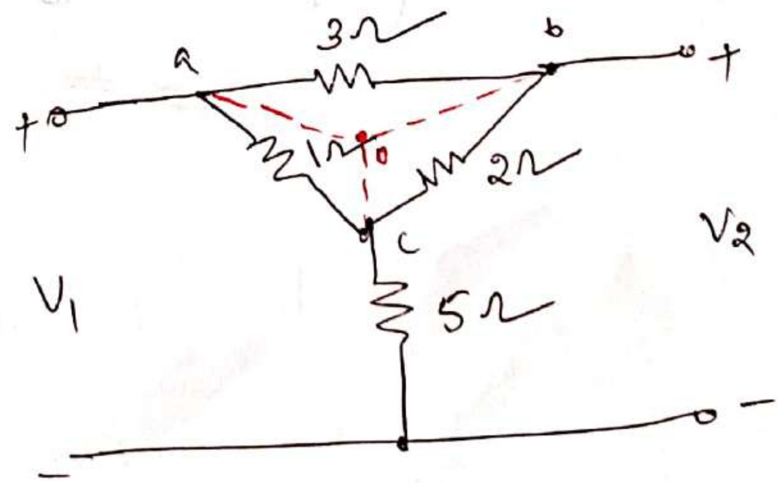
Compare (5) & (1)

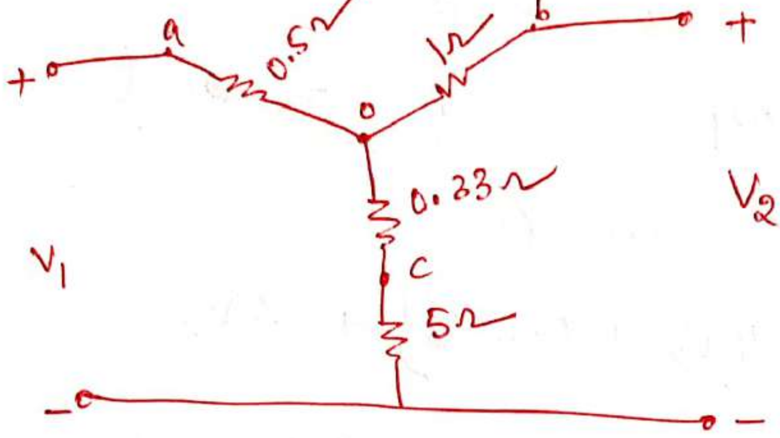
$\boxed{A = 2.92}$ $\boxed{B = -0.4}$

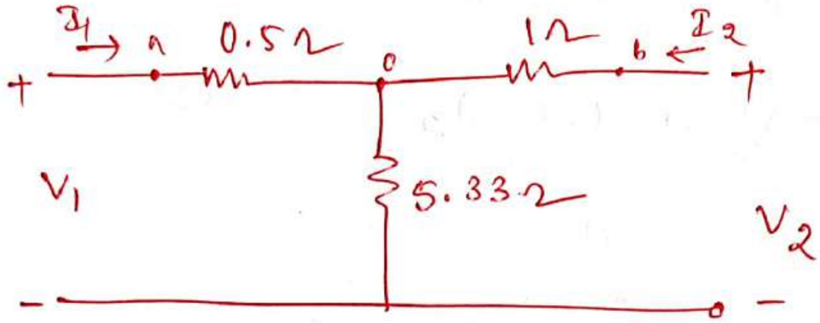
$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 2.92 & -0.4 \\ -0.04 & -0.2 \end{bmatrix}$$

24) Determine Z-parameters for the n/w. June/July-18









Since T-n/w,

$$Z_{11} = 5.83\,\Omega \qquad Z_{22} = 6.33\,\Omega$$

$$Z_{12} = Z_{21} = 5.33\,\Omega$$

$$\therefore \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 5.83 & 5.33 \\ 5.33 & 6.33 \end{bmatrix} \Omega$$

CBCS SCHEME

USN | | | | | | | | | | 15EC34

Third Semester B.E. Degree Examination, June/July 2018
Network Analysis

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Determine the equivalent resistance across XY shown in Fig.Q1(a) **(05 Marks)**

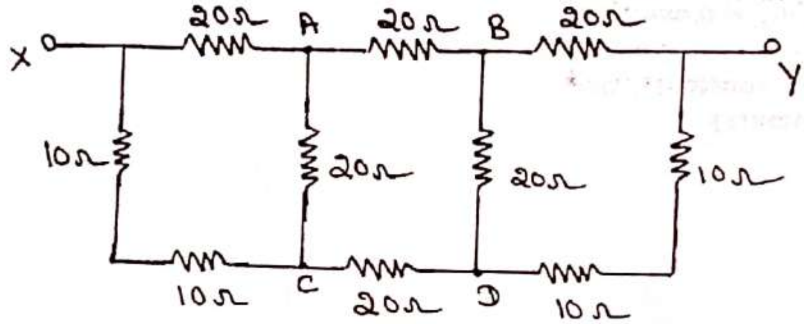


Fig.Q1(a)

b. Calculate the voltage across the 6Ω resistor using source shifting and transformation technique shown in Fig.Q1(b). **(05 Marks)**

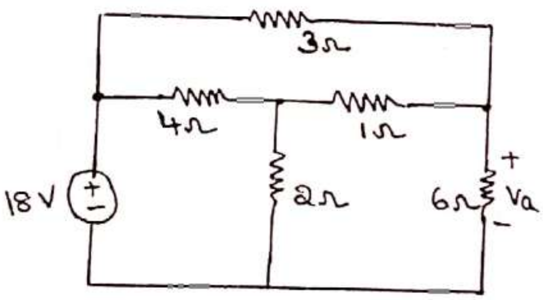


Fig.Q1(b)

c. Determine the power supplied by the dependent source of Fig.Q1(c) shown. **(06 Marks)**

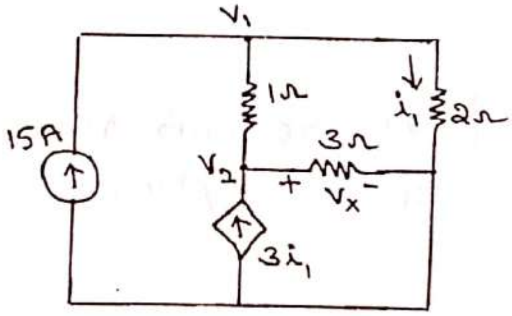


Fig.Q1(c)

OR

4 a. Using Millman's theorem, find I_L through R_L for the network shown in Fig.Q4(a). (06 Marks)

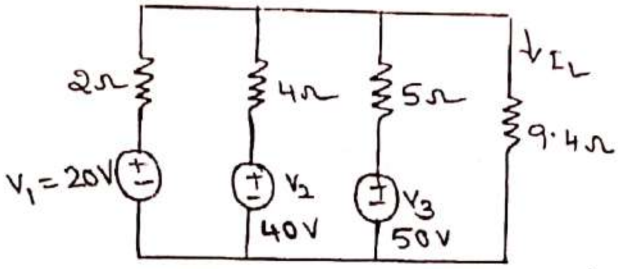


Fig.Q4(a)

b. Verify reciprocity theorem for the circuit shown in Fig.Q4(b). (06 Marks)

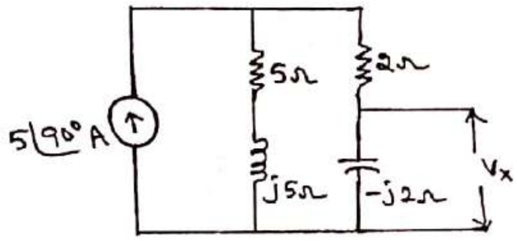


Fig.Q4(b)

c. State and explain maximum power transfer theorem. (04 Marks)

Module-3

5 a. In the circuit shown in Fig.Q5(a), the switch K is changed from position 1 to position 2 at t = 0, the steady state has been reached before switching. Find the values of $i, \frac{di}{dt}$ and $\frac{di^2}{dt^2}$ at $t=0$. (08 Marks)

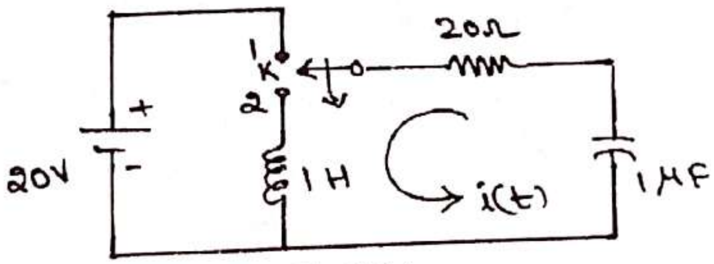


Fig.Q5(a)

b. The switch in the network shown in Fig.Q5(b) is closed at t = 0. Determine the voltage across the capacitor. Use Laplace transform. (08 Marks)

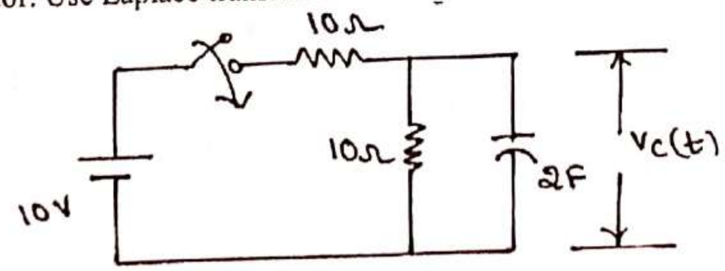


Fig.Q5(b)

OR

6 a. In the network shown in Fig.6(a), the switch K is opened at $t = 0$. At $t = 0^+$, solve for the values of v, $\frac{dv}{dt}$ and $\frac{d^2v}{dt^2}$ if $I = 2A$, $R = 200\Omega$ and $L = 1H$. **(08 Marks)**

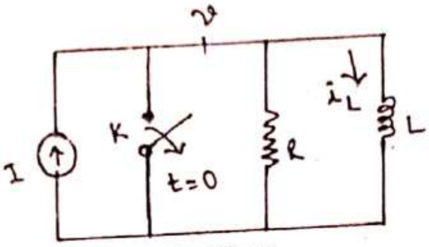


Fig.Q6(a)

b. Determine the Laplace transform of the periodic saw tooth waveform of Fig.Q6(b). Use gate function. **(08 Marks)**

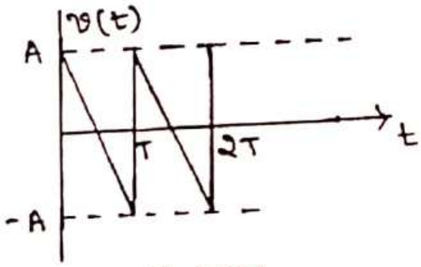


Fig.Q6(b)

Module-4

7 a. Derive for a resonant circuit, the resonant frequency $f_0 = \sqrt{f_1 f_2}$, where f_1 and f_2 are the two half power frequencies. **(07 Marks)**

b. Find the value of L for which the circuit shown in Fig.Q7(b) is resonant at a frequency of $w = 5000$ rad/sec. **(06 Marks)**

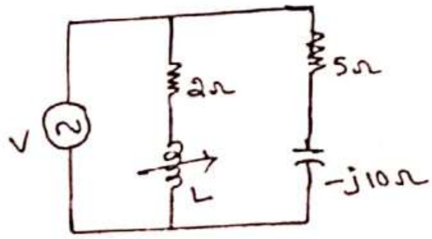


Fig.Q7(b)

c. A series RLC circuit has $R = 10\Omega$, $L = 0.01H$ and $c = 0.01\mu F$ and it is connected across 10mV supply. Calculate : i) f_0 ii) Q_0 iii) B.w. **(03 Marks)**

OR

8 a. A series RLC circuit has a resistance of 10Ω, an inductance of 0.3H and a capacitance of $100\mu F$. The applied voltage is 230V. Find : i) Resonant frequency ii) Quality factor iii) Lower and upper cut off frequencies iv) Bandwidth v) Current at resonance vi) currents at f_1 and f_2 vii) voltage across inductance at resonance. **(08 Marks)**

b. Derive an expression for the resonant frequency of a parallel resonant circuit. Also show that the circuit is resonant at all frequencies if $R_L = R_C = \sqrt{\frac{L}{C}}$ where R_L = Resistance in the inductor branch, R_C = resistance in the capacitor branch. **(08 Marks)**

Module-5

9 a. Find Y parameters and Z parameters for the circuit show in Fig.Q9(a). **(08 Marks)**

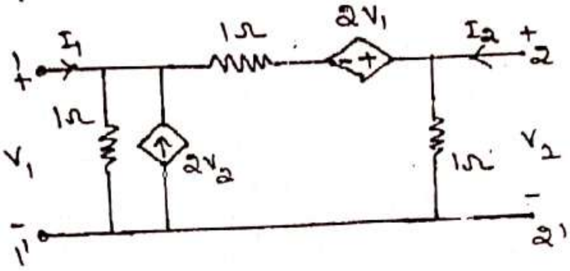


Fig.Q9(a)

b. Express ABCD parameters interms of Y-parameters and h-parameters. **(08 Marks)**

OR

10 a. Determine z parameters for the network shown in Fig.Q10(a). **(08 Marks)**

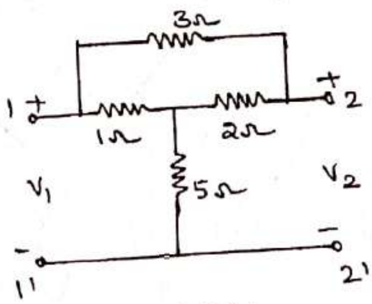


Fig.Q10(a)

b. Express h–parameters interms of Y–parameters. **(08 Marks)**

* * * * *

CBCS SCHEME

USN

17EC35

Third Semester B.E. Degree Examination, June/July 2019
Network Analysis

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define the following terms with examples:
   i) Active elements
   ii) Passive elements
   iii) Linear and non linear elements
   iv) Lumped node
   v) Unilateral and bilateral elements. (10 Marks)

b. Use the node analysis and find the value of V_x in the circuit shown in below Fig.Q.1(b). Such that the current through the impedance $(2 + J3)\Omega$ is zero.

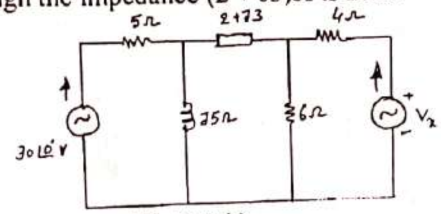


Fig.Q.1(b) (10 Marks)

OR

2 a. Derive an expression for i) Δ to Y transformation ii) Y to Δ transformation. (10 Marks)

b. Find the voltage across 20Ω resistor in the network shown in Fig.Q.2(b) below by using Mesh analysis method. (10 Marks)

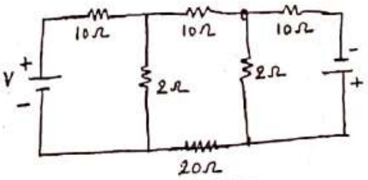


Fig.Q.2(b)

Module-2

3 a. State and prove Millman's theorem with an example. (10 Marks)

b. Find the Thevenin's equivalent circuit of Fig.Q.3(b) shown below: (10 Marks)

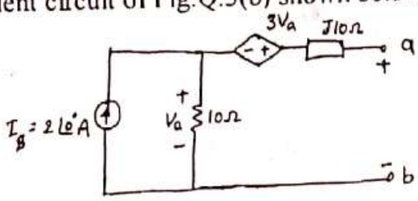


Fig.Q.3(b)

OR

4 a. Prove that the maximum power transferred from source to load when,

i) $R_L = R_o$ ii) $R_L = |Z_o|$ iii) $Z_L = \dot{Z}_o$ **(10 Marks)**

b. Find the value of i_b using Norton's equivalent circuit when $R = 667\Omega$, refer Fig.Q.4(b). **(10 Marks)**

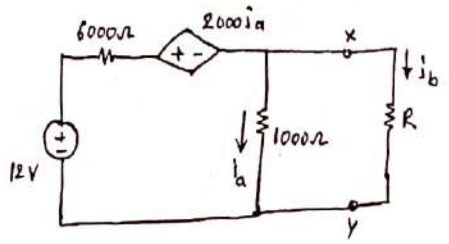


Fig.Q.4(b)

Module-3

5 a. Determine i, $\frac{di}{dt}, \frac{d^2i}{dt^2}$ at $t = 0^+$, when the switch is closed at $t = 0$, from the Fig.Q.5(a) shown below. **(10 Marks)**

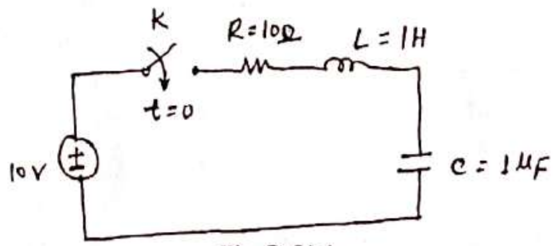


Fig.Q.5(a)

b. Find :

i) $i(0^-)$ and $v(0^+)$

ii) $\frac{di(0^+)}{dt}$ and $\frac{dv(0^+)}{dt}$

iii) $I(\infty)$ and $v(\infty)$

from the circuit shown in Fig.Q.5(b) below. **(10 Marks)**

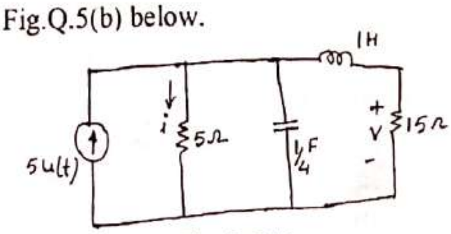


Fig.Q.5(b)

OR

6 a. Deduce the Laplace transform of the following:

i) $\text{Sin}^2 t$ ii) $\text{Cos}^2 t$ iii) Sinwt iv) $\int_0^t i(t).dt$ **(10 Marks)**

b. State and prove Initial and Final value theorems. **(10 Marks)**

Module-4

7 a. Demonstrate the terms: i) Resonance ii) Q-factor iii) Band width iv) Selectivity v) Half power frequency pertaining to a R-L-C series circuit. **(10 Marks)**

b. Prove that the Resonating frequency in a R-L-C series circuit is geometrical mean of half power frequencies i.e. $f_0 = \sqrt{f_1 f_2}$. **(10 Marks)**

OR

8 a. Evaluate w_0, Q, BW and half power frequencies and the output voltage V at W_0. refer Fig.Q.8(a). **(10 Marks)**

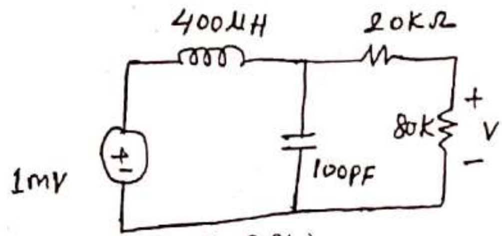


Fig.Q.8(a)

b. Derive an expression for resonance by varying R_L in parallel RLC circuit. **(10 Marks)**

Module-5

9 a. Express Z parameters in terms h parameters and what are hybrid parameters. **(10 Marks)**

b. Determine the transmission parameters for the network shown Fig.Q.9(b) below. **(10 Marks)**

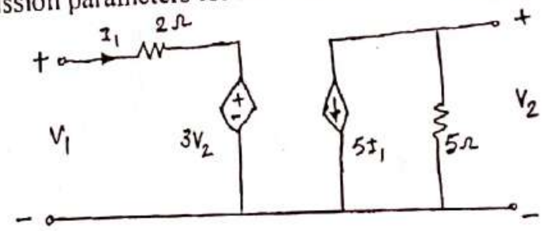


Fig.Q.9(b)

OR

10 a. Obtain the condition of transmission parameters for two networks connected in cascade. **(10 Marks)**

b. Determine the Z-parameters for the circuit shown in Fig.Q.10(b) below. **(10 Marks)**

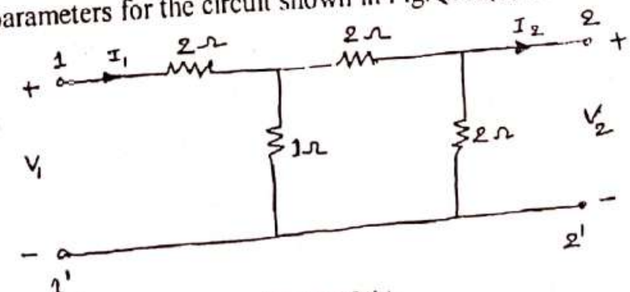


Fig.Q.10(b)

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CBCS SCHEME

USN

17EC35

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Network Analysis

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the expression for: (i) Δ to Y transformation (ii) Y to Δ transformation **(10 Marks)**

b. Calculate the voltage across the 6Ω resistor in the network of Fig.Q1(b) using source shifting technique.

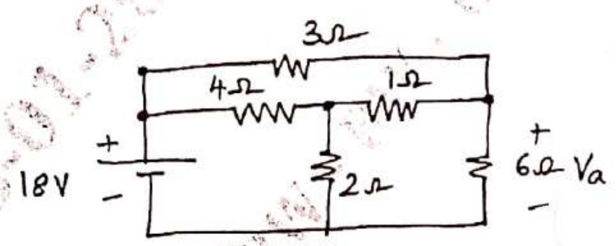

Fig.Q1(b) **(10 Marks)**

OR

2 a. Determine the resistance between the terminals A and B of the network shown in Fig.Q2(a).

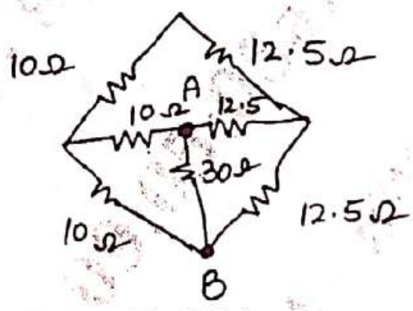

Fig.Q2(a) **(10 Marks)**

b. Find currents in all the branches of the network shown in Fig.Q2(b) using mesh analysis.

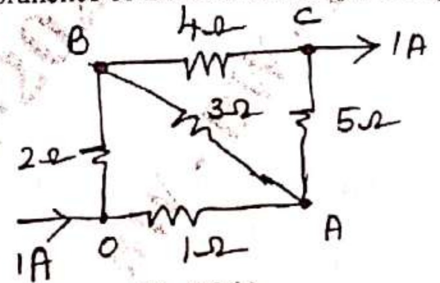

Fig.Q2(b) **(05 Marks)**

c. Find voltages V_1 and V_2 in the network shown in Fig.Q2(c) using node analysis method.

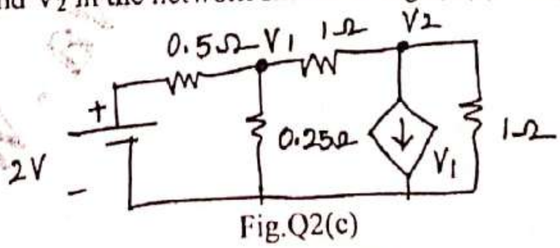

Fig.Q2(c) **(05 Marks)**

Module-2

3 a. Obtain Thevenin's equivalent network for Fig.Q3(a).

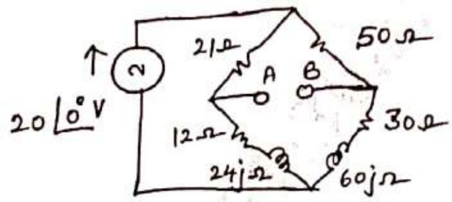

Fig.Q3(a) (08 Marks)

b. State and prove Millman's theorem. (06 Marks)

c. For the circuit shown in Fig.Q3(c), find the voltage V_x and verify reciprocity theorem.

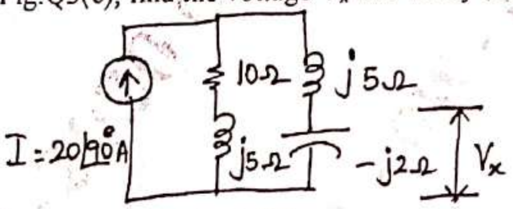

Fig.Q3(c) (06 Marks)

OR

4 a. State and prove maximum power transfer theorem for AC circuits (when R_L and X_L are varying) (10 Marks)

b. Find 'V' in the circuit shown in Fig.Q4(b) using super position theorem.

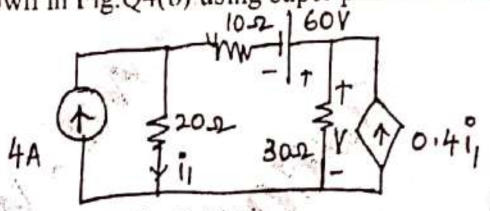

Fig.Q4(b) (10 Marks)

Module-3

5 a. What is the significance of initial conditions? Write a note on initial and final conditions for basic circuit elements. (05 Marks)

b. In the network shown in Fig.Q5(b) switch 'S' is changed from A to B at t = 0 having already established a steady state in position A shown that at $t = 0^+$, $i_1 = i_2 = \frac{-V}{R_1 + R_2 + R_3}$ and $i_3 = 0$.

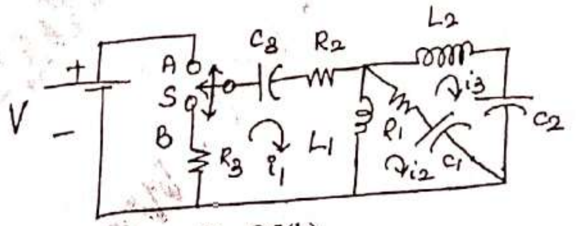

Fig.Q5(b) (10 Marks)

c. In the network of Fig.Q5(c) switch 'S' is closed at t = 0 with zero initial current in the inductor. Find i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at $t = 0^+$ if $R = 10\,\Omega$, L = 1 H and V = 10 Volts.

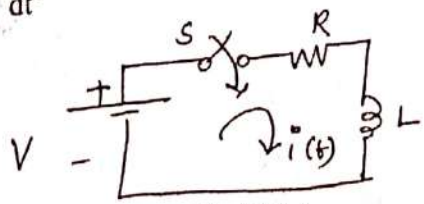

Fig.Q5(c) (05 Marks)

OR

6 a. Obtain Laplace transform of:
   (i) Step function
   (ii) Ramp function
   (iii) Impulse function **(10 Marks)**

b. Find the Laplace transform of the waveform shown in Fig.Q6(b).

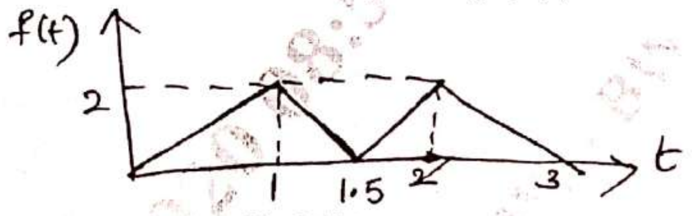

Fig.Q6(b) **(10 Marks)**

Module-4

7 a. Derive the relation between bandwidth and quality factor B.W = f_0/Q. **(10 Marks)**

b. Show that the value of capacitance for max voltage across the capacitor in case of capacitor tuning series resonance is given by $C = \frac{L}{R^2 + X_L^2}$.

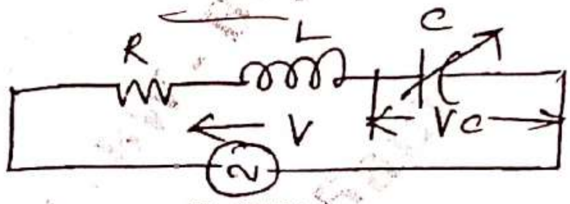

Fig.Q7(b) **(10 Marks)**

OR

8 a. Derive for f_0 for parallel resonance circuit when the resistance of the capacitance is considered.

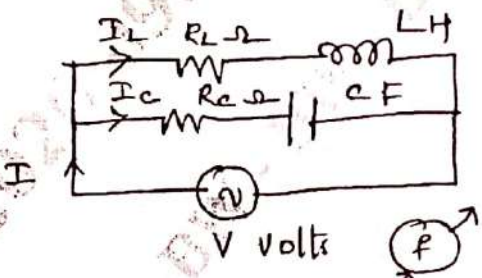

Fig.Q8(a) **(10 Marks)**

b. Find the value of L for which the circuit in Fig.Q8(b) resonates at ω = 5000 rad/sec.

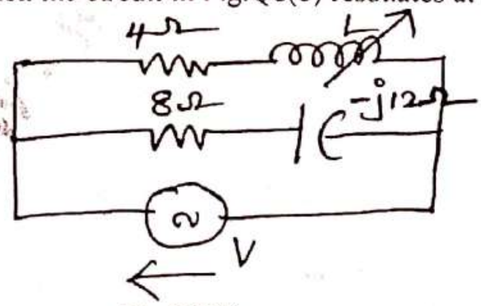

Fig.Q8(b) **(10 Marks)**

Module-5

9 a. Derive the expression of Z parameters in terms of Y parameters. (10 Marks)

b. Determine Y and Z parameters for the network shown in Fig.Q9(b).

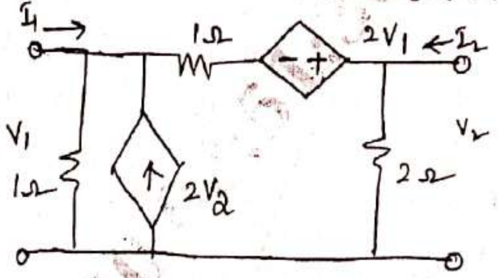

Fig.Q9(b) (10 Marks)

OR

10 a. Derive the expression of h parameters in terms of ABCD parameters. (10 Marks)

b. Find ABCD constants and show that AD – BC = 1 for the network shown in Fig.Q10(b).

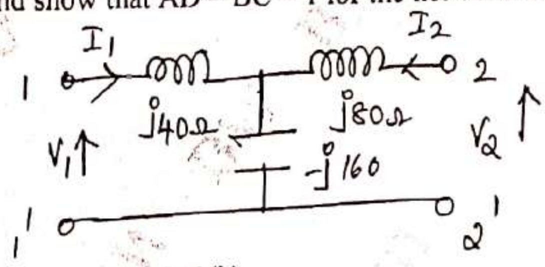

Fig.Q10(b) (10 Marks)

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ADICHUNCHANAGIRI UNIVERSITY

18EC35

Third Semester BE Degree Examination November 2020
(CBCS Scheme)

Time: 3 Hours | Max Marks: 100 marks

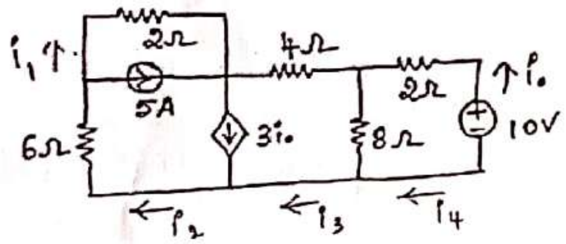
Sub: Network Analysis

Q P Code: 62305

Instructions: 1. Answer **five full** questions.
2. Choose one full question from each module.
3. Your answer should be specific to the questions asked.
4. write the same question numbers as they appear in this question paper.
5. Write Legibly

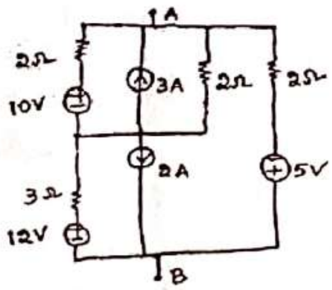
Module – 1

1 a Find the currents i_1, i_2, i_3 and i_4 using mesh analysis for the circuit shown in figure Q1(a). 07 marks



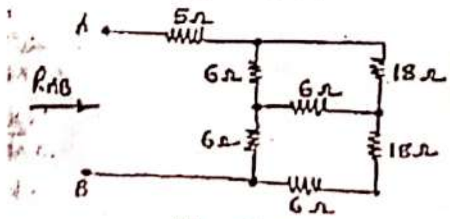
Fig, Q1(a)

b Reduce the network shown in figure Q1(b) to a single voltage source in series with a resistance between terminals A and B. 07 marks



Fig, Q1(b)

c Determine R_{AB} in the network shown in figure Q1(c). 06 marks

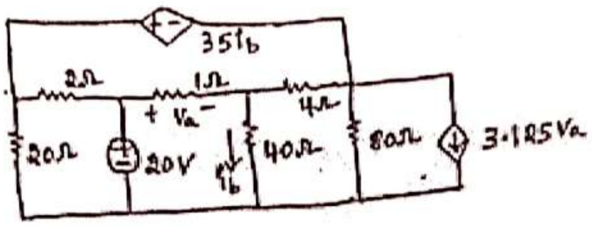


Fig, Q1(c)

PTO

Or

2 a Determine the power supplied by the 20V voltage source to the circuit shown in figure Q2(a) using nodal analysis. 10 marks



Fig, Q2(a)

b Distinguish between the following with suitable examples 10 marks

i) Linear and non-linear elements.
ii) Dependent and independent sources.
iii) Supernode and supermesh.
iv) Ideal and practical current sources.
v) Unilateral and bilateral elements.

Module – 2

3 a State and prove Thevenin's theorem. 10 marks

b Using superposition theorem, obtain the response I for the network shown in figure Q3(b). 10 marks

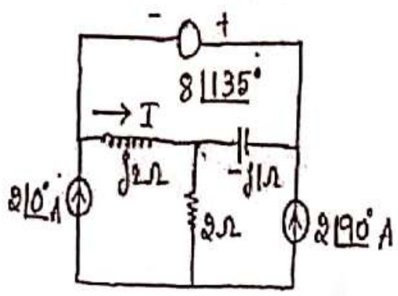


Fig. Q3(b)

Or

4 a State and prove maximum power transfer theorem for an AC circuit with an impedance as the load with variable R_L and fixed load reactance. 10 marks

b For the circuit shown in figure Q4(b), find Thevenin's equivalent circuit across the terminals ab. 10 marks

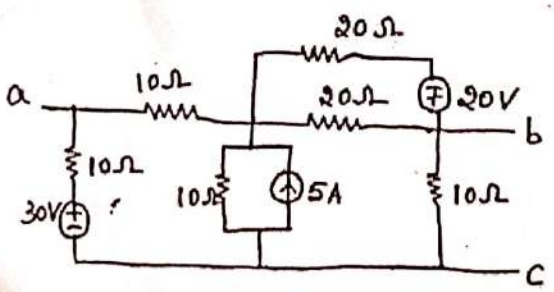


Fig. Q4(b)

Module – 3

5 a The network shown in figure Q5(a), has two independent node pairs. Switch K is opened at t=0, find the following quantities at $t=0^+$. 10 marks

i) V_1 ii) V_2 iii) dV_1/dt iv) dV_2/dt v) di_L/dt

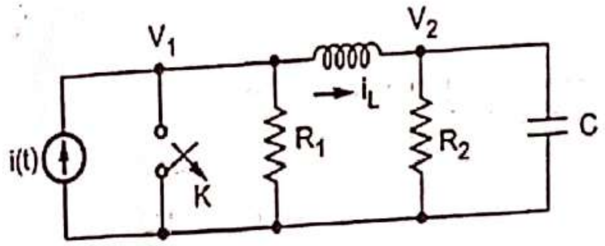


Fig. Q5(a)

b In the network shown in figure Q5(b), K is changed from position 1 to 2 at t=0. Solve for i, di/dt and d^2i/dt^2 at $t=0^+$. 10 marks

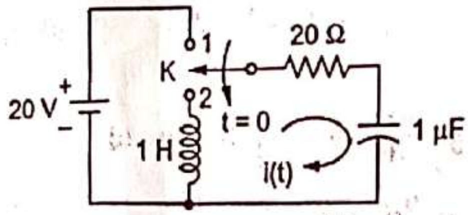


Fig. Q5(b)

Or

6 a Obtain the Laplace transform of saw tooth waveform shown in figure Q6(a). 06 marks

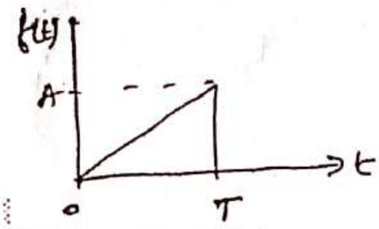


Fig. Q6(a)

b Find the Laplace transform of i) $\delta(t)$ ii) t iii) e^{-at} 06 marks

c Find initial and final value theorem for the function given below. 08 marks

$F(s)=(s^3+7s^2+5)/s(s^3+3s^2+4s+2)$

Module – 4

7 a Two coils one of $R_1=0.51\Omega$, $L_1=32mH$, the other of $R_2=1.3\Omega$ and $L_2=15mH$ and two capacitors of $25\mu F$ and $62\mu F$ are all in series with a resistance of 0.24Ω. Determine the following of this circuit. 10 marks

i) Resonance frequency ii) Q of each coil iii) Q of the circuit

iv) Cut-off frequencies v) Power dissipated of resonance if E=10V.

b In a two RL-RC parallel resonant circuit L=0.4H and C=40μF, obtain resonant frequency for the following values of R_L and R_C. 10 marks

i) $R_L=120\ \Omega$, $R_C=80\ \Omega$ ii) $R_L=R_C=80\Omega$ iii) $R_L=80\ \Omega$, $R_C=0\ \Omega$

iv) $R_L=R_C=100\ \Omega$ v) $R_L=R_C=120\ \Omega$

PTO

Or

8 a A RLC series circuit consists of 50 Ω resistance, 0.2H inductance and 10μF capacitance with an applied voltage of 20V. Determine i) Resonant frequency ii) Q factor iii) Lower and upper frequency limits iv) Bandwidth. 10 marks

b Define the following terms with reference to resonant circuit 04 marks
i) Resonance ii) Q-factor iii) Half-power frequency iv) Selectivity

c Derive the expression for resonant frequency of a parallel resonant circuit with lossless capacitor in parallel with a coil of resistance R and inductance L. 06 marks

Module – 5

9 a Define Y parameters. Determine the Y parameters for the network shown in figure Q9(a). 08 marks

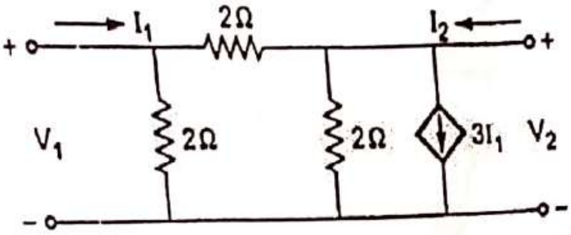


Fig. Q9(a)

b The Z parameters of a two port network are $Z_{11}=20\Omega$, $Z_{12}=10\Omega$, $Z_{21}=10\Omega$ and $Z_{22}=10\Omega$. Find its Y and ABCD parameters. 06 marks

c Define h-parameters. Represent h-parameters in terms of ABCD parameters. 06 marks

Or

10 a Define transmission parameters and Z parameters. Express transmission parameters in terms of impedance parameters. 10 marks

b Find the h parameters of the network shown in figure Q10(b). Also draw its equivalent circuit. 10 marks

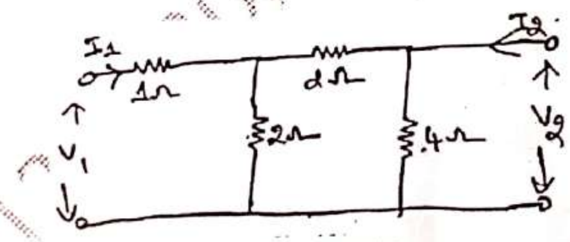


Fig. Q10(b)

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ADICHUNCHANAGIRI UNIVERSITY

18EC35

Third Semester BE Degree Examination January 2020

(CBCS Scheme)

Time: 3 Hours | Max Marks: 100 Marks

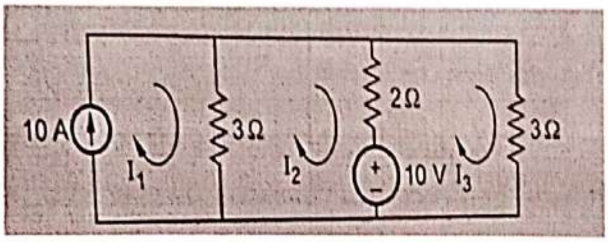
Sub: Network Analysis

Instructions:
1. Answer five full questions
2. Choose one full question from each module
3. Your answer should be specific to the questions asked
4. Write the same question numbers as they appear in this question paper
5. Write Legibly.

Module -1

1 a. Derive expressions for i) Star to Delta conversion
ii) Delta to Star conversion **(10 marks)**

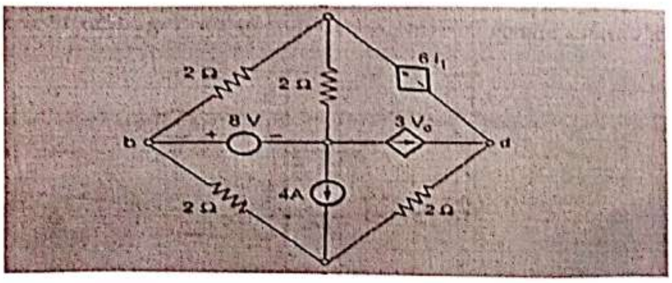
b. Write the mesh equation for the circuit shown below and determine mesh currents using mesh analysis. **(10 marks)**



OR

2 a. Explain the classification of Networks. **(10 marks)**

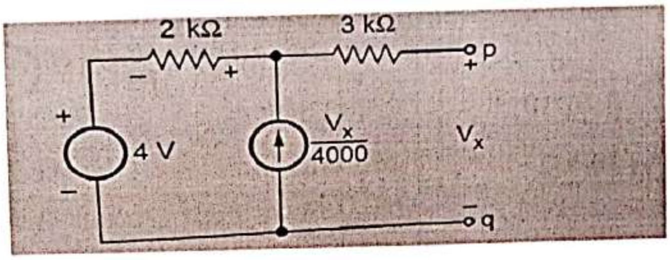
b. For the network shown below, find the node voltages V_d and V_c. **(10 marks)**



Module -2

3 a. State and prove Maximum power transfer theorem for AC circuits. **(10 marks)**

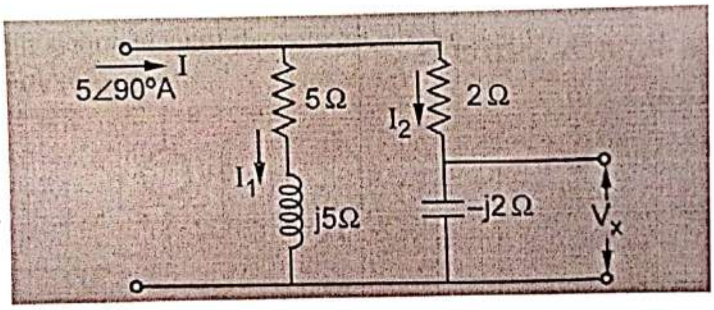
b. Find the Thevenin's equivalent of the network shown below. **(10 marks)**



OR

4 a. State and prove Millman's Theorem. **(10 marks)**

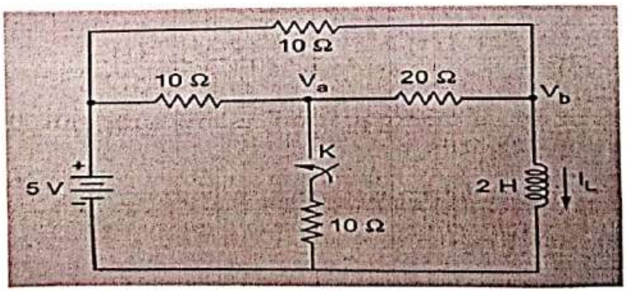
b. Find the voltage V_x and verify the reciprocity theorem for the network shown below. **(10 marks)**



Module -3

5 a. Write a note on initial conditions in basic circuit elements. **(10 marks)**

b. In the network shown below, a steady state is reached with the switch K open. At t =0, the switch is closed. For the element values given, determine the values of $V_a(0^-)$ and $V_a(0^+)$. **(10 marks)**



OR

6 a. State and prove i) Initial value theorem and ii) Final value theorem. **(10 marks)**

b. Find the Laplace transform of the fallowing: i) $\sin^2 t$ and ii) $\cos^2 t$ **(10 marks)**

Module -4

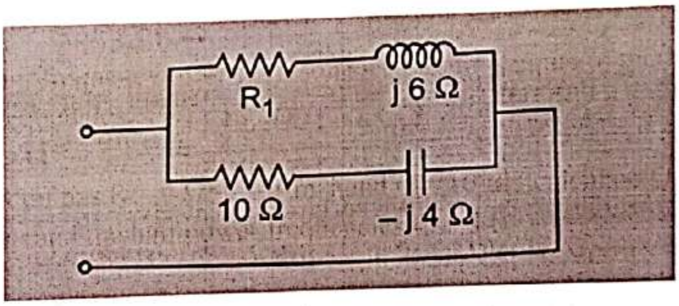
7 a. Show that resonant frequency of series resonance circuit is equal to the geometric mean of two half power frequencies. **(10 marks)**

b. A series RLC circuit has R = 4 Ω, L = 1 mH and C = 10 μF, calculate Q-factor, bandwidth, resonant frequency and the half power frequencies f_1 and f_2. **(10 marks)**

OR

8 a. Derive the expression for resonant frequency for parallel circuit containing resistance in both the branches. **(10 marks**

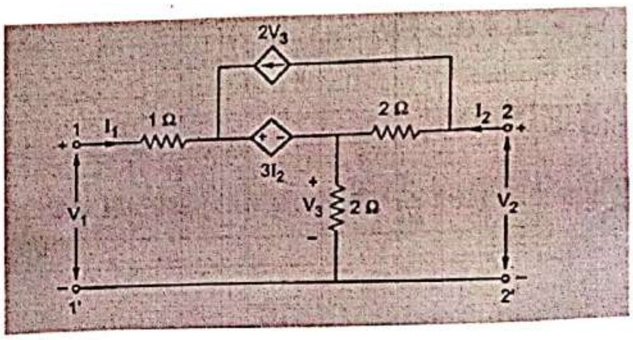
b. Find the value of R_1 such that the circuit given below is resonant. **(10 marks)**



Module -5

9 a. Define Y parameters and derive Y parameters in terms of h parameters. **(10 marks)**

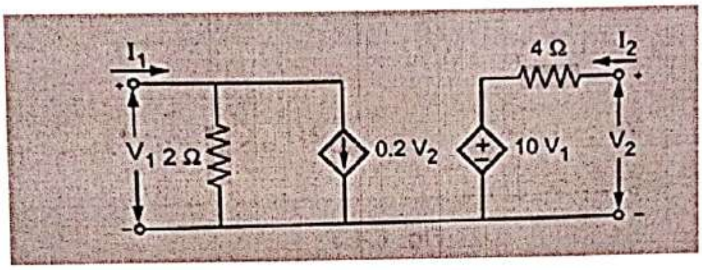
b. Find Z parameters for the circuit shown below. **(10 marks)**



OR

10 a. Define Z parameters and derive Z parameters in terms of y parameters. **(10 marks)**

b. Determine Y parameters for the circuit shown below. **(10 marks)**



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