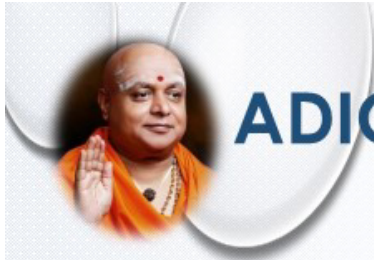


|| Jai Sri Gurudev ||



ADICHUNCHANAGIRI UNIVERSITY



BGS Institute of Technology

BG Nagara – 571448, Mandya District



Webinar Series – 2020-21

**Department of Electronics and Communication
Engineering**

System Design using Xilinx Vivado on Zynq Soc

CoreEL
Technologies

Main Objectives:

- Hardware Modelling Overview
- Verilog Language Concepts
- Dataflow Modeling
- Test Benches Writing
- Coding for Synthesis
- RTL to FPGA Flow (Demonstration)
- FPGA Based Design using System Generator

Speaker:

Mr. Prakash
Lead Application Engineer,
CoreEL Technologies

Date: 13th May 2020, 10.00AM

Online Platform: Webex Meetings



Topic: System Design using Xilinx Vivado for ZynqSoC

Speaker:Mr.Prakash, Lead Application Engineer. Coreel Technologies, Bengaluru

No. of Participants:140

Online Plat form:Webex

Date: 13th May 2020

e-certificate is provided to all the participants by coreel technologies

Mr.Prakash was discussed about his company for 5 min and another 1 hour and 30 minutes he completely discussed about *Use Xilinx Design Constraints* to communicate performance. Rapidly architect an embedded *system* targeting the ARM processor of *Zynq* located on *ZedBoard* using *Vivado* and IP Integrator. Extend the hardware *system* with *Xilinx* provided peripherals. Create a custom peripheral and add it to the *system*. Students are able to Use Xilinx Design Constraints to communicate performance, Rapidly architect an embedded system targeting the ARM processor of Zynq located on ZedBoard using Vivado and IP Integrator, Extend the hardware system with Xilinx provided peripherals, Create a custom peripheral and add it to the system, Debug a design using Vivado hardware analyzer and how to use Vivado HLS to generate an IP-XACT compliant hardware accelerator.Creating HDL Design and Xilinx design constraints.